# Good Practice for the NCP1602 CSZCD Pin Design and PCB Layout

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APPLICATION NOTE

NCP1602 combines the current sense (CS) and the core demagnetization detection (ZCD, zero crossing detection) signals into a single pin named CSZCD. In some noisy environment, a non-optimum choice of sensing resistors combined with a dense PCB layout can lead to a unstable operation of 1602. This application note describes good practices for designing the circuitry around the NCP1602 CSZCD pin, including choice of component values and PCB layout.

### Drain Connection for CSZCD Pin (Sensitivity to PCB Parasitics)

When trying to reduce the no-switching standby consumption current by increasing (above 1 MΩ) the resistance ($R_{CS1}$ + $R_{CS2}$) of the CSZCD bridge connected between the drain and the source of the power MOSFET (see Figure 1), the sensitivity of the CSZCD pin to PCB parasitic capacitors is increased. In some case, it can lead to non-functionality caused for example by a constant false triggering of OCP (Over Current Protection) or OVP (Over Voltage Protection). This is due to the fact that the CSZCD voltage is distorted and the internal circuitry cannot work as intended. While recommendations for avoiding such CSZCD pin sensitivity are given in [1], this application note will focus only on optimizing the CSZCD pin operations.

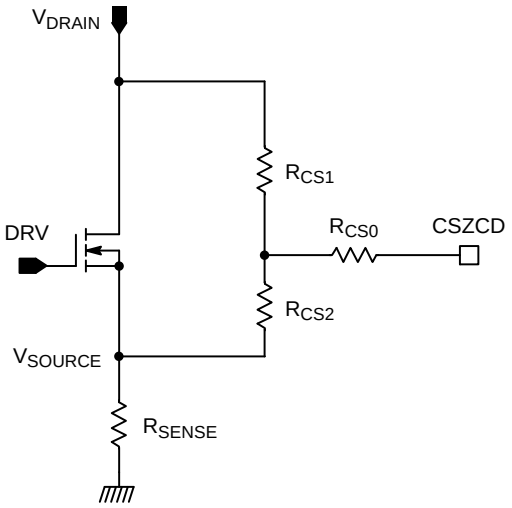


**Figure 1. The CSZCD Connection without an Auxiliary Winding**

For safety and reliability reasons, the $R_{CS1}$ resistor is generally made with three resistors in series ($R_{CS1,a}$, $R_{CS1,b}$ and $R_{CS1,c}$) shown in Figure 2.

Safety:

If one resistor gets shorted, the drain voltage which is high (e.g., 400 V) is not directly applied to CSZCD pin and no damage will be observed.

Reliability:

If $R_{CS1,a}$, $R_{CS1,b}$ and $R_{CS1,c}$ have the same resistance value, the power MOSFET drain voltage is divided by the resistors and each $R_{CS1,i}$ resistor has roughly one third of drain voltage across it, well under the max voltage rating of each resistor.

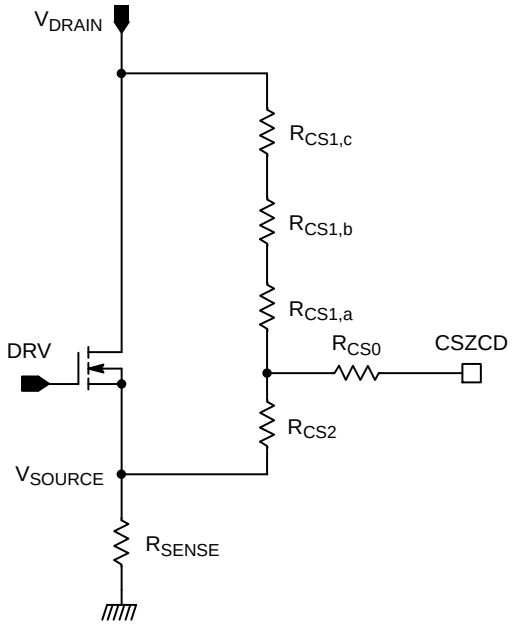


**Figure 2. CSZCD Pin Circuitry Showing How $R_{CS1}$ is Made**

What are not shown in Figure 2 are the PCB parasitic capacitors $C_{pi}$ and the CSZCD pin to GND parasitic capacitance $C_{CSZCDpar}$ which are shown in Figure 3. The parasitic capacitors $C_{p0}$ and $C_{p7}$ do not cause problems because $C_{p0}$ together with the resistance $R_{SENSE}$ create a very high frequency pole (well above the MHz range) and the same for $V_{DRAIN}$ output impedance and $C_{p7}$.

On the contrary, when $R_{CS1,a}$, $R_{CS1,b}$ and $R_{CS1,c}$ values are getting close to 1 MΩ, very small parasitic capacitance values like for example 159 fF (femto farad) can creates a pole at 1 MHz which is right in the range of the ringing frequency of power MOSFET drain voltage. As we want a distortion-free drain voltage image at the CSZCD pin, we are in trouble.

There is an internal zero inside the controller for cancelling the effect of the pole made by $R_{CS}$ resistors and the CSZCD pin to grounds parasitic capacitor (mostly due to the TSOP6 package) $C_{CSZCDpar}$. In case $C_{pi}$ have a low effect ($C_{pi}$ values low and/or $R_{CSi}$ values low), $R_{CS}$ values are determined by the following Equations 1, 2 and 3.

$$R_{CS2} \geq 20\ k\Omega \quad \text{(eq. 1)}$$

$$\frac{R_{CS2} + R_{CS1,a} + R_{CS1,b} + R_{CS1,c}}{R_{CS2}} = 138 \pm 10\% \quad \text{(eq. 2)}$$

$$\left[ R_{CS0} + \frac{1}{\frac{1}{R_{CS2}} + \frac{1}{R_{CS1,a}+R_{CS1,b}+R_{CS1,c}}} \right] \cdot C_{CSZCDpar} \quad \text{(eq. 3)}$$

$$= 500\ ns$$

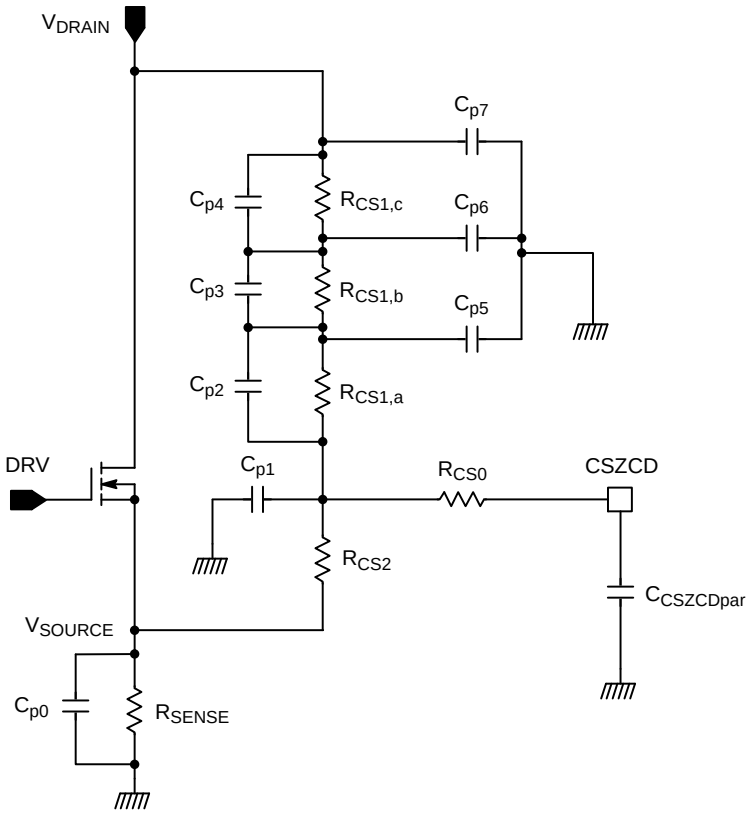


**Figure 3. CSZCD Pin External Circuitry Showing Some of the PCB Parasitic Capacitors**

Unfortunately, it is not possible to cancel the effects of MHz-range poles and zeroes created by the combination of PCB parasitic capacitances $C_{pi}$ (there are even more $C_{pi}$ than those shown in Figure 3, for example those coupling each node of the $R_{CS}$ resistor ladder and DRV signal, $V_{IN}$ signal, …) by a schematic trick, and the only way to avoid problems is to keep $C_{pi}$ values as low as possible and/or avoid $R_{CS1,a}$, $R_{CS1,b}$ and $R_{CS1,c}$ to have a value greater than 333-kΩ ($R_{CS1,a}$ + $R_{CS1,b}$ + $R_{CS1,c}$ lower than 1-MΩ limit).

While application note [1] already contains information, it is good to remind the following.

*Do Not Do This*

Using $R_{CS1,a}$ = $R_{CS1,b}$ = $R_{CS1,c}$ with $R_{CS1}$ = $R_{CS1,a}$ + $R_{CS1,b}$ + $R_{CS1,c}$ if $R_{CS1}$ is greater than 1 MΩ.

*($R_{CS1}$ + $R_{CS2}$) Lower than 1 MΩ*

Three $R_{CS1}$ 200-V SMD1206 resistors can be placed in series $R_{CS1}$ = $R_{CS1,a}$ + $R_{CS1,b}$ + $R_{CS1,c}$.

*($R_{CS1}$ + $R_{CS2}$) Greater than 1 MΩ and Lower than 5.12 MΩ*

Bench experiments have shown that three SMD 200-V resistors of same value in series ($R_{CS1}$ = $R_{CS1,a}$ + $R_{CS1,b}$ + $R_{CS1,c}$) lead to false fault tripping (e.g., OVP2 false triggering). It is advised to have one 500-V SMD high-value resistor $R_{CS1,c}$ on the drain side (e.g., 5.1 MΩ for The EVB) with two low value (e.g., 240 kΩ) 200-V SMD resistors in series ($R_{CS1,a}$ + $R_{CS1,b}$). This is to avoid having inter-resistor capacitance to GND and observe difficulties to discharge them before a $t_{ON}$ cycle.

*Type of $R_{CS}$ Resistors*

Bench experiments have proven SMD1206 & 0805 superiority, parasitic capacitance wise, over trough-hole resistors for $R_{CS1}$, $R_{CS2}$ and $R_{CS0}$ resistors.

*PCB Layout Considerations*

$R_{CS0}$ must be placed as close as possible to CS/ZCD pin voltage and $R_{CS1}$ and $R_{CS2}$ as close as possible to $R_{CS0}$.

PCB traces connecting the $R_{CSi}$ resistors must be kept as short as possible, the width of the trace being as small as possible (minimum parasitic capacitance).

It is wise to keep a safety distance of 1 cm between the high value resistors of the CSZCD bridge and DRV, $V_{IN}$, $V_{DRAIN}$ copper traces to avoid coupling.

*Showing Bad CSZCD Waveforms*

As said before, very low parasitic capacitances between the nodes of the CSZCD divider bridge and GND creates a distorted CSZCD signal as shown in Figure 4 from both simulation and measurements. At the beginning of on-time, a voltage bump is added with can trigger OVS or OCP protections and during dead-time the parasitic capacitors are masking the image of drain voltage ringing which is well seen when the parasitic capacitances are low (see blue simulated curve on Figure 4)

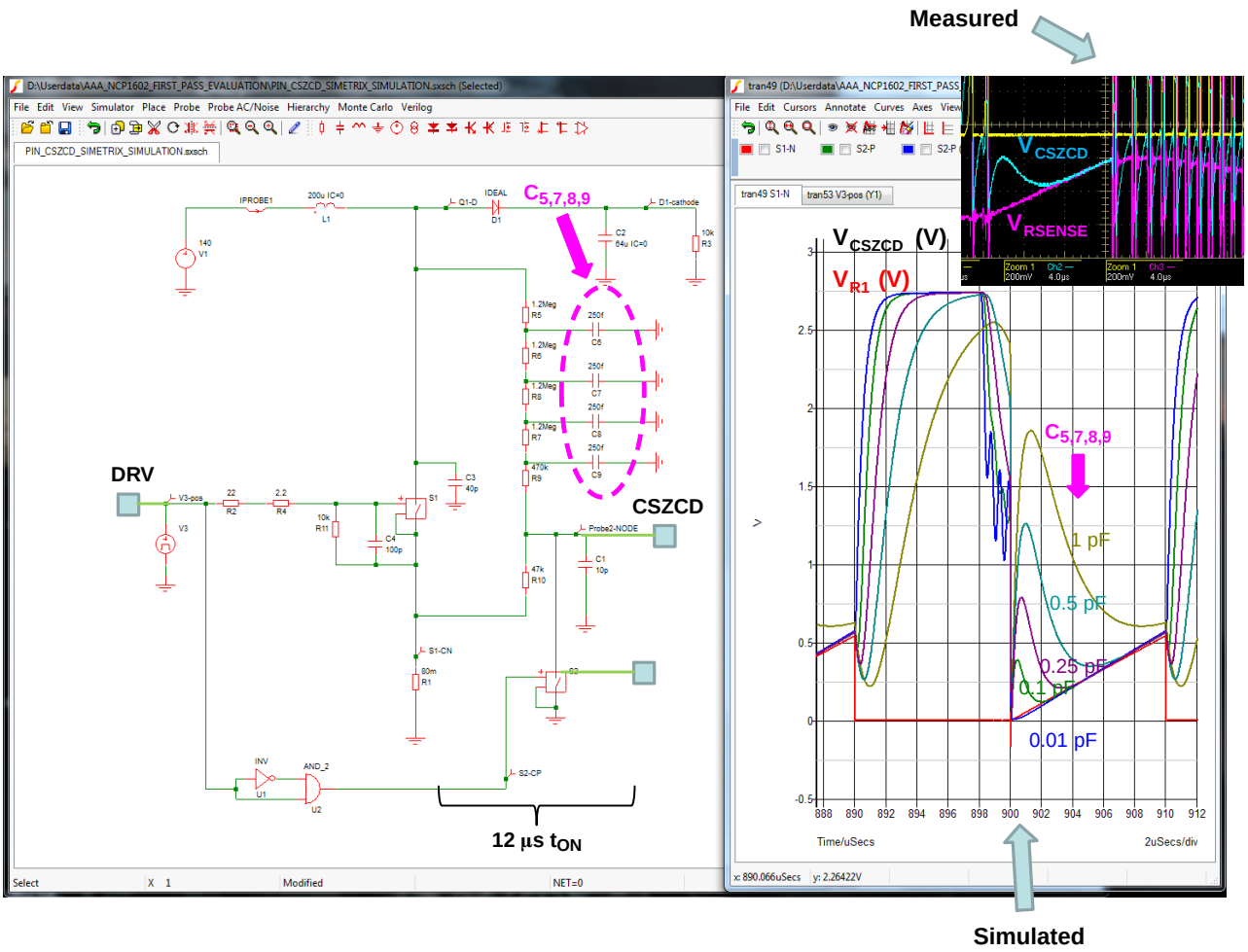


**Figure 4. Effect of Parasitic Capacitances on CSZCD Signal**

## References

[1] Application Note AND9218/D “5 Key Steps to Designing a Compact, High-Efficiency PFC Stage Using the NCP1602” which can be downloaded at: http://www.onsemi.com/pub_link/Collateral/AND9218−D.PDF



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