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AND9720/D

KAI-29050 versus KAI-43140 Key Differences

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APPLICATION NOTE

Architecture

KAI−29050

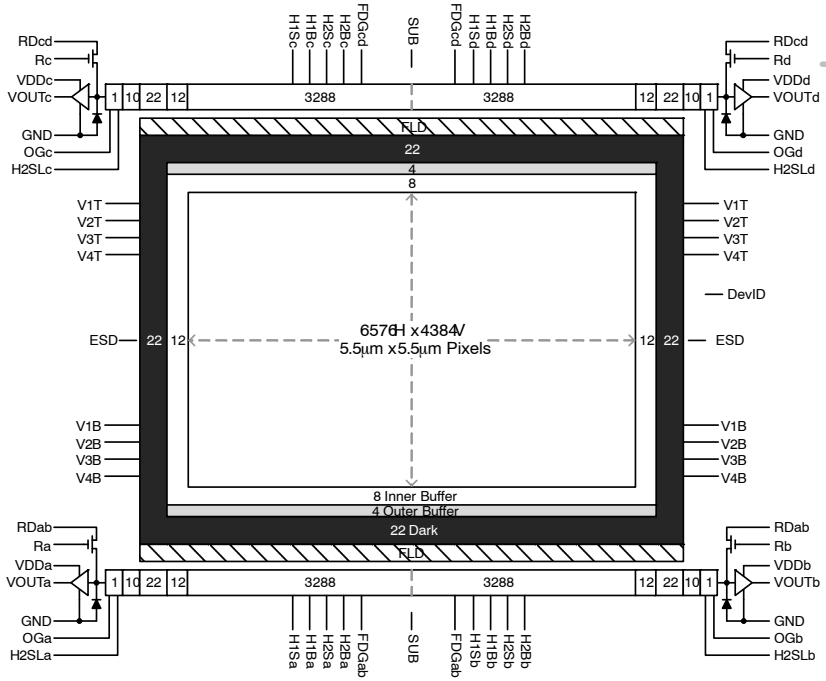


Figure 1. KAI−29050 Block Diagram

KAI−43140

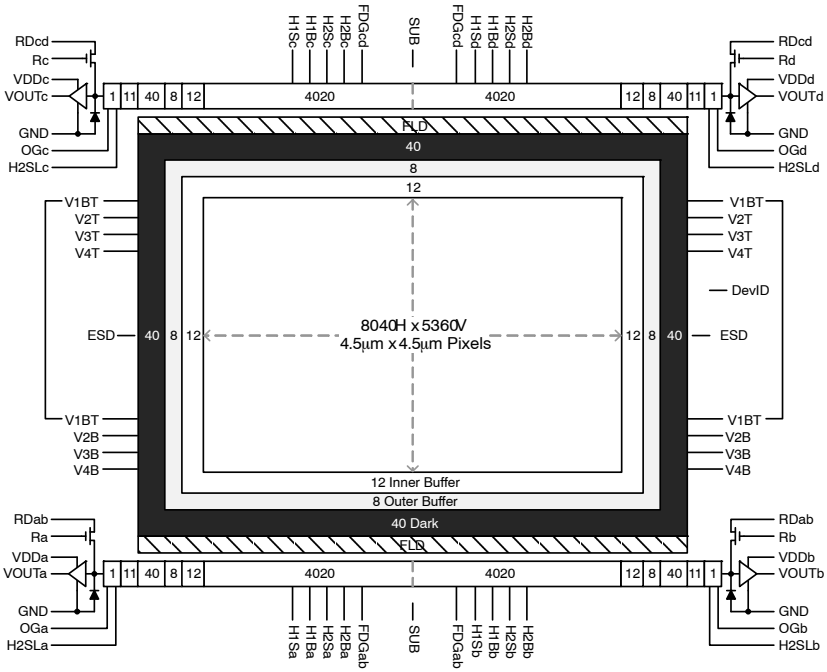


Figure 2. KAI−43140 Block Diagram

Dark Reference Pixels

KAI−29050

There are 22 dark rows at the top and 22 dark rows at the bottom of the image sensor. The dark rows at the top and bottom of the sensor are not entirely dark and so should not be used as a dark reference level. The 22 dark columns on the left and right side of the image sensor can be used as a dark reference region. Only the center 20 columns of the 22 column dark reference region should be used as a dark reference due to the potential of light leakage into the first column of the dark reference region.

KAI−43140

There are 40 dark rows at the top and 40 dark rows at the bottom of the image sensor. The dark rows at the top and bottom of the sensor are not entirely dark and so should not be used as a dark reference level. The 40 dark columns on the left and right side of the image sensor can be used as a dark reference region. Only the center 38 columns of the 40 column dark reference region should be used as a dark reference due to the potential of light leakage into the first column of the dark reference region.

Dummy Pixels

KAI−29050

Within each horizontal shift register there are 11 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

KAI−43140

Within each horizontal shift register there are 12 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

KAI−29050

There are 12 unshielded pixels on all four sides of the Active Pixel area. These pixels are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non−uniformities. The outer buffer pixels are less sensitive as compared to the inner buffer pixels and active pixels.

- There are 4 outer buffer rows at the top and bottom of the image sensor.
- There are 0 outer buffer columns on the left and right side of the image sensor.
- There are 8 inner buffer rows at the top and bottom of the image sensor.
- There are 12 inner buffer columns on the left and right side of the image sensor.

KAI−43140

There are 20 unshielded pixels on all four sides of the Active Pixel area. These pixels are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non−uniformities. The outer buffer pixels are less sensitive as compared to the inner buffer pixels and active pixels.

- There are 8 outer buffer rows at the top and bottom of the image sensor.
- There are 8 outer buffer columns on the left and right side of the image sensor.
- There are 12 inner buffer rows at the top and bottom of the image sensor.
- There are 12 inner buffer columns on the left and right side of the image sensor.

General Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	KAI−29050	KAI−43140
Architecture	Interline CCD; Progressive Scan	Interline CCD; Progressive Scan
Total Number of Pixels	6644 (H) x 4452 (V)	8160 (H) x 5480 (V)
Number of Effective Pixels	6600 (H) x 4408 (V)	8080 (H) x 5400 (V)
Number of Active Pixels	6576 (H) x 4384 (V)	8040 (H) x 5360 (V)
Active Pixel Resolution	28.8 Megapixels	43.1 Megapixels
Pixel Size	5.5 μm (H) x 5.5 μm (V)	4.5 μm (H) x 4.5 μm (V)
Active Image Size	36.17 mm (H) x 24.11 mm (V) 43.47 mm (diag.) 35 mm Optical Format	36.18 mm (H) x 24.12 mm (V) 43.48 mm (diag.) 35 mm Optical Format
Aspect Ratio	3:2	3:2
Number of Outputs	1, 2, or 4	1, 2, or 4
Charge Capacity	20,000 electrons	13,000 electrons
Output Sensitivity	34 μV/electron	42 μV/electron
Read Noise	12 electrons rms (f = 40 MHz)	12 electrons rms (f = 60 MHz)
Dynamic Range	64 dB	60 dB
Maximum Pixel Clock Speed	40 MHz	60 MHz
Package	72 pin PGA	72 pin PGA
Cover Glass	AR coated, 2 sides	AR coated, 2 sides

Package Pin Designations

The KAI−29050 and KAI−43140 use the same pin designations with the following exceptions:

- RD: The package pin designations have been updated for the RD pins.
  - RDa and RDb: The RDa and RDb pins are internally connected together on the die for both the KAI−29050 and KAI−43140 image sensors.

    For the KAI−29050 image sensor the pins are named RDa and RDb

    For the KAI−43140 image sensor these two pins are both named RDab

    NOTE: For both the KAI−29050 and KAI−43140 image sensors, these two pins should be connected to the same bias voltage source.
  - RDc and RDd: The RDc and RDd pins are internally connected together on the die for both the KAI−29050 and KAI−43140 image sensors.

    For the KAI−29050 image sensor the pins are named RDc and RDd

    For the KAI−43140 image sensor these two pins are both named RDcd

    NOTE: For both the KAI−29050 and KAI−43140 image sensors, these two pins should be connected to the same bias voltage source.
- V1B and V1T
  - KAI−29050: The V1B and V1T pins are not internally connected together on the die.
  - KAI−43140: The V1B and V1T pins are internally connected together on the die and have been named V1BT.

    NOTE: For the KAI−43140 image sensor, all four V1BT pins should be connected to the same clock driver source.

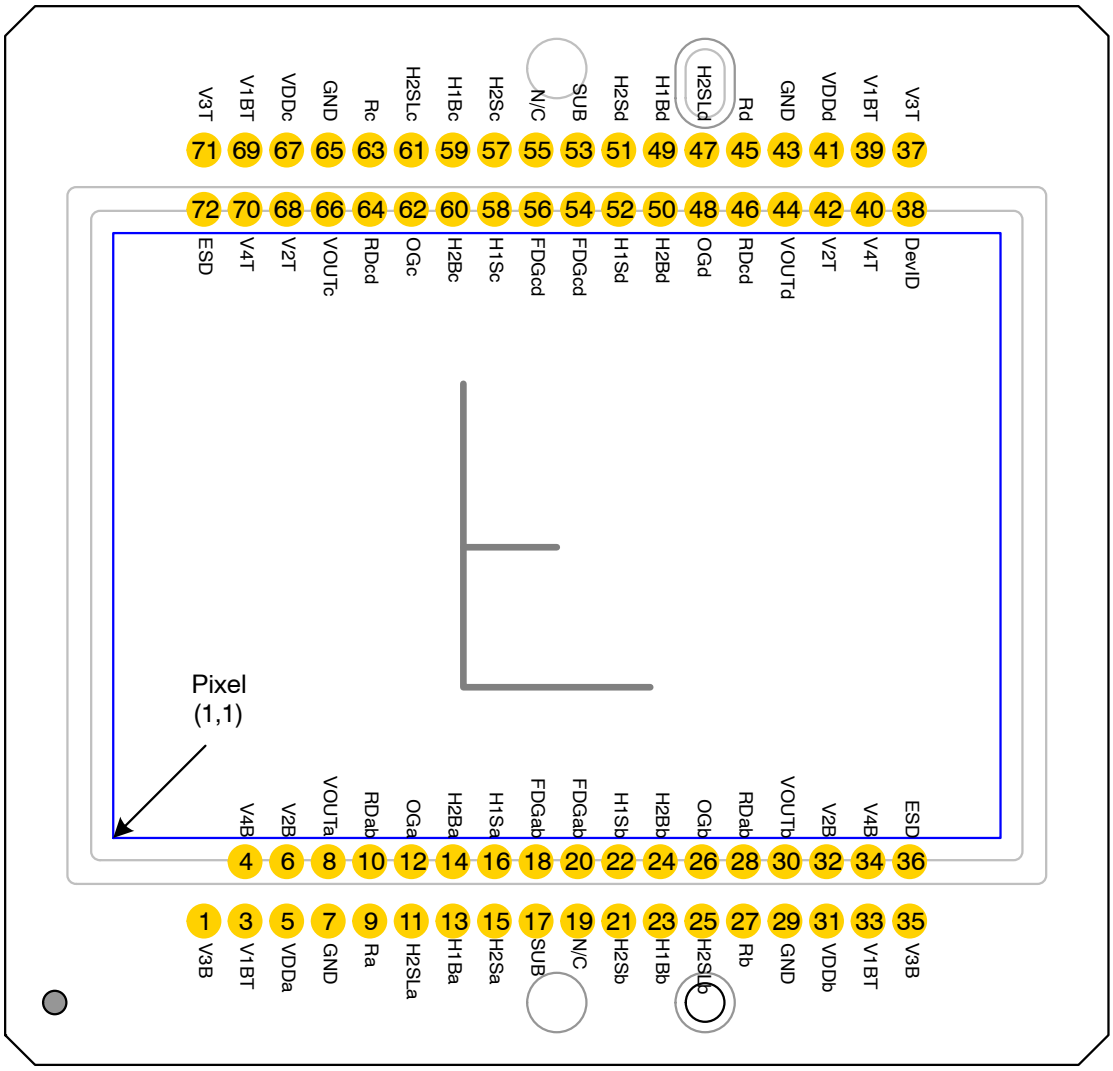


Figure 3. KAI−43140 Package Pin Designations − Top View

Table 2. KAI−43140 PIN DESCRIPTION

Pin	Name	Description	Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom	72	ESD	ESD Protection Disable
			71	V3T	Vertical CCD Clock, Phase 3, Top
3	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top	70	V4T	Vertical CCD Clock, Phase 4, Top
4	V4B	Vertical CCD Clock, Phase 4, Bottom	69	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top
5	VDDa	Output Amplifier Supply, Quadrant a	68	V2T	Vertical CCD Clock, Phase 2, Top
6	V2B	Vertical CCD Clock, Phase 2, Bottom	67	VDDc	Output Amplifier Supply, Quadrant c
7	GND	Ground	66	VOUTc	Video Output, Quadrant c
8	VOUTa	Video Output, Quadrant a	65	GND	Ground
9	Ra	Reset Gate, Quadrant a	64	RDcd	Reset Drain, Quadrants c and d
10	RDab	Reset Drain, Quadrants a and b	63	Rc	Reset Gate, Quadrant c
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a	62	OGc	Output Gate, Quadrant c
12	OGa	Output Gate, Quadrant a	61	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a	60	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a	59	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a	58	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a	57	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
17	SUB	Substrate	56	FDGcd	Fast Line Dump Gate, Top
18	FDGab	Fast Line Dump Gate, Bottom	55	N/C	No Connect
19	N/C	No Connect	54	FDGcd	Fast Line Dump Gate, Top
20	FDGab	Fast Line Dump Gate, Bottom	53	SUB	Substrate
21	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b	52	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
22	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b	51	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
23	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b	50	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
24	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b	49	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
25	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b	48	OGd	Output Gate, Quadrant b
26	OGb	Output Gate, Quadrant b	47	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
27	Rb	Reset Gate, Quadrant b	46	RDcd	Reset Drain, Quadrants c and d
28	RDab	Reset Drain, Quadrants a and b	45	Rd	Reset Gate, Quadrant d
29	GND	Ground	44	VOUTd	Video Output, Quadrant d
30	VOUTb	Video Output, Quadrant b	43	GND	Ground
31	VDDb	Output Amplifier Supply, Quadrant b	42	V2T	Vertical CCD Clock, Phase 2, Top
32	V2B	Vertical CCD Clock, Phase 2, Bottom	41	VDDd	Output Amplifier Supply, Quadrant d
33	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top	40	V4T	Vertical CCD Clock, Phase 4, Top
34	V4B	Vertical CCD Clock, Phase 4, Bottom	39	V1BT	Vertical CCD Clock, Phase 1, Bottom and Top
35	V3B	Vertical CCD Clock, Phase 3, Bottom	38	DevID	Device Identification
36	ESD	ESD Protection Disable	37	V3T	Vertical CCD Clock, Phase 3, Top

1. Liked named pins are internally connected and should have a common drive signal.
2. N/C pins (19, 55) should be left floating.

Device ID

Table 3. DEVICE ID DESCRIPTION

Pin	Symbol	KAI−29050			KAI−43140			Units
		Min.	Nominal	Max.	Min.	Nominal	Max.	
DevID	DevID	200,000	300,000	400,000	230,000	260,000	300,000	Ω

DC Bias Operating Conditions

Table 4. DC OPERATING CONDITIONS

Pins	Symbol	KAI−29050			KAI−43140			Units
		Min.	Nominal	Max.	Min.	Nominal	Max.	
RDα	RD	+11.8	+12.0	+12.2	+12.3	+12.5	+12.7	V
OGα	OG	−2.2	−2.0	−1.8	+1.5	+1.7	+2.4	V
VDDα	VDD	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
GND	GND	+0.0	+0.0	+0.0	+0.0	+0.0	+0.0	V
SUB	SUB	+5.0	VAB	VDD	+5.0	VAB	VDD	V
ESD	ESD	−9.2	−9.0	−8.8	−9.2	−9.0	−8.8	V
VOUTα	Iout	−3.0	−7.0	−10.0	−3.0	−5.0	−10.0	mA

1. α denotes a, b, c, or d

Clock Levels

- The nominal value for the vertical clock low level is −8 V for the KAI−43140 as compared to the nominal value for the vertical clock low level of −9 V for the KAI−29050.
- The KAI−43140 requires positive voltages for the horizontal and reset clocks rails as compared to the KAI−29050 which requires negative voltages for the horizontal and reset clocks rails.
  - Example #1: The H1Sa clock voltage swing is +4 V to 0V on the KAI−43140 as compared to the KAI−29050 which requires a clock voltage swing of 0 V to −4.4 V.
  - Example #2: The Reset clock voltage swing is +3.0 V to +7.0 V on the KAI−43140 as compared to the KAI−29050 which requires a clock voltage swing of −2.0 V to +3.0 V.

Table 5. CCD CLOCK VOLTAGE LEVELS

Pins	Symbol	Level	KAI−29050			KAI−43140			Units
			Min.	Nom.	Max	Min	Nom.	Max.	
V1B, V1T	V1_L	Low	−9.2	−9.0	−8.8	−8.2	−8.0	−7.8	V
	V1_M	Mid	−0.2	+0.0	+0.2	−0.2	+0.0	+0.2	
	V1_H	High	+12.8	+13.0	+14.0	+10.3	+10.5	+10.7	
V2B, V2T	V2_L	Low	−9.2	−9.0	−8.8	−8.2	−8.0	−7.8	V
	V2_H	High	−0.2	+0.0	+0.2	−0.2	+0.0	+0.2	
V3B, V3T	V3_L	Low	−9.2	−9.0	−8.8	−8.2	−8.0	−7.8	V
	V3_H	High	−0.2	+0.0	+0.2	−0.2	+0.0	+0.2	
V4B, V4T	V4_L	Low	−9.2	−9.0	−8.8	−8.2	−8.0	−7.8	V
	V4_H	High	−0.2	+0.0	+0.2	−0.2	+0.0	+0.2	
H1Sα	H1S_L	Low	−5.0 (2)	−4.4	−4.2	−0.2	+0.0	+0.2	V
	H1S_A	Amplitude	+4.2	+4.4	+5.0	+3.8	+4.0	+5.2	
H1Bα	H1B_L	Low	−5.0 (2)	−4.4	−4.2	−0.2	+0.0	+0.2	V
	H1B_A	Amplitude	+4.2	+4.4	+5.0	+3.8	+4.0	+5.2	
H2Sα	H2S_L	Low	−5.0 (2)	−4.4	−4.2	−0.2	+0.0	+0.2	V
	H2S_A	Amplitude	+4.2	+4.4	+5.0	+3.8	+4.0	+5.2	

Table 5. CCD CLOCK VOLTAGE LEVELS

Pins	Symbol	Level	KAI−29050			KAI−43140			Units
			Min.	Nom.	Max	Min	Nom.	Max.	
H2Bα	H2B_L	Low	−5.0 (2)	−4.4	−4.2	−0.2	+0.0	+0.2	V
	H2B_A	Amplitude	+4.2	+4.4	+5.0	+3.8	+4.0	+5.2	
H2SLα	H2SS_L	Low	−5.2	−5.0	−4.8	−0.2	+0.0	+0.2	V
	H2SL_A	Amplitude	+4.8	+5.0	+5.2	+3.8	+5.0	+5.2	
Rα	R_L	Low	−3.5	−2.0	−1.5	+2.0	+3.0	+3.2	V
	R_H	High	+2.5	+3.0	+4.0	+6.8	+7.0	+7.2	
SUB	SUB VES	High (3)	+29.0	+30.0	+40.0	–	–	+40.0	V
		Offset (4)	–	–	–	VAB + 24	VAB + 25	–	
FDGα	FDG_L	Low	−9.2	−9.0	−8.8	−8.2	−8.0	−7.8	V
	FDG_H	High	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	

1. α denotes a, b, c, or d
2. If the minimum horizontal clock low level is used (−5.0 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a −5.0 V to 0.0 V clock
3. With respect to ground
4. With respect to VAB

KAI−43140 Timing

The V1B and V1T pins are internally connected together on the die for the KAI−43140 image sensor. Therefore, the KAI−43140 timing differs from the KAI−29050 timing.

Table 6. KAI−43140 TIMING REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	T_{PD}	6	–	–	μs	
VCCD Leading Pedestal	T_{3P}	16	–	–	μs	
VCCD Trailing Pedestal	T_{3D}	16	–	–	μs	
VCCD Transfer Delay	T_D	4			μs	
VCCD Transfer	T_V	10	–	–	μs	
VCCD Clock Cross−over	V_{VCR}	75	–	100	%	
VCCD Rise, Fall Time	T_{VR}, T_{VF}	5	–	10	%	1
FDG Delay	T_{FDG}	5	–	–	μs	
HCCD Delay	T_{HS}	1	–	–	μs	
HCCD Transfer	T_E	16.66	–	–	ns	60 MHz Pixel Rate Clock
Shutter Transfer	T_{SUB}	1	–	–	μs	
Shutter Delay	T_{HD}	1	–	–	μs	
Reset Pulse	T_R	2.5	–	–	ns	
Reset – Video Delay	T_{RV}	–	2.2	–	ns	
H2SL – Video Delay	T_{HV}	–	3.1	–	ns	
Line Time	T_{LINE} (2)	89.21	–	–	μs	Dual/Quad HCCD Readout
		157.21	–	–		Single HCCD Readout
Frame Time	T_{FRAME} (3)	244.43	–	–	ms	Quad HCCD Readout
		488.86	–	–		Dual HCCD Readout (VOUTa, VOUTb)
		861.50	–	–		Single HCCD Readout

1. Relative to pulse width
2. Tline = Tv + Tv + Ths + Te * (pixel counts per line) + Te/2
3. Tframe = Tline * (Lines per Frame)

Timing Diagrams

The timing sequence for the clocked device pins may be represented as one of seven patterns (P1−P7) as shown in the table below.

Table 7. KAI−43140 TIMING SEQUENCES

Device Pin	Quad Readout	Dual Readout VOUTa, VOUTb	Dual Readout VOUTa, VOUTc	Single Readout (VOUTa)
V1BT	P1BT	P1BT	P1BT	P1BT
V2T	P2T	P4B	P2T	P4B
V3T	P3T	P3B	P3T	P3B
V4T	P4T	P2B	P4T	P2B
V2B	P2B			
V3B	P3B			
V4B	P4B			
H1Sa	P5			
H1Ba				
H2Sa [2]	P6			
H2Ba				
Ra	P7			
H1Sb	P5		P5	
H1Bb			P6	
H2Sb [2]	P6		P6	
H2Bb			P5	
Rb	P7		P7 [1] or Off [3]	P7 [1] or Off [3]
H1Sc	P5	P5 [1] or Off [3]	P5	P5 [1] or Off [3]
H1Bc				
H2Sc [2]	P6	P6 [1] or Off [3]	P6	P6 [1] or Off [3]
H2Bc				
Rc	P7	P7 [1] or Off [3]	P7	P7 [1] or Off [3]
H1Sd	P5	P5 [1] or Off [3]	P5	P5 [1] or Off [3]
H1Bd			P6	
H2Sd [2]	P6	P6 [1] or Off [3]	P6	P6 [1] or Off [3]
H2Bd			P5	
Rd	P7	P7 [1] or Off [3]	P7 [1] or Off [3]	P7 [1] or Off [3]

# Lines/Frame (Minimum)	2740	5480	2740	5480
# Pixels/Line (Minimum)	4092		8172	

1. For optimal sensor performance. May be clocked at a lower frequency. If clocked at a lower frequency, the frequency selected should be a multiple of the frequency used on the VOUTa and VOUTb registers.
2. H2SLx follows the same pattern as H2Sx. For optimal speed performance use a separate clock driver.
3. Off = R_H voltage for the Reset Gate and Hxx_H voltage for the Horizontal CCD gates. Note that there may be operating conditions (high temperature and/or very bright light sources) that will cause blooming from the unused c/d register into the image area.

Photodiode Transfer Timing

A row of charge is transferred to the HCCD on the falling edge of V1 as indicated in the P1BT pattern below. Using this timing sequence, the leading dummy row or line is combined with the first dark row in the HCCD. The “Last Line” is dependent on readout mode – either 2740 or 5480 minimum line counts required. It is important to note that, in general, the rising edge of a vertical clock (patterns P1−P4) should be coincident or slightly leading a falling edge at the same time interval. This is particularly true at the point where P1 returns from the high (3rd level) state to the mid−state when P4 transitions from the low state to the high state.

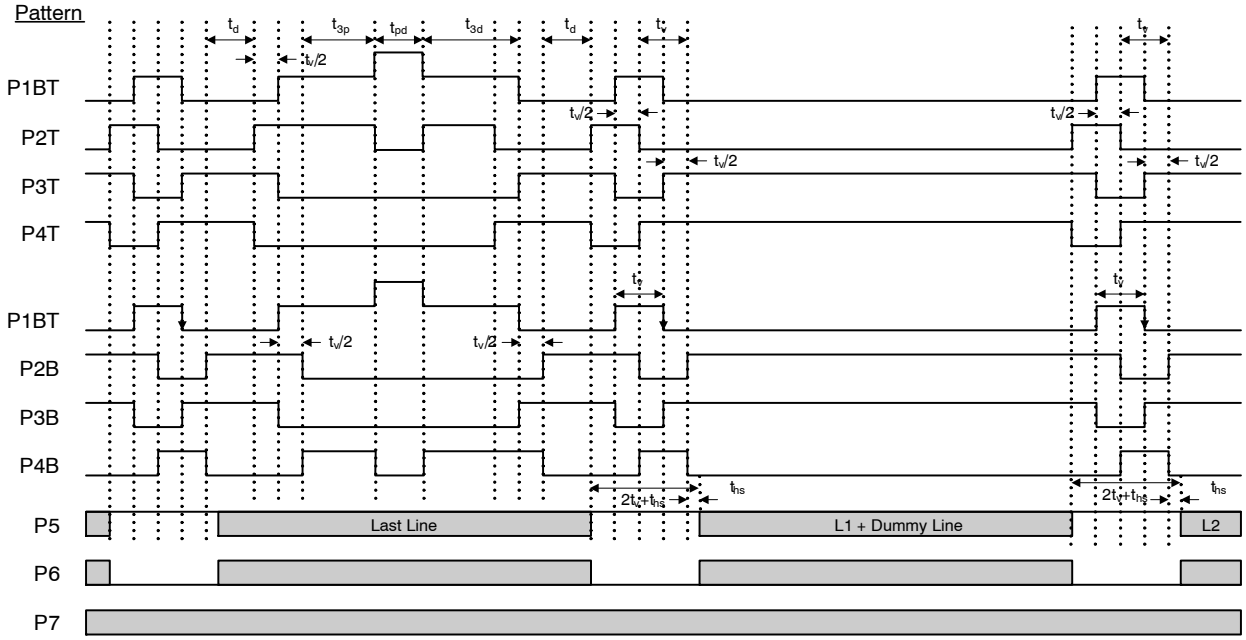


Figure 4. KAI−43140 Photodiode Transfer Timing

Line and Pixel Timing

Each row of charge is transferred to the output on the falling edge of H2SL (illustrated below, indicated as P6 pattern). The number of pixels in a row is dependent upon the readout mode. A minimum of 4092 pixel counts are required in either Quad readout or Dual (VOUTa, VOUTb) readout modes. A minimum of 8172 pixel counts are required in Single readout mode.

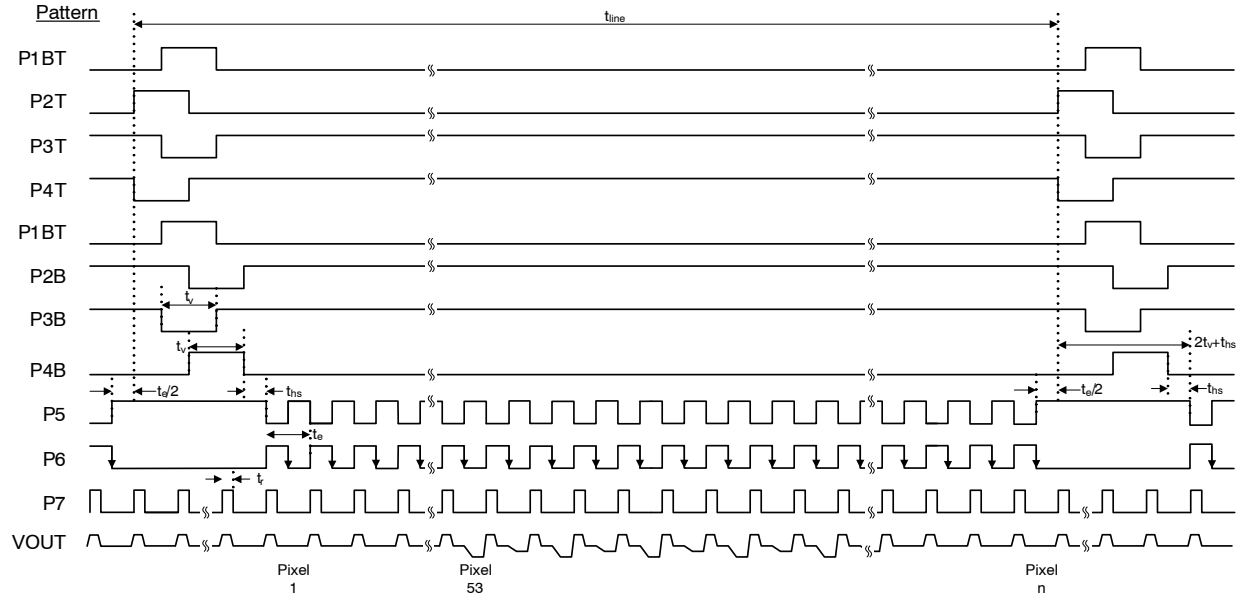
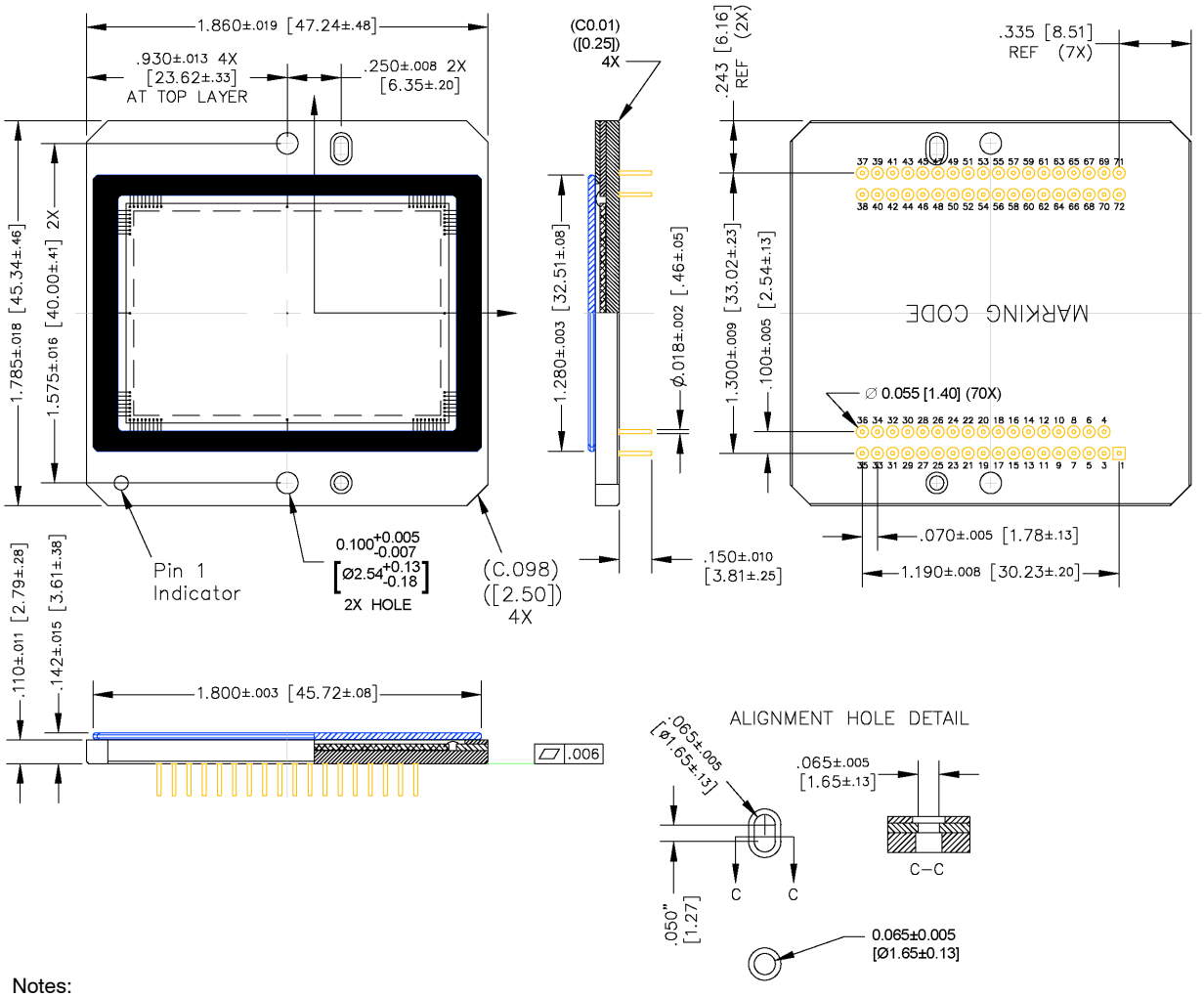


Figure 5. Line and Pixel Timing (Tline = Tv + Tv + Ths + Te * (pixel counts per line) + Te/2)

Completed Assembly

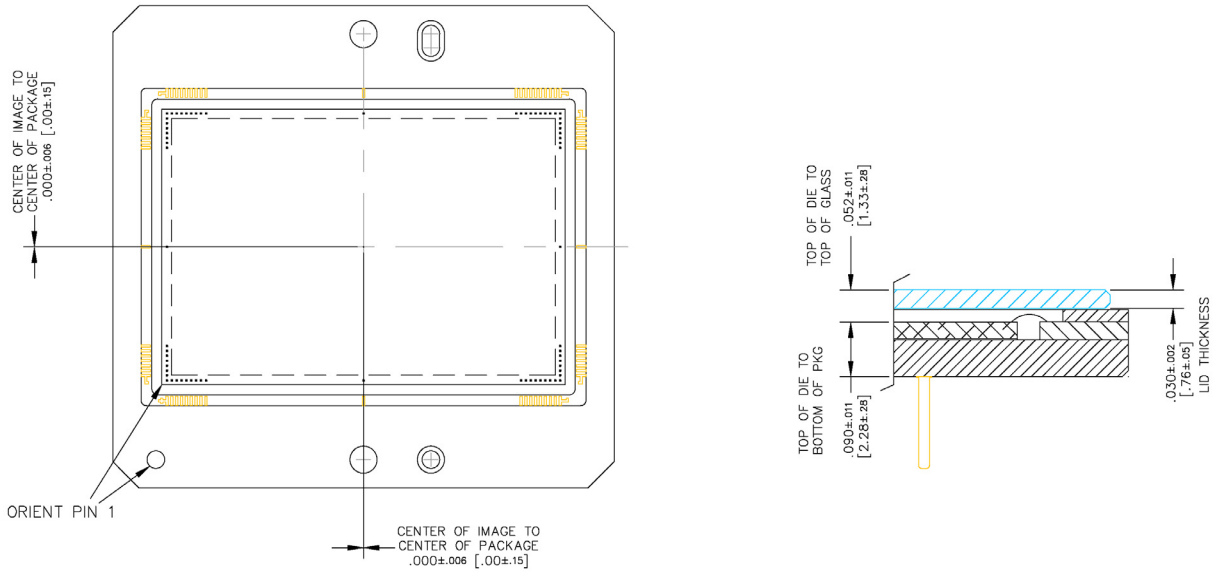
The KAI−29050 and KAI−43140 are to be manufactured with the same package and cover glass.



Notes:

1. See Ordering Information for marking code.
2. Cover glass not to overhang package holes or outer ceramic edges
3. Glass epoxy not to extend over image array
4. No materials to interfere with clearance through package holes
5. Units: IN [MM]

Figure 6. Completed Assembly (1 of 2)

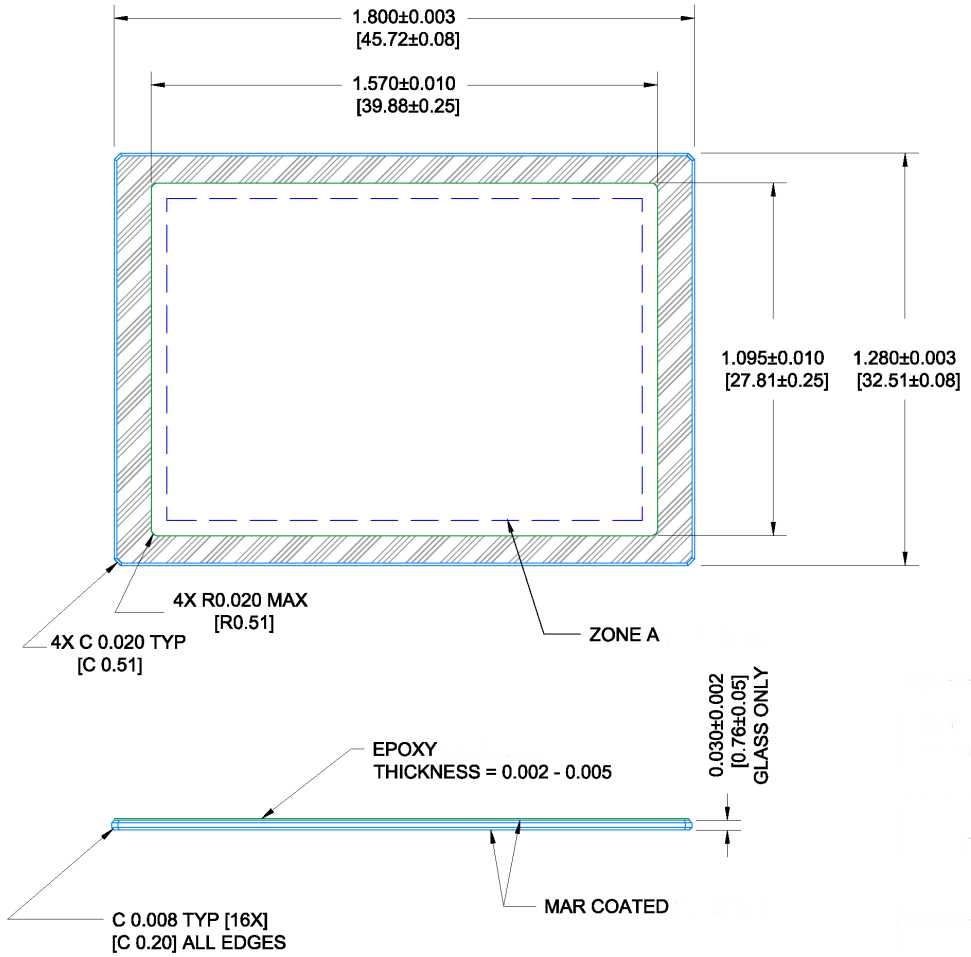


Note:
1. Units: IN [MM]

Figure 7. Completed Assembly (2 of 2)

Cover Glass Drawing

The KAI−29050 and KAI−43140 are to be manufactured with the same cover glass.



Note:

1. Substrate = Schott D 263T eco
2. Dust, Scratch, Inclusion Specification:
    a. 20 μm Max size in Zone A
    b. Zone A = 1.474 x 1.000 [16.43 x 10.08] centered
3. MAR coated both sides
4. Spectral Transmission
    a. 350 − 365 nm: T ≥ 88%
    b. 365 − 405 nm: T ≥ 94%
    c. 405 − 450 nm: T ≥ 98%
    d. 450 − 650 nm: T ≥ 99%
    e. 650 − 690 nm: T ≥ 98%
    f. 690 − 770 nm: T ≥ 94%
    g. 770 − 870 nm: T ≥ 88%
5. Units: IN [MM]

Figure 8. Cover Glass

Cover Glass Transmission

The KAI−29050 and KAI−43140 are to be manufactured with the same cover glass.

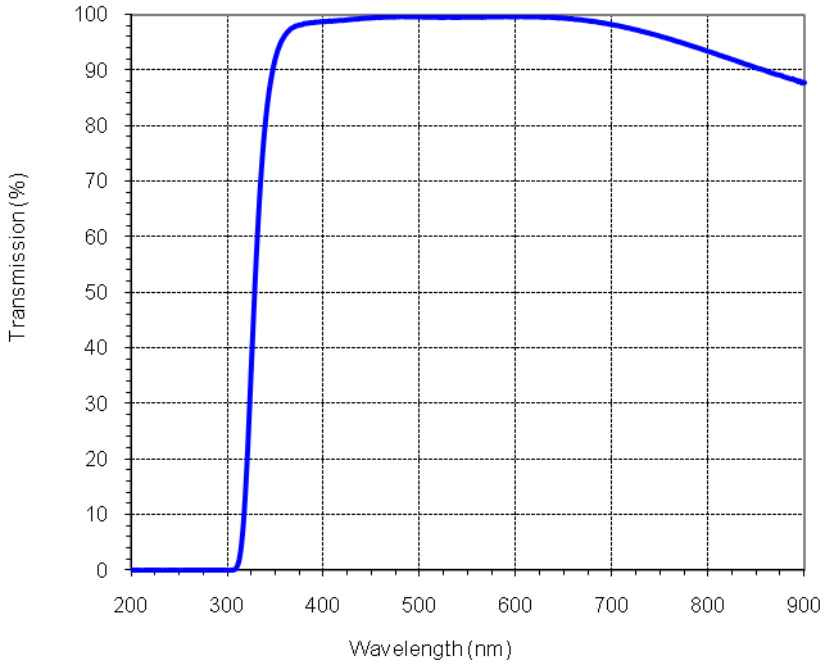


Figure 9. Cover Glass Transmission

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