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External Reset Signal for AX8052F1xx, AX-SFxx-1-xx, AX-SFxx-API-1-xx, AX-SIP-SFxx-1-xx and AX-SIP-SFxx-API-1-xx

APPLICATION NOTE

Introduction

This application note discusses the external reset signal sequence for AX8052F1xx, AX-SFxx-1-xx, AX-SFxx-API-1-xx, AX-SIP-SFxx-1-xx and AX-SIP-SFxx-API-1-xx families. Those families contains a Power-on Reset (POR) circuit which resets the chip when power up. The following sections will describe the suggested external reset signals applying to the RESET_N in case if external reset is needed.

Suggested External Reset Sequence

The followings show the suggested external reset sequences which should apply to the RESET_N pin of the AX8052F1xx, AX-SFxx-1-xx, AX-SFxx-API-1-xx, AX-SIP-SFxx-1-xx and AX-SIP-SFxx-API-1-xx families.

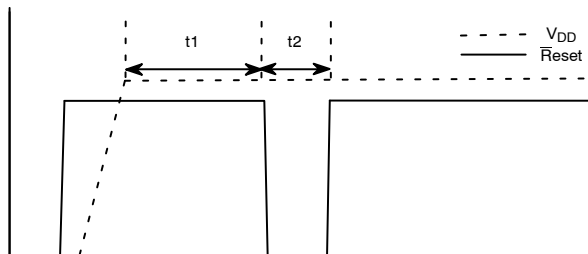


Figure 1. A – Suggested External Reset Signal

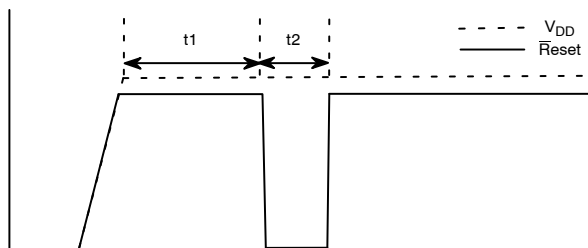


Figure 2. B – Suggested External Reset Signal

Two suggested external reset signal sequences have been shown in Figure 1 and Figure 2. For Figure 1, an external reset signal with logic high has been first applied prior to V_{DD}. For Figure 2, the external reset signal follows the V_{DD} and this can be implemented by using an open drain GPIO which tied an external pull-up resistor to V_{DD}.

After V_{DD} has been applied to the chip, the internal POR circuit needs time to finish the power on reset process. We suggested that the external reset signal should be applied after the POR have been finished. The suggested time for t1 should be larger or equal to 600 μs.

Once logic level low is applied to the RESET_N pins, reset will be performed and it takes some time for reset. The suggested time t2 should be larger or equal to the 1 μs.


Table 1 summarized the timing requirement for the suggested external signal:

Table 1. SUGGESTED TIMING

	Suggested Minimum Requirement
t1	600 μs
t2	1 μs

Conclusion

The built-in POR of the AX8052F1xx, AX-SFxx-1-xx, AX-SFxx-API-1-xx, AX-SIP-SFxx-1-xx and AX-SIP-SFxx-API-1-xx families should normally be enough for most of the application. This application note provided a suggested reset sequence in case if external reset is needed.

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