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Building Arrays of ON Semiconductor SiPM Sensors

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APPLICATION NOTE

INTRODUCTION

This document focusses on the creation of close-packed arrays of SiPM sensors. It gives both general advice and describes the design and test of a 12×12 (144) pixel array using 3 mm surface mount SiPM sensors. Primarily, the design was carried out to investigate the achievable pixel pitch and planarity when producing arrays using these devices. To evaluate the functionality of the array, it was decided to design the board to have the necessary output to be compatible with the Matrix readout system which allowed for performance testing of the array. Although the work here uses the MLP type of surface mount sensor package, all of the information applies equally to the creation of arrays using ON Semiconductor TSV packaged parts.

ON SEMICONDUCTOR SiPM SURFACE MOUNT PACKAGES

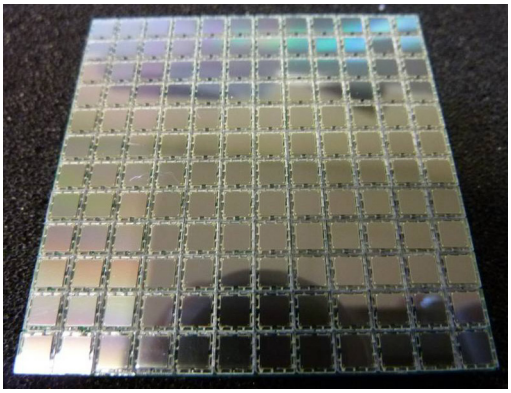
This document contains information necessary for the user to create close-packed, 1D or 2D arrays of ON Semiconductor SiPM sensors; either the micro leadframe package (MLP) or through-silicon via (TSV) parts. The MLP products have a part number with the suffix "−SMT" or "−MLP", whereas the TSV packaged products are denoted by "−TSV". Figure 1 shows examples of each package type.

ARRAY BUILD CONSIDERATIONS

The following key parameters should be taken into account when assembling the MLP or TSV packaged sensors into an array, to ensure the best quality.

- Sensor Storage
- Sensor Handling
- Solder Reflow Conditions
- Board Material
- Minimum Component Spacing
- Planarity

These factors are addressed individually below.



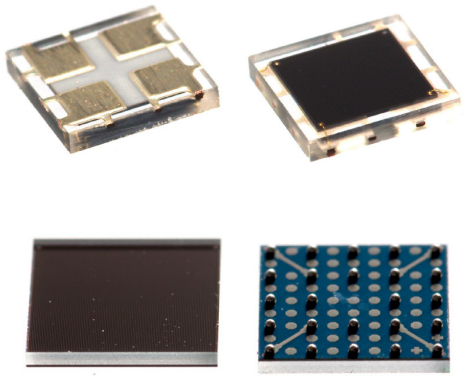


Figure 1. MLP Parts (Top) and TSV Parts (Bottom)

Sensor Storage

Both the MLP and TSV packaged surface mount sensors are moisture sensitive. Moisture can diffuse into the package from atmospheric humidity. Surface mount soldering of the packages to PCBs exposes the entire package body to temperatures of up to 260°C. Rapid expansion of trapped moisture during this process can result in package cracking, delamination of critical interfaces within the package or damaged bond wires. Therefore it is critical that sensors are stored carefully, with attention to the device moisture sensitivity level (MSL) and the packing date and storage conditions on the of the moisture barrier bag (MBB) that the parts are shipped in. The MSL levels and schematics of the MBB can be found in the Handling and Soldering application note for either the MLP or the TSV:

- TSV Handling and Soldering Guide
- MLP Handling and Soldering Guide

The information in the following documents should also be consulted.

- IPC/JEDEC J−STD−020
- IPC/JEDEC J−STD−033

Sensor Handling

The user should be aware of the fact that the SiPM is a sensitive optoelectronic instrument and should always be handled as carefully as possible. Physical contact with the sensor should be minimized during assembly and in particular, care should be taken to avoid contact with abrasive materials.

There are three points in the manufacture process where the user should be aware of the potential for damage:

- *Pick and Place* − automatic assembly directly from reels is recommended.
- *Singulation of the Array from the PCB after Reflow* − we recommend the use of a V-groove on the singulation tab to minimise the mechanical shock to the sensors.
- *Packing of the Arrays for Fransport* − Manual handling of the arrays should be minimized. Arrays should not be stacked, but should be packed in a way that avoids contact between the parts during transport.

Further information on the handling of the MLP and TSV packaged sensors, including cleaning, is given in the Handling and Soldering application notes:

- TSV Handling and Soldering Guide
- MLP Handling and Soldering Guide

Solder Reflow Conditions

MLP and TSV products must be mounted according to specified soldering pad patterns. Recommended solder footprints and pin-outs for each product are available in the CAD files, which are linked to in the product datasheets, e.g.:

- C-Series MLP datasheet
- J-Series TSV datasheet

Full reflow soldering information is given in the Handling and Soldering application notes:

- TSV Handling and Soldering Guide
- MLP Handling and Soldering Guide

In addition, solder reflow conditions must be in compliance with J−STD−20, Table 5.2. This is summarized in Figure 2. The number of passes should not be more than 2.

Recommended solder pastes are Multicore WS300 or Qualitek DSP 875 Type 5, which have been shown to avoid any potential voiding issues, as described further in the Solder Paste section.

Board Material

There are no requirements for a particular board material. ON Semiconductor use standard 1.6 mm FR4 PCB.

Minimum Component Spacing

The MLP package has a tolerance of +0.05 mm/−0.1 mm, and the TSV package as a tolerance of ±0.05 mm. Therefore, if the parts are placed with 0.1 mm spacing there could be extreme cases where the components are touching. Figure 3 shows how the package tolerance results in a variable gap between the sensor components. Therefore, to ensure that there is always a minimum spacing of 0.1 mm, a component spacing of 0.2 mm is recommended.

Based on a spacing of 0.2 mm the active areas of a 3 mm MLP packaged sensor will be 1.2 mm apart. This gives an array fill factor (for a 3 mm part) of:

$$\frac{(3.0)^2}{(4.2)^2} = 51\% \qquad \text{(eq. 1)}$$

For a 3 mm TSV packaged part using a 0.2 mm spacing, the active areas will be 0.29 mm apart and the fill factor is:

$$\frac{(3.07)^2}{(3.36)^2} = 84\% \qquad \text{(eq. 2)}$$

NOTE: The minimum spacing of 0.2 mm is too small to allow re-work. Should the user wish to design an array that can be reworked, then a minimum of 0.5 mm spacing is recommended.

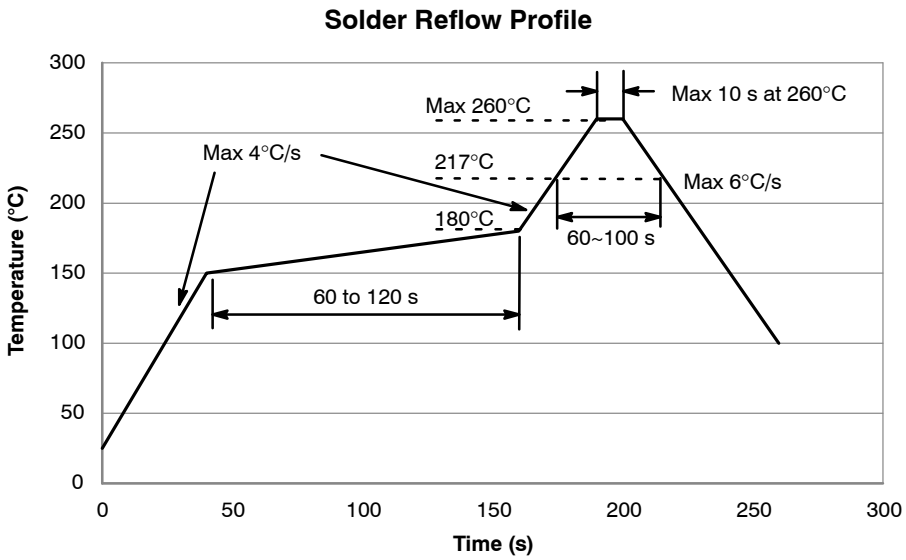


Figure 2. Solder Reflow Profile for the MLP and the TSV Packaged Parts

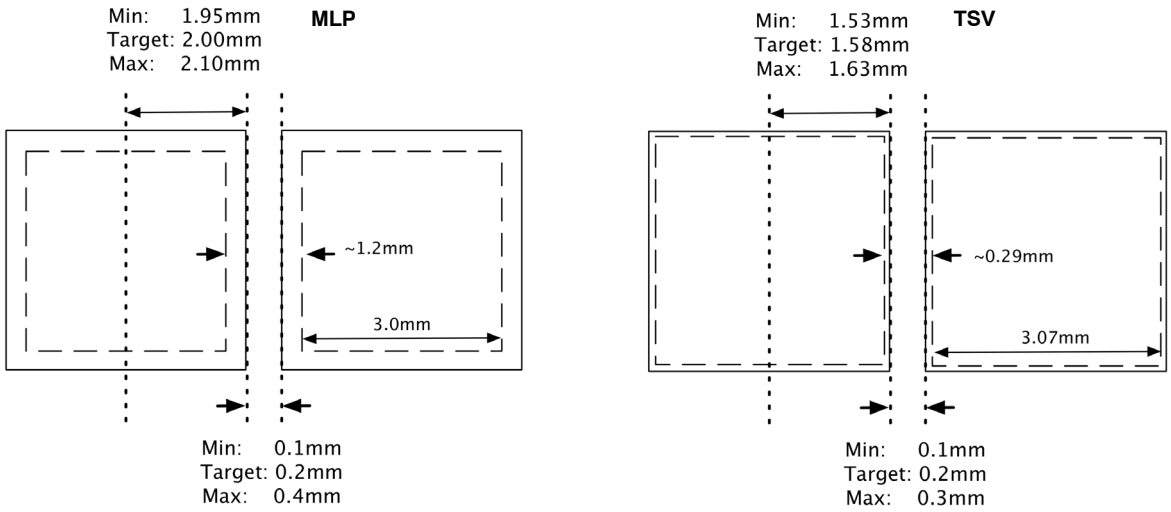


Figure 3. Using a Target Component Spacing of 0.2 mm will Result in a Range of Component Spacings that Depend on the Tolerance of the Package Size. This is Illustrated above for the MLP (Left) and the TSV (Right)

Planarity

It is useful to know the flatness, or planarity, of the assembled sensor array, and can be used to assess the quality of array manufacture. To achieve the best planarity it has been found to be beneficial to hold the PCB in a rigid frame to avoid any warping due to the heat process.

The planarity is measured as the deviation from 2 diagonal points as a percentage of the diagonal measurement. For example, if two corners of a 30 mm × 40 mm board deviate by 0.2 mm then the planarity is:

$$\frac{0.2}{50} = 0.4\% \quad \text{(Diagonal of board is 50 mm)} \qquad \text{(eq. 3)}$$

Ideally, planarity should be < 0.5%.

ON SEMICONDUCTOR MLP ARRAY BUILD CASE STUDY

Electronics Design

A test array was created using ON Semiconductor MLP packaged sensor parts. The array layout was designed to be compatible with the SensL® Matrix System, that was used for evaluation of the constructed array.

Figure 4 shows one of 9 blocks designed to replicate the function of the 4×4 array used on the Matrix system detector head, with each element representing, in this case, a MicroFM−30035−SMT sensor. The 16 cathodes (N) of each 4×4 block of devices are connected together to create the 9 ARRAY signal lines. The corresponding anode (P) outputs of each 4×4 block of devices are connected together to create 16 PIXEL signal lines. The positive bias is applied to the ARRAY side of the device.

However, with alternative readout electronics, other routing of the signals is possible.

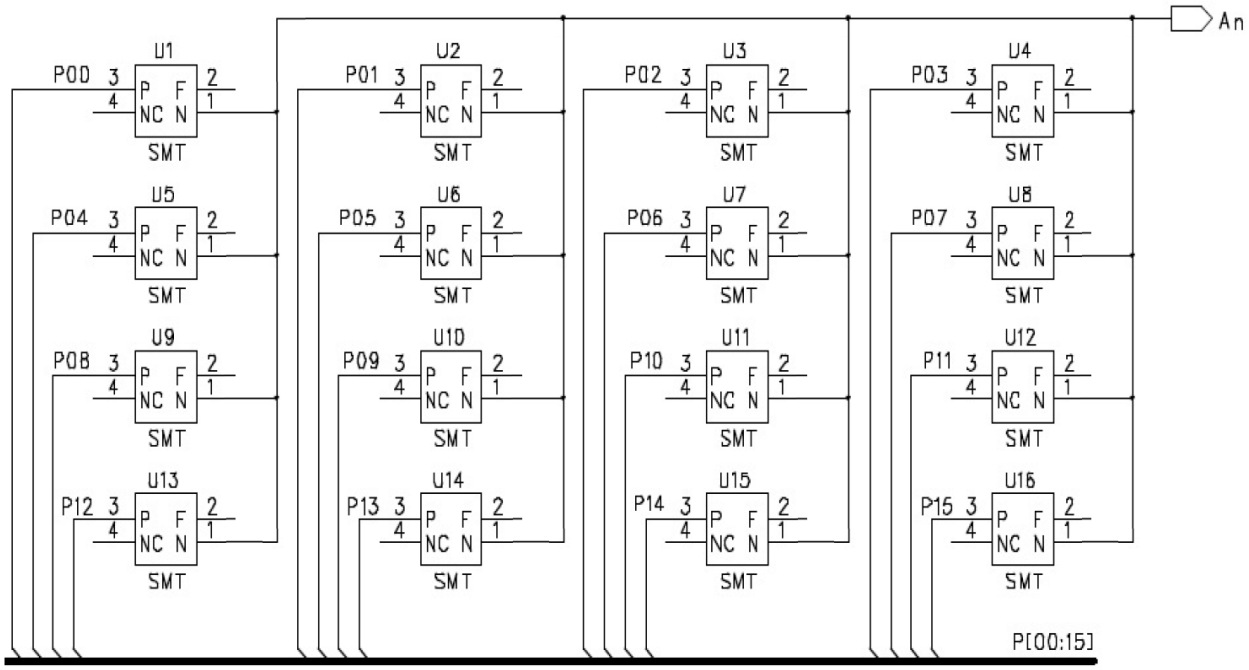


Figure 4.

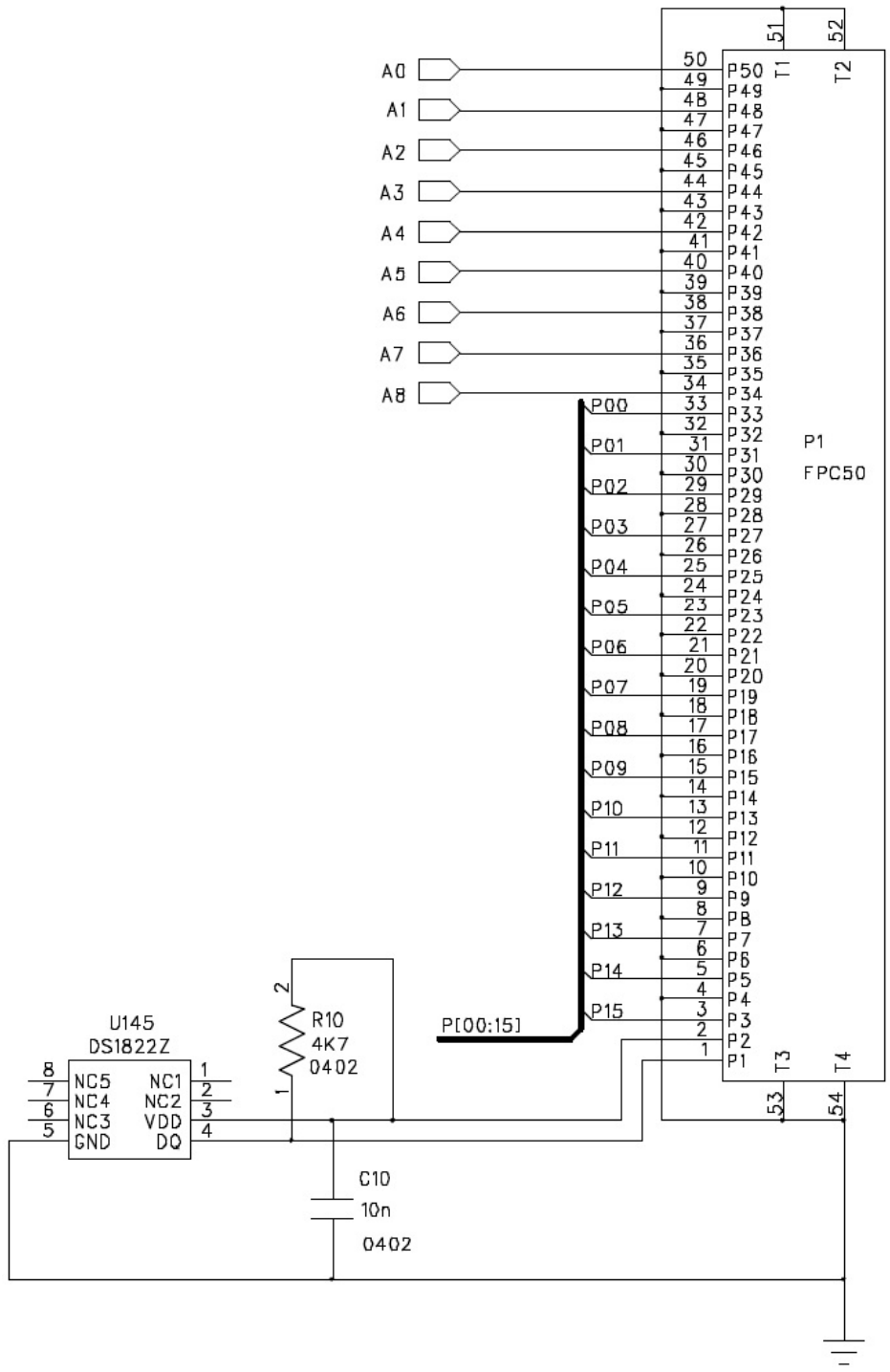


Figure 5.

Figure 5 shows the ribbon cable connector and thermometer IC. This is identical to the circuit used for the Matrix System and hence the board is electrically identical to that of the Matrix System detector head.

Manufacturing the Test Array

Figure 6 shows the engineering CAD of the MicroFM−30035−SMT devices which was used for the test array. The MLP package is nominally a 4 mm × 4 mm square housing the SiPM die of 3.16 mm × 3.16 mm.

The manufacturing challenge for this project was two-fold:

1. MLP Device Spacing – manufacture a board with the devices as close as possible to ensure the best possible fill factor.
2. Planarity – manufacture the board with the best planarity possible.

Common practice is to ground any floating pins such as the NC pin (#4). Grounding the pin helps shielding and keeps noise interference from external sources (EMI/RF) down but it may also be left floating without issue. In the production of the PCBs discussed in this document, the NC pin was grounded.

In addition, it was ensured that the assembly of the array board took into account the MSL specifications of the devices.

The solder footprint shown in Figure 7 has been shown to work well for the 3 mm MLP parts (e.g. MicroFM−30035−SMT) and was used for the test array. It consists of four square 1.4 mm × 1.4 mm pads arranged in a square with a pitch of 1.8 mm between pad centres (0.4 mm gap between pads). In general, links to the solder footprint for a given part can be found in the relevant product datasheet.

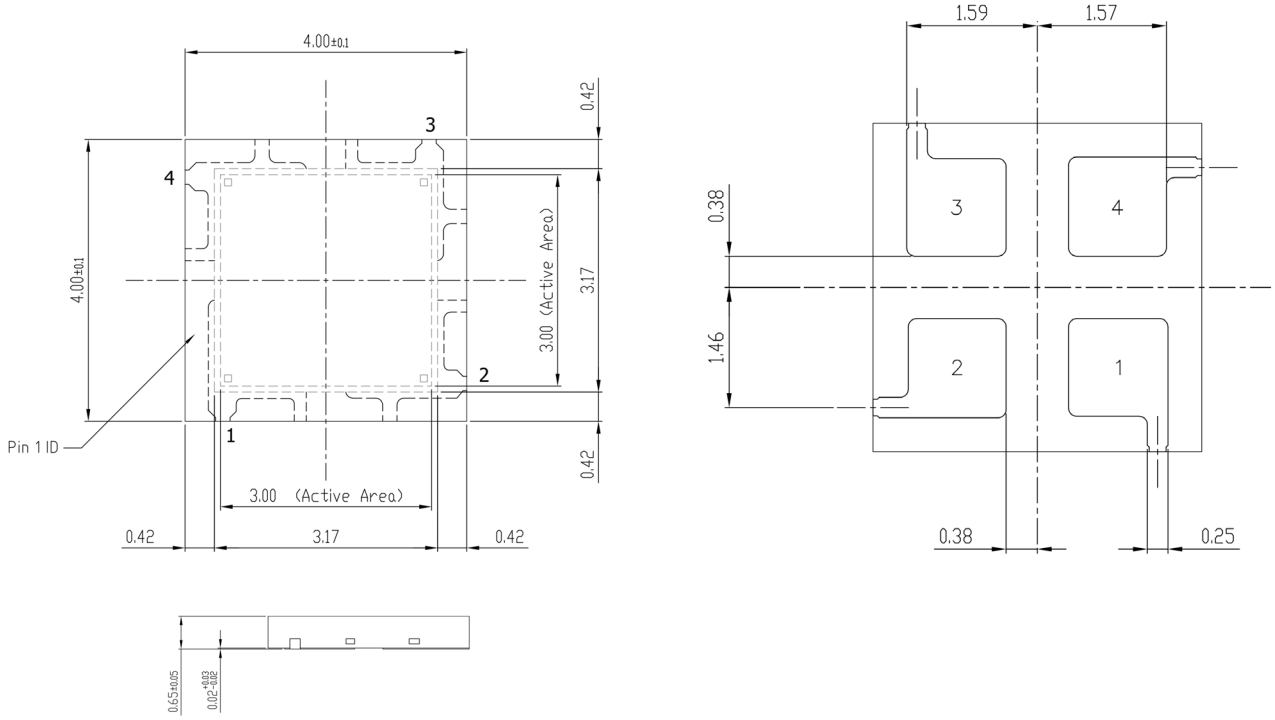


Figure 6. CAD of the MicroFM−30035−SMT Sensor Used in the Test Array

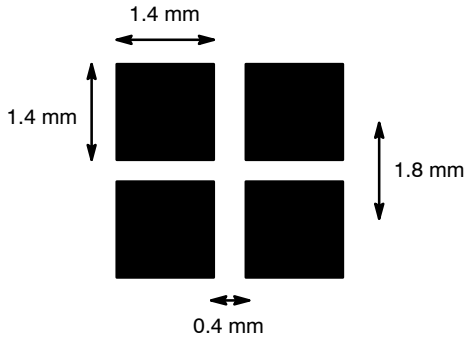


Figure 7. Solder Footprint used for the MicroFM−30035−SMT Sensor used in the Test Array

MLP Device Spacing

This MLP package has a tolerance of ±0.05 mm. Therefore, a component spacing of 0.2 mm was chosen. More details about minimum component spacing can be found in the Minimum Component Spacing section.

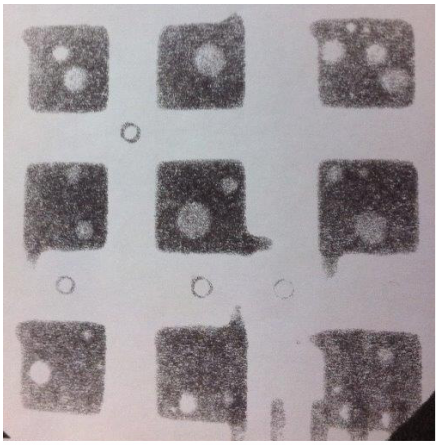
Solder Paste

To avoid significant voiding under the MLP pads it was found to be important to use the correct type of solder paste.

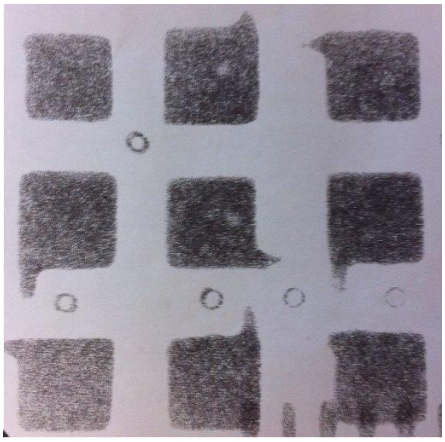
It was found that using a standard solder paste, such as the Qualitek DSP 875 Type3, resulted in significant solder voids formed under the MLP pads. This problem was resolved by using either of the following solder pastes:

- Multicore WS300 solder paste
- Qualitek DSP 875 Type 5

Figure 8 shows how voiding is significantly reduced by using the Qualitek DSP 875 Type 5 solder paste rather than the more standard Type 3 paste.



Qualitek DSP 875 Type 3



Qualitek DSP 875 Type 5

Figure 8.

Planarity

The vendor used for the array assembly believed that a 1.6 mm, 6-layer FR4 PCB would be acceptable providing good care was taken during the manufacturing process.

The planarity of the resulting array was found to be very much dependent on the process of soldering the devices to the board. It was observed by the vendor that during the re-flow process it was important to hold the boards in a rigid frame to avoid any warping due to the heat process. By designing a specific frame to hold the boards, less than 220 μm warping diagonally from corner to corner was achieved with relative ease.

As the diagonal measurement of the board is 71 mm (see Figure 9) this gives a planarity measurement of:

$$\frac{0.22}{71} = 0.3\% \qquad \text{(eq. 4)}$$

This value is considered to be a good value for the planarity.

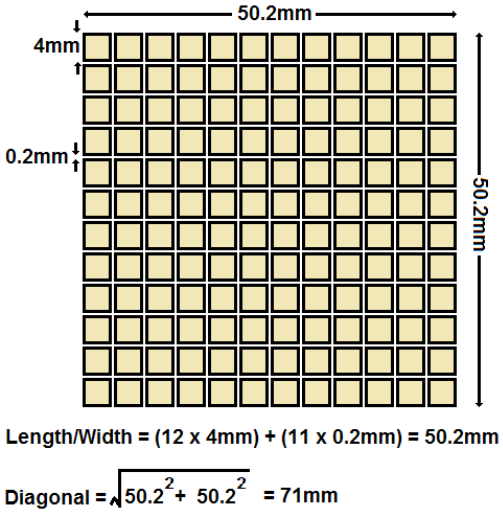


Figure 9.

Detailed Planarity Measurements

Prototype boards were manufactured, as shown in Figure 10 (sensor side) and Figure 11 (rear connector side).

To fully test the planarity, one of the samples was analyzed using a non-contact optical instrument specifically designed for this type of measurement.

The machine first takes the position of each corner of the board and from 2 diagonal lines it calculates the ideal plane.

The position of the surface of each sensor pixel is then measured and compared with the ideal plane. An example result from one of the prototype arrays is shown in Figure 12. It displays a value that tells you how close (+ or −) the device is from the ideal plane for each pixel.

For example:
Pixel 111 is +0.005 mm (5 μm above the ideal plane)
Pixel 80 is −0.013 mm (13 μm below the ideal plane)
Blue = +ve = ABOVE
Green = −ve = BELOW

The graph in Figure 13 shows the 144 values placed in 10 μm bins from −100 μm to +100 μm.

The results shows the range is −80 μm to +60 μm = 140 μm.

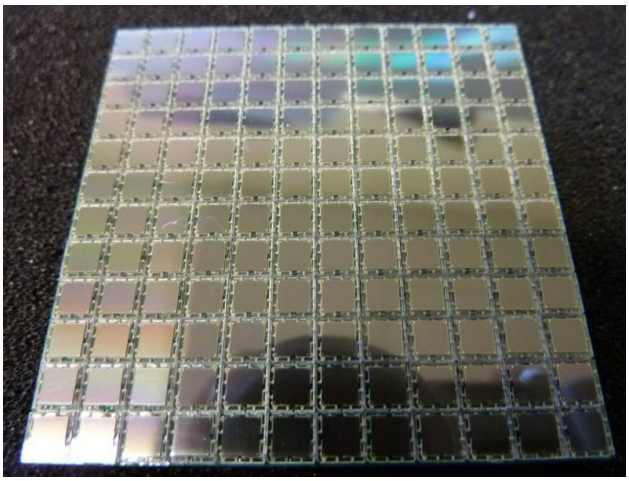


Figure 10.

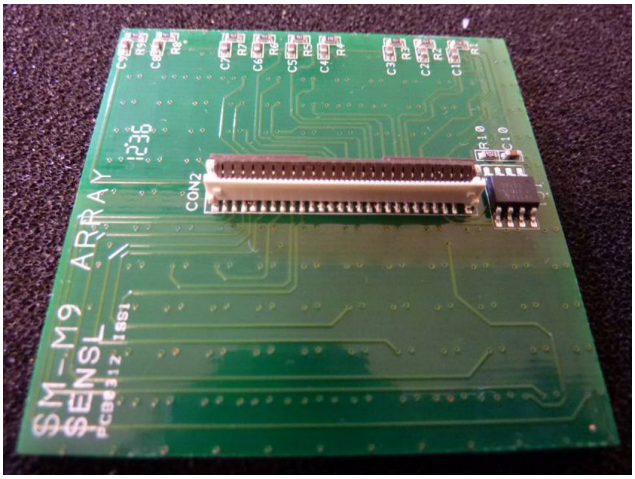


Figure 11.

133	134	135	136	137	138	139	140	141	142	143	144
+0.031	+0.004	+0.001	+0.011	−0.012	−0.001	−0.019	−0.018	+0.014	−0.005	−0.019	+0.014
121	122	123	124	125	126	127	128	129	130	131	132
+0.028	+0.029	+0.003	+0.001	+0.007	−0.017	−0.022	+0.020	+0.003	−0.006	+0.019	+0.023
109	110	111	112	113	114	115	116	117	118	119	120
+0.027	+0.019	+0.005	+0.000	−0.009	−0.016	+0.045	−0.014	−0.003	−0.006	+0.024	+0.032
97	98	99	100	101	102	103	104	105	106	107	108
+0.030	+0.020	+0.001	−0.006	−0.009	+0.034	−0.017	−0.017	+0.007	+0.013	+0.036	+0.037
85	86	87	88	89	90	91	92	93	94	95	96
+0.030	+0.013	+0.001	−0.009	+0.052	−0.009	−0.009	−0.014	+0.015	+0.016	+0.034	+0.041
73	74	75	76	77	78	79	80	81	82	83	84
+0.033	+0.015	−0.002	+0.051	+0.003	−0.009	−0.016	−0.013	+0.014	+0.036	+0.031	+0.032
61	62	63	64	65	66	67	68	69	70	71	72
+0.021	+0.005	+0.040	−0.005	−0.012	−0.012	−0.013	−0.006	+0.026	+0.029	+0.005	+0.033
49	50	51	52	53	54	55	56	57	58	59	60
+0.009	+0.049	+0.008	−0.007	−0.013	−0.012	−0.015	−0.01	+0.013	+0.042	+0.026	+0.023
37	38	39	40	41	42	43	44	45	46	47	48
+0.029	−0.001	−0.011	−0.015	−0.026	−0.032	−0.025	−0.016	+0.002	+0.036	+0.021	+0.018
25	26	27	28	29	30	31	32	33	34	35	36
−0.013	−0.011	−0.029	−0.034	−0.041	−0.033	−0.039	−0.027	−0.001	+0.011	+0.028	+0.004
13	14	15	16	17	18	19	20	21	22	23	24
−0.035	−0.038	−0.047	−0.047	−0.058	−0.057	−0.052	−0.044	−0.011	+0.008	+0.023	+0.035
1	2	3	4	5	6	7	8	9	10	11	12
−0.017	−0.021	−0.013	−0.04	−0.072	−0.077	−0.076	−0.072	−0.059	−0.029	−0.006	+0.004

Figure 12.

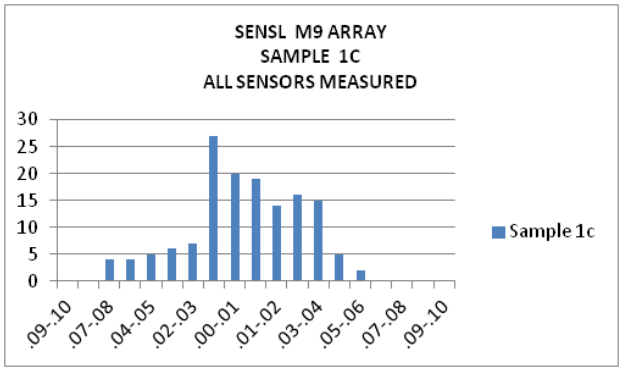


Figure 13.

Array Testing

To test the MLP test array, the board was connected to a Matrix System and then on to a PC hosting the Matrix System GUI software.

Basic Pixel Functionality Test

The initial test was carried out to prove that each SiPM pixel in the fabricated array functioned correctly. This was carried out using a $3 \times 3 \times 15$ mm^3 LYSO scintillating crystal and the SensL Matrix system software GUI. The crystal was moved from pixel to pixel. Each time, the GUI was used to verify that the particular pixel was detecting the intrinsic radioactivity from the Lutetium in the LYSO crystal. All pixels were found to be functional.

Cesium−137 Source Energy Resolution Measurement

Using a Cs−137 radioactive source (that produces gamma rays of 662 keV) and a $3 \times 3 \times 15$ mm^3 LYSO crystal, energy resolution measurements were carried out on 9 different pixels. Figure 14 shows a typical energy spectrum using the Matrix System GUI. It was found that, for all pixels, an energy resolution of < 12.5% was measurable.

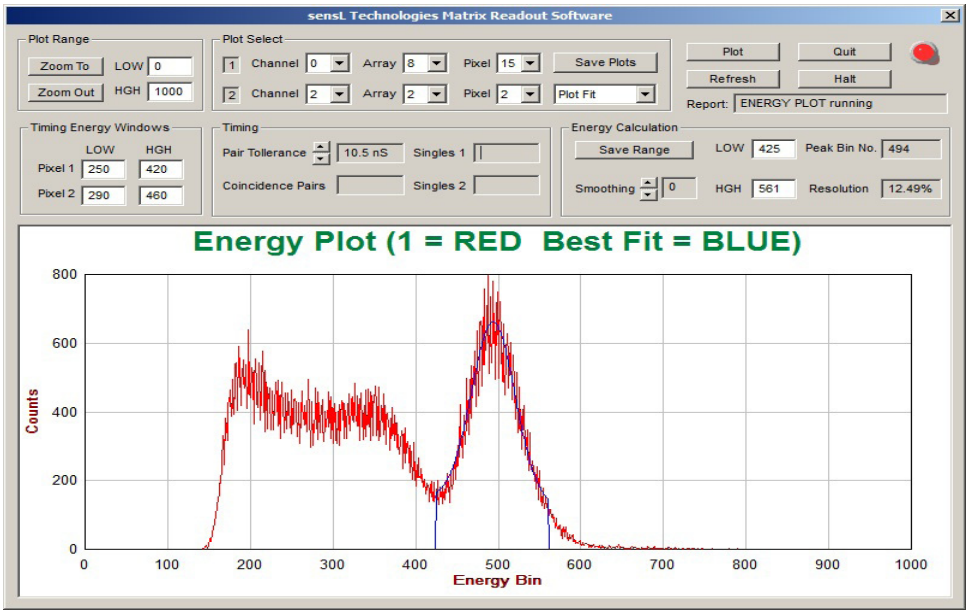


Figure 14.

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