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Designing A Compact, High-Efficiency PFC Stage Using The NCL2801

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APPLICATION NOTE

This paper describes the key steps to rapidly design a Discontinuous Conduction Mode PFC stage driven by the NCL2801. The process is illustrated in a practical 200−W, universal mains application:

- Maximum Output Power: 200 W
- Rms Line Voltage Range: from 90 V to 305 V
- Regulation Output Voltage: 450 V
- Frequency Fold−back at Reduced Load

INTRODUCTION

Housed in a SO−8 package, the NCL2801 is designed to optimize the efficiency of your PFC stage throughout the load range. Incorporating protection features for robust operation, it is ideal in systems where cost−effectiveness, reliability, low stand−by power and high efficiency are key requirements:

Valley Count Frequency Fold−back (VCFF): The circuit operates in Critical conduction Mode (CrM) when the VCTRL pin voltage is above a threshold level. When the VCTRL pin voltage goes lower than this threshold, the controller enters a Discontinuous Conduction Mode and starts adding dead−time (power MOSFET drain voltage valley counting to add dead time) after the inductor demagnetization phase. The lower the VCTRL pin voltage, the higher the value (number of valleys counted) of the dead time added. As a result, when VCTRL pin voltage decreases, due to lower output power demand, the switching frequency decreases down to a minimum of about 27.4 kHz, to avoid entering the audible frequency range.

Low Start−up Current and large V_{CC} range: The extra low start−up consumption of the NCL2801−[*A*]&[*B*] versions allows the use of high−value resistors for charging the V_{CC} capacitor. The NCL2801−[*C*], [*D*], [*E*] & [*F*] versions are targeted in applications where the circuit is fed by an auxiliary power source. The NCL2801−[*E*]&[*F*] versions have a start−up level lower than 11.25 V, allowing the circuit to be powering from a 12−V rail. NCL2801−[*C*] & [*D*] versions have a V_{CC} operating range (10 V to 27 V). NCL2801 − [*A*] & [*B*] & [*E*] & [*F*] versions have a V_{CC} operating range (9 V to 27 V).

Fast Line / Load Transient Compensation (Dynamic Response Enhancer and Soft OVP): Due to the slow loop response of traditional PFC stages, abrupt changes in the load or in the input voltage may cause significant over or under−shoots. This proprietary circuit drastically limits these possible deviations from the regulation point.

Safety Protections: NCL2801 features make the PFC stage extremely robust. Among them, we can mention the Brown−Out Detection block (on versions making it available) that stops operation when the ac line is too low and the 2−level Current Sensing, that forces a low duty−ratio operation mode in the event that the inductor current exceeds 150% of the current limit. This situation can be caused by inductor saturation or by the bypass or boost diode short circuit.

Eased Manufacturing and Safety Testing: Some elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive mechanical stress or other troubles. In particular, some adjacent pins can be shorted, a single pin can be grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke or hazardous conditions. The NCL2801 integrates enhanced functions that help address these requirements, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode. Application note AND9079 details the behavior of a similar NCP1612−driven PFC stage under safety tests [1].

PFC Stage Dimensions

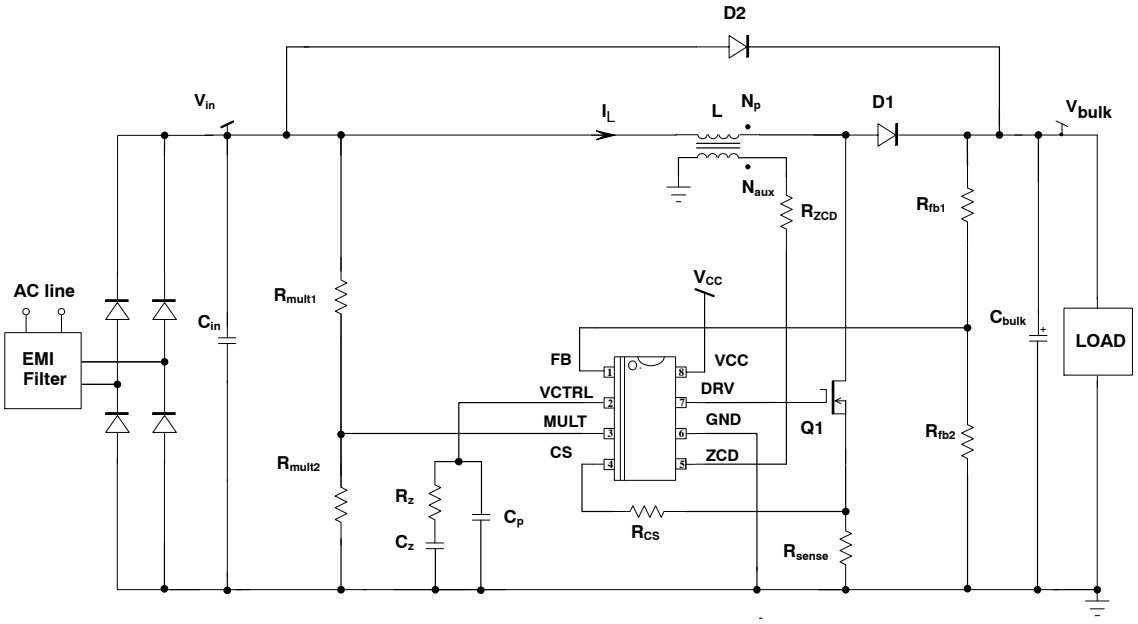


Figure 1. Evaluation Board Schematic with Power and Control Circuitry

Step 1: Define the key specifications

- f_{line} : Line frequency. 50 Hz /60 Hz applications are targeted. Practically, they are often specified in a range of 47−63 Hz and for calculations such as hold−up time, one has to factor in the lowest specified value.
- $V_{line,rms,min}$:Lowest level of the line voltage. This is the minimum rms input voltage for which the PFC stage must operate. Such a level is usually 10−12% below the minimum typical voltage which could be 100 V in many countries. We will take $V_{line,rms,min}$ = 90 V
- $V_{line,rms,max}$: Highest level for the line voltage. This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries), but for some lighting application it must go as high as 305 V We select $V_{line,rms,max}$ = 305 V
- High Line $V_{line,rms,HL}$ and Low Line $V_{line,rms,LL}$ thresholds for internal line feedforward. Operating line voltage must be well above Line $V_{line,rms,HL}$ or well below $V_{line,rms,LL}$. These thresholds values cannot be changed because V_{HL} et V_{LL} internal reference voltage are fixed, and they must not be changed by changing K_m value $K_m = \frac{R_{mult2}}{R_{mult1} + R_{mult2}}$ because K_m value also controls current control level and a good starting design value is K_m=6.622m.

$$(V_{line,rms})_{LL} = \frac{V_{LL}}{K_m\sqrt{2}} = \frac{1.422}{0.006622\sqrt{2}} = 151.8V_{rms} \quad \text{(eq. 1)}$$

$$(V_{line,rms})_{HL} = \frac{V_{HL}}{K_m\sqrt{2}} = \frac{1.625}{0.006622\sqrt{2}} = 173.5V_{rms} \quad \text{(eq. 2)}$$

- :$(V_{line,\,rms})_{boH}$ Brown−out line upper threshold (In case the controller is using an option featuring the brown−out protection. For controller option not featuring the brown−out protection, the following lines don't apply). The circuit prevents operation until the line rms voltage exceeds $(V_{line,\,rms})_{boH}$. The NCL2801 offers a 10% hysteresis. Hence, if no specific action is taken, it will detect a brown−out situation and stop operation when the rms line voltage goes below $(V_{line,\,rms})_{boL}$ that equates (90% $(V_{line,\,rms})_{boH}$. A brown−out event is sensed through the MULT pin and the parameter Km, $K_m = \frac{R_{mult2}}{R_{mult1} + R_{mult2}} = 0.006622$. Internal brown−out fixed value reference voltages V_{BOH} = 787 mV and V_{BOL} = 709 mV are used for calculating the line brown−out thresholds :

$$(V_{line,rms})_{boH} = \frac{V_{BOH}}{K_m\sqrt{2}} = \frac{0.787}{0.006622\sqrt{2}} = 84Vrms \quad \text{(eq. 3)}$$

$$(V_{line,rms})_{boL} = \frac{V_{BOL}}{K_m\sqrt{2}} = \frac{0.709}{0.006622\sqrt{2}} = 75.7rms \quad \text{(eq. 4)}$$

NOTE: Line brown−out thresholds cannot be modified using K_m because K_m also controls the peak inductor current (Current Control Mode)

- $V_{out,nom}$: Nominal output voltage. This is the regulation level for the PFC output voltage (also

designated as the bulk voltage). $V_{out,nom}$ must be higher than $\left(\sqrt{2} \cdot \left(V_{line,rms}\right)_{HL}\right) = \sqrt{2} \cdot 305 = 431V$

450 V is our target value.

- $(\delta V_{out})_{pk-pk}$: Peak−to−peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the Dynamic Response Enhancer (DRE) in normal operation.
- P_{out}: Output power. This is the power consumed by the PFC load.
- $P_{out,max}$: Maximum output power. This is the maximum output power level which is 200 W in our application.
- $(P_{in,avg})_{max}$: Maximum input power. This is the maximum power that can be absorbed from the mains in normal operation. This level is obtained at full load, low line. Assuming an efficiency of 95% in these conditions, we will use: $\left(P_{in,avg}\right)_{max} = \frac{200}{95\%} \cong 210W$
- $I_{line,max}$: Maximum line current obtained at full load, low line.
- $V_{ctrl,th,*}$: VCTRL pin voltage threshold below which the circuit reduces the frequency (VCFF). If the VCTRL pin voltage Vctrl is lower than Vctrl,th,*, the PFC stage will permanently operates with a reduced frequency. Conversely if Vctrl is higher than Vctrl,th,*, then the PFC stage will operate in CrM (no frequency fold−back).

Step 2: Power components selection

In heavy load conditions, the NCL2801 operates in **Cr**itical conduction **M**ode (CrM). Hence, the inductor, the bulk capacitor and the power silicon devices are dimensioned as usually done with any other CrM PFC. This chapter does not detail this process, but simply highlights key points.

1. Inductor Selection

The on−time of the circuit is internally limited. The power the PFC stage can deliver depends on the inductor since *L* will determine the current rise for a given on−time. More specifically, the following equation gives the power capability of the PFC stage:

$$\left(P_{in,avg}\right)_{HL} = \frac{V_{line,rms^2}}{2L} \cdot T_{on,max} \quad \text{(eq. 5)}$$

The smaller the inductor, the higher the PFC stage power capability. Hence, *L* must be low enough so that the full power can be provided at the lowest line level:

$$L \leq \frac{V^2_{line,rms_{LL}}}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max} \quad \text{(eq. 6)}$$

Like in traditional CrM applications, the following equations give the other parameters of importance:

Maximum peak current:

$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2}\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}} \quad \text{(eq. 7)}$$

Maximum rms current:

$$\left(I_{L,rms}\right)_{max} = \frac{\left(I_{L,pk}\right)_{max}}{\sqrt{6}} \quad \text{(eq. 8)}$$

In our application, the inductor must then meet the following requirements:

Note: $T_{ON,max}$ = 30 μs @V_{CTRL}=4.5 V

$$L \leq \frac{90^2}{2 \cdot 210} \cdot 30\mu = 578\mu H$$
$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{210}{90} \cong 6.6A \quad \text{(eq. 9)}$$
$$\left(I_{L,rms}\right)_{max} = \frac{6.6}{\sqrt{6}} \cong 2.7A$$

Any value of boost inductor lower than 578 uH will be able to transfer the maximum power, however we have to consider the switching frequency .

On the other hand, we need the switching frequency to be kept above the audible range at minimum line voltage. In CrM mode, at full load and minimum line voltage, the switching frequency at the top of the line sinusoid voltage, $F_{sw,min}$ can be easily written and associated L_{min} inductor value can be calculated as shown in the following formula:

$$L_{min} = \frac{1}{F_{SW,min} I_{pk,max} \cdot \left(\frac{1}{V_{bulk} - \sqrt{2} \cdot V_{mains,rms,min}} + \frac{1}{\sqrt{2} \cdot V_{mains,rms,min}} \right)} \quad \text{(eq. 10)}$$

Numerical calculation corresponding to the values previously used and using $F_{sw,min}$ = 77 kHz gives:

$$L_{min} = \frac{1}{77k \cdot 6.616 \cdot \left(\frac{1}{450 - \sqrt{2} \cdot 90} + \frac{1}{\sqrt{2} \cdot 90} \right)} = 179\mu H \quad \text{(eq. 11)}$$

In the 200 W Evaluation Board, we will use a Wurth Elektronik 180 mH inductor WE760806400

One can note that the switching frequency in CrM operation depends on the inductor value:

$$f_{SW} = \frac{V_{line}(t)^2 \cdot (V_{out} - V_{line}(t))}{4 \cdot P_{in,avg} \cdot V_{out} \cdot L} \quad \text{(eq. 12)}$$

For instance, at low line, full load (top of the sinusoid), the switching frequency is:

$$f_{SW} = \frac{(\sqrt{2} \cdot 90)^2 \cdot (450 - \sqrt{2} \cdot 90)}{4 \cdot 210 \cdot 450 \cdot 180 \cdot 10^{-6}} \cong 77kHz \quad \text{(eq. 13)}$$

NOTE: Note: While this equation is OK for the top of the sinusoid, the THD enhancement system which is increasing the on−time close to line voltage zero−crossing makes the switching frequency lower than which is predicted by Eq. 13.

2. Power silicon devices

Generally, the diode bridge and the power MOSFET are placed on the same heat−sink.

As a rule of the thumb, one can estimate that the heat−sink will have to dissipate around:

- 4% of the output power in wide mains applications (95% being generally the targeted minimum efficiency)
- 2% of the output power in single mains applications.

In our wide−mains application, about 8 W are then to be dissipated. We selected a standard Extruded Aluminum Profile from Heatsinkusa (1.813'' wide / 3.000'' long) whose thermal resistance is specified as 4.5°C/W.

Among the sources of losses that contribute to this heating, one can list:

- The diodes bridge conduction losses that can be estimated by the following equation:

$$P_{bridge} = 2 \cdot V_f \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta} \quad \text{(eq. 14)}$$

$$P_{bridge} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta} \approx \frac{1.8 \times 1}{90} \cdot \frac{200}{0.95} = 4.2W$$

where V_f is the forward voltage of the bridge diodes at the rated current.

- The MOSFET conduction losses are given by:

$$(p_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(15 \frac{P_{out,max}}{\eta \cdot (V_{line,rms})_{LL}} \right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}} \right) \quad \text{(eq. 15)}$$

$$(p_{on})_{max} = \frac{4}{3} \cdot \left(\frac{200}{0.95 \cdot 90} \right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 450} \right) \cdot R_{DS(on)} = 5.54 \cdot R_{DS(on)}$$

In our application, we have:

- P_{BRIDGE} = 4.2 W, assuming that V_f is 1 V.
- $(P_{on})_{max} = 5.54 \cdot R_{DS(on)}$.

  A low *RDS*(*on*) MOSFET (0.25 Ω@ 25 °C) is selected to avoid excessive conduction losses. Assuming that *RDS*(*on*) doubles at high temperature, the maximum conduction losses peak to about 2.77 W.

The total conduction losses for the MOSFET and the diode bridge can be as high as 6.97 W.

Switching losses cannot be easily computed. We will not attempt to predict them. Instead, as a rule of the thumb, we will assume a loss budget equal to that of the MOSFET conduction ones. Experimental tests will check that they are not under−estimated.

The boost diode is the source of the following conduction losses:$(I_{out} \cdot V_f)$, where I_{out} is the load current and V_f the diode forward voltage. The maximum output current being nearly 0.444 A, the diode conduction losses are in the range of 0.444 W (assuming V_f = 1 V). P_{DIODE} = 0.444 W

3. Output Bulk Capacitor

There generally are three main criteria / constraints when defining the bulk capacitor:

- Peak−to−peak low frequency ripple at $2f_{line}$ frequency:

$$(\delta V_{out})_{pk-pk} = \frac{P_{out,\,max}}{C_{bulk} \cdot 2\pi \cdot f_{line} \cdot V^2_{out,nom}} \quad \text{(eq. 16)}$$

This ripple must keep lower than +/−4% of the output voltage (8% peak−to−peak) in order to avoid triggering the Dynamic Response Enhancer (DRE) system while in steady state. Taking into account the minimum line frequency value

(47 Hz) which is the worst case for ripple amplitude, this leads to:

$$C_{bulk} \geq \frac{200}{8\% \cdot 2\pi \cdot 47 \cdot 450^2} \cong 42\mu F \quad \text{(eq. 17)}$$

For the 200 W Evaluation Board we have selected a 150 μF bulk capacitance which gives a 10 V (2.2%) peak−peak ripple voltage as shown by Eq. 18 equation here after.

$$(\delta V_{out})_{pk-pk} = \frac{200}{150\mu \cdot 2\pi \cdot 47 \cdot 450} = 10.0V \quad \text{(eq. 18)}$$

- Hold−up time specification:

$$C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^{\ 2} - V_{out,min}^{\ 2}} \quad \text{(eq. 19)}$$

Hence, a 10−ms hold−up time imposes:

$$C_{bulk} \geq \frac{2 \cdot 200 \cdot 10m}{450^2 - 400^2} \cong 94\mu F \quad \text{(eq. 20)}$$

We can see that the hold−up time is not a problem with the 150 μF bulk capacitance used in the 200 W Evaluation Board.

- RMS capacitor Current:

The rms current depends on the load characteristic. Assuming a resistive load, we can derive the following approximate expression of its magnitude[1]:

$$(I_{c,rms})_{max} \cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{(P_{out})_{max}/P_{eff}}{\sqrt{(V_{line,rms})_{LL} \cdot V_{out,nom}}}\right)^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2} \quad \text{(eq. 21)}$$

In our 200 W Evaluation Board, we have:

$$(I_{c,rms}) \cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{200/0.95}{\sqrt{85 \cdot 450}}\right)^2 - \left(\frac{200}{450}\right)^2} \simeq 1.29A \quad \text{(eq. 22)}$$

Step 3: Bulk Voltage Monitoring and Regulation Loop

As shown by Figure 1, the feedback arrangement consists of:

- A resistor divider that scales down the bulk voltage to provide pin FB with the feedback signal. The upper resistor of the divider generally consists of three or four series resistors for allowable voltage stress and safety considerations. Use typical power supply design guidelines when choosing resistors for high voltage applications.
- A filtering capacitor that is often placed between pin FB and ground to prevent switching noise from distorting the feedback signal. A 1−nF capacitor is often implemented. Generally speaking, the pole it forms with the feedback resistors must remain at a very high−frequency compared to the ac line frequency

$$C_{fb} \leq \frac{1}{150 \cdot (R_{fb1} \| R_{fb2}) \cdot f_{line}}$$

Practically, generally give good results.

- A type−2 compensation network. Consisting of two capacitors and of one resistor, this circuitry sets the crossover frequency and the loop characteristic.

In steady−state the feedback being in the range of the 2.5−V regulation reference voltage, the feedback bottom resistor (R_{fb2} of Figure 1) sets the bias current in the feedback resistors as follows:

$$I_{FB} = \frac{V_{REF}}{R_{fb2}} = \frac{2.5V}{R_{fb2}} \quad \text{(eq. 23)}$$

Trade−off between losses and noise immunity dictate the choice of this resistor. Resistors up to 56 kΩ ($I_{FB} \cong 50$ mA) generally give good results. Higher values can be considered if allowed by the PCB layout. Please note anyway that a 200−nA sink current (450 nA max. on the −40° to 125°C temperature range) is built−in to pull the feedback pin down and disable the driver if the pin is accidently open. If I_{FB} is set below 50 μA, the regulation level may be significantly impacted by the 200−nA sink current.

When the bottom resistor is selected, select the upper resistor as follows:

$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right) \quad \text{(eq. 24)}$$

In our application, we select a 22−kΩ value for R_{fb2}($I_{FB} \cong 114$ μA). As for R_{fb1}, two 1800−kΩ resistors are placed in series with a 330−kΩ one. These normalized values precisely give: (R_{fb1} = 3.93 MΩ), leading to a nominal 449−V regulation level, which is acceptable (0.2% under the 450 V target).

Compensating the loop:

Small signal wise, the regulation loop to be compensated is comprised of a Plant Transfer Function $T_{plant}(s)$ Eq. 25 which is physically placed between the VCTRL pin and the positive node of bulk capacitance,

$$T_{plant}(s) = \frac{V_{bulk}(s)}{V_{CTRL}(s)} \quad \text{(eq. 25)}$$

and of a Type II Compensator $T_{comp}(s)$ Eq.26 which is physically placed between the positive node of the bulk capacitor and the VCTRL pin.

$$T_{comp}(s) = \frac{V_{CTRL}(s)}{V_{bulk}(s)} \quad \text{(eq. 26)}$$

The Open Loop transfer function $T_{OL}(s)$ is the product of the Plant Transfer function by the Compensator transfer function.

$$T_{OL}(s) = T_{plant}(s) \cdot T_{comp}(s) \quad \text{(eq. 27)}$$

[1]It remains wise to verify the bulk capacitor heating on the bench!

The loop gain of a PFC boost converter is proportional to the square of the line magnitude if no feed−forward is applied. Hence, this gain almost varies by an order of magnitude in universal mains conditions. The NCL2801 senses the line voltage level value by the means of a resistor divider bridge connected between the rectified line voltage and the MULT pin. The NCL2801 uses this information to perform a 2−level feed−forward function: in high−line, which is detected when $V_{line,rms}$ happens to exceed $(V_{in,rms})_{HL}$, the internal multiplier gain is divided by 3.2 compared to a low−line state (which is set if $V_{line,rms}$ is less than $(V_{in,rms})_{HL}$ for 25 ms – see Figure 2). While we cover here the product option which detects the line level and adjust the multiplier gain, typically for wide mains application, there are options where there is no detection of line level and only one multiplier gain value is used. In this later case the compensation network values are calculated exactly the same way.

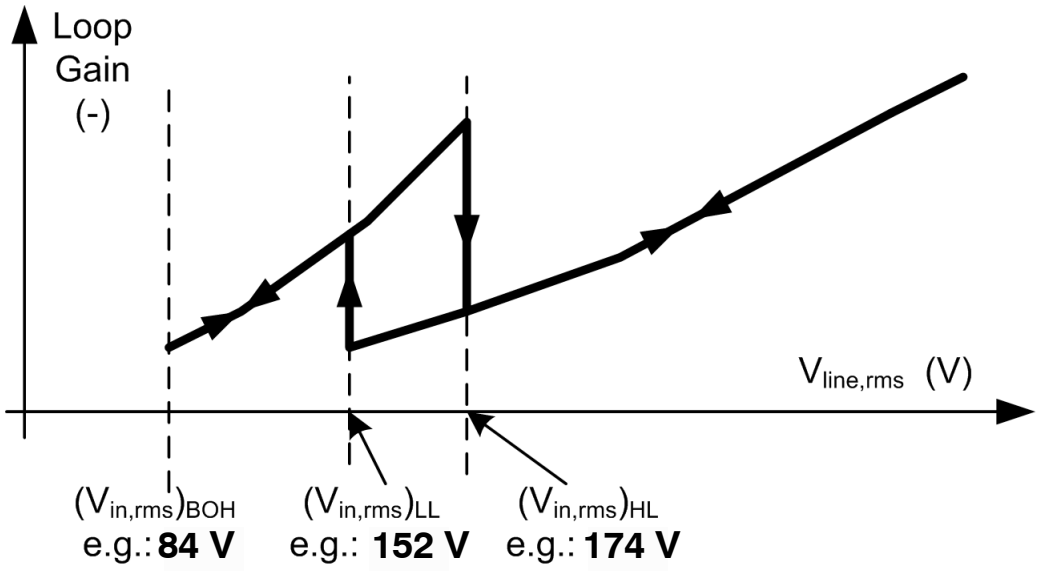


Figure 2. 2−Step Feed−Forward Limits the Loop Gain Variation With Respect to Line

Using small signal methods described in [1], [2] and [5], we can derive two small−signal Plant Transfer Functions of our PFC stage (one for High Line, one for Low Line) which differ only from the value of the multiplier gain which is different at High Line and Low Line:

- Low−Line small signal Plant transfer function

$$T_{plant,LL}(s) = \frac{v_{bulk}(s)}{v_{CTRL}(s)} = \frac{V_{line,rms}^{2} \cdot K_m \cdot K_{mult,LL}}{4 \cdot V_{bulk,nom}} \cdot \frac{V_{regul,range}}{V_{CTRL,range}} \cdot \frac{R_{load}}{R_{sense}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}} \quad \text{(eq. 28)}$$

- High−Line small signal Plant transfer function:

$$T_{plant,HL}(s) = \frac{v_{bulk}(s)}{v_{CTRL}(s)} = \frac{V_{line,rms}^{2} \cdot K_m \cdot K_{mult,HL}}{4 \cdot V_{bulk,nom}} \cdot \frac{V_{regul,range}}{V_{CTRL,range}} \cdot \frac{R_{load}}{R_{sense}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}} \quad \text{(eq. 29)}$$

Where:

- $V_{line,rms}$ is the Line root mean squared voltage
- K_m is the ratio between instantaneous MULT pin voltage and instantaneous Line rectified voltage (resistor divider plugged between mains rectified voltage and MULT pin).
- $K_{mult,\,LL}$ and $K_{mult,\,HL}$ are respectively the Low Line and High Line multiplier gains.
- $V_{bulk,nom}$ is the nominal regulation level of the PFC output (ripple voltage is not included here)
- $V_{CTRL,\,range}$ = 4 V and $V_{regul,\,range}$ = 1.5 V are internal controller parameters, and represent the operating range of VCTRL pin voltage and the operating range of an internal voltage correlated to VCTRL pin voltage.
- R_{load} is the load equivalent resistance which is defined by: $R_{load} = (V_{bulk})^2 / P_{out,max}$
- R_{sense} is the sense resistor placed between pin CS and GND for sensing the inductor current value during on−time.
- C_{bulk} is the bulk capacitor, also named output capacitor.

PFC stages regulation loop speed must be slow. More practically, high PF ratios require the low regulation

bandwidth to be in the range of 20 Hz or lower. Hence, sharp variations of the load result in excessive over and under−shoots. These deviations are effectively contained by the NCL2801 ***Dynamic Response Enhancer*** together with its accurate over−voltage protection.

The recommended compensator used in the regulation loop is a Type−II one Figure 3, which transfer function is given by Eq. 30:

$$T_{comp}(s) = \frac{v_{CTRL}(s)}{v_{bulk}(s)} = -\frac{R_{fb2}}{R_{fb1} + R_{fb2}} \cdot R_z G_m \cdot \frac{C_z}{C_z + C_p} \cdot \frac{1 + \frac{1}{R_z C_z} \cdot \frac{1}{s}}{1 + R_z \frac{C_p C_z}{C_z + C_p} \cdot s} \quad \text{(eq. 30)}$$

G_m is the 200−μS trans−conductance gain of the OTA shown in Figure 3.

The compensator transfer function can be simplified and written in the form of Eq. 31 if we assume that C_Z is much greater than C_p and taking into account that the positive input of the OTA is connected to an internal 2.5−V reference voltage.

$$T_{comp}(s) = \frac{v_{CTRL}(s)}{v_{bulk}(s)} = -\frac{2.5V}{V_{bulk,nom}} \cdot R_z G_m \cdot \frac{1 + \frac{1}{R_z C_z} \cdot s^{-1}}{1 + R_z C_p \cdot s} \quad \text{(eq. 31)}$$

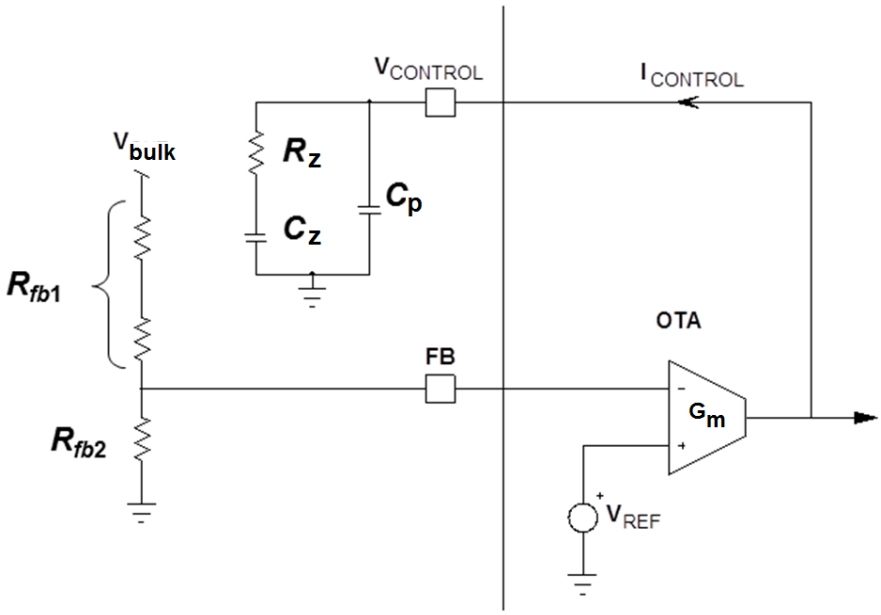


Figure 3. Regulation Trans−Conductance Error Amplifier, Feed−Back and Compensation Network

To calculate the values of the compensation components we'll use the K factor method used in [4]

We'll target an Open Loop cross−over frequency $f_{co,max}$ equal to 10 Hz ($f_{co,max}$=10 Hz) and an Open Loop Phase Margin of 60° (φ_m=60°) for when V_{mains} is at the maximum operating value (i.e. $V_{mains,max}$ = 305 Vrms).

The reason to have a target cross−over frequency and phase margin at the higher voltage of High Line is that at low line, the cross−over frequency will naturally shift to lower values to its dependency versus V_{mains} and the phase margin is getting better when the cross over frequency decreases.

Applying the compensation K factor method described in [4] we obtain the following design equations which are for max output Power.

G_0 is the static gain at the highest of the High Line voltage $V_{mains,max,HL}$

$$G_0 = \frac{\left(V_{mains,max,HL}\right)^2 K_m K_{mult,HL}}{4V_{bulk,nom}} \cdot \frac{V_{regul,range}}{V_{CTRL,range}} \cdot \frac{R_{load,min}}{R_{sense}} \quad \text{(eq. 32)}$$

Where $R_{load,min}$ is the equivalent load resistor at maximum output power

$$R_{load,min} = \frac{\left(V_{bulk,nom}\right)^2}{P_{out,max}} \quad \text{(eq. 33)}$$

$G_{plant,fco,max}$ is the plant Gain in dB at the open−loop cross−over frequency $f_{co,max}$

$$G_{plant,fco,max} = 20\log_{10}\left|\frac{G_0}{1 + i2\pi f_{co,max}C_{bulk}\frac{R_{load,min}}{2}}\right| \quad \text{(eq. 34)}$$

$\varphi_{plant,fco,max}$ is the Plant phase in degrees at the maximum open−loop cross−over frequency $f_{co,max}$

$$\varphi_{plant,fco,max} = Phase\left(\frac{G_0}{1 + i2\pi f_{co,max}C_{bulk}\frac{R_{load,min}}{2}}\right) \quad \text{(eq. 35)}$$

$$K_{factor} = \tan\left(\frac{\pi}{360}\cdot\left(\varphi_m - \varphi_{plant,fco,max}\right)\right) \quad \text{(eq. 36)}$$

R_z is the compensation resistor in series with C_z, both placed between VCTRL pin and GND

$$R_z = \frac{V_{bulk,nom}}{10^{\frac{G_{plant,fco,max}}{20}}\cdot G_m \cdot V_{ref}} \quad \text{(eq. 37)}$$

Gm is the OTA trans−conductance (typically 200 μS) and V_{ref} is the 2.5−V internal voltage reference connected to the positive input of the OTA

C_z is the compensation capacitor in series with R_z, both placed between VCTRL pin and GND

$$C_z = \frac{K_{factor}}{2\pi R_z f_{co,max}} \quad \text{(eq. 38)}$$

C_p is the compensation capacitor placed between VCTRL pin and GND, in parallel with C_z in series with R_z and is given by:

$$C_p = \frac{C_z}{2\pi C_z K_{factor} R_z f_{co,max} - 1} \quad \text{(eq. 39)}$$

Soft and Fast Overvoltage Protection (SOVP & FOVP):

These functions are checking that the output voltage is within the proper regulation window by monitoring the FB pin voltage:

The Fast Over−Voltage Protection (FOVP) trips if the bulk voltage reaches an abnormally high level.

$V_{out,fovp} = 112.5\% \cdot V_{out,nom}$ for versions [A**]

$V_{out,fovp} = 110\% \cdot V_{out,nom}$ for versions [B**]

$V_{out,fovp} = 107\% \cdot V_{out,nom}$ for versions [C**]

After the Fast OVP trips, the DRV pin is immediately disabled (t_{ON}=0) hence the name Fast.

When the feedback network is properly designed and correctly connected, the bulk voltage cannot exceed the level set by the Fast OVP function.

Soft OVP is disabled for versions [A**]&[B**]

$V_{out,sovp}$ = 105 % for versions [C**]

If soft OVP threshold is reached, for example during no−load startup, the on−time is gradually reduced instead of disabling the drive pin (t_{ON} = 0) hence the name soft. The Fast OVP threshold is set higher than the Soft OVP one.

Undervoltage Protection (UVP):

At startup, the DRV pin is enabled, allowing switching, if V_{FB} rises above an internal threshold voltage named V_{UVPH} (V_{UVPH} = 450 mV).

After startup, the DRV pin is disabled if V_{FB} drops below an internal threshold voltage named V_{UVPL} (V_{UVPL} = 200 mV)

Line Voltage Sensing – Brown−out:

The line voltage is sensed thanks to the MULT pin which is sensing the rectified line voltage by the means of the resistor bridge divider. The ratio between MULT pin voltage and rectified line voltage V_{in} is called K_m (not to be confused with K_{mult} which is the gain of the internal multiplier).

So through the MULT pin, brown−in/out level (versions [**A]&[**B]) as well as line voltage status (HL/LL) (versions [**A]&[**C])can be set.

Brown−in brown−out

By default and before startup, the brown−out is enabled. When V_{MULT} sensed through MULT pin goes higher than the internal reference voltage V_{BOH} = 787 mV the brown−out is reset and allows the controller to start switching. After brown−out is reset, and switching activity starts, V_{line} continues to be sensed through MULT pin and when V_{MULT} falls under the brown−out internal reference voltage V_{BOL} = 709 mV for 50 ms, then brown−out is enabled. After brown−out is confimed, drive pulses are not immediately disabled, instead, a 30−μA current source is applied to the VCTRL pin to gradually reduce V_{CTRL}. As a result, the circuit only stops pulsing when the static OVP function is activated (that is when V_{CTRL} reaches a 0.550−V threshold). At that moment, the circuit stops switching. This method limits any risk of false tripping. The following formulas are showing how internal brown−out reference voltages translate to line rms voltage thresholds.

$$(V_{line,rms})_{boH} = \frac{V_{boH}}{K_m\sqrt{2}} = \frac{0.787}{0.006622\sqrt{2}} = 80V \quad \text{(eq. 40)}$$

$$(V_{line,rms})_{boL} = \frac{V_{boL}}{K_m\sqrt{2}} = \frac{0.787}{0.006622\sqrt{2}} = 72V \quad \text{(eq. 41)}$$

Where:

- V_{boH} is the 787−mV upper brown−out internal threshold, also called brown−in.
- V_{boL} is the 709−mV lower brown−out internal threshold.

High and low line detection

An internal digital flag named LLINE is used to detect if the line voltage is low (LLINE=1) or high (LLINE=0). This flag is used to change the internal multiplier gain K_{mult} and the current sense voltage reference V_{CS_OCP} for over current protection for the versions [**A]&[**C]. This K_{mult} change versus line level does a two−level line feed−forward and reduce the spread of the small signal open−loop cut−off

frequency. Changing the OCP internal levels versus line level make also sense as the inductor peak current at high line will be much lower than at low line.

There is an abrupt change in VCTRL pin voltage when transitioning from high line to low line and vice versa. Like in the brown−out detection circuit, the MULT pin voltage V_{MULT} is compared to two levels defining an hysteresis between high line and low line states. When V_{MULT} goes above V_{HL}=1.625 V, the controller enters the high line state and when V_{MULT} goes under V_{LL}=1.422 V it toggles into the low line state. Translation of high line to low line thresholds and vice versa into line rms voltage is given by the following equations.

Low line to high line threshold is :

$$\left(V_{line,rms}\right)_{HL} = \frac{V_{HL}}{K_m\sqrt{2}} = \frac{1.625}{0.006622\sqrt{2}} = 173.5V \qquad \text{(eq. 42)}$$

High line to low line threshold is :

$$\left(V_{line,rms}\right)_{LL} = \frac{V_{LL}}{K_m\sqrt{2}} = \frac{1.422}{0.006622\sqrt{2}} = 151.9V \qquad \text{(eq. 43)}$$

X2 Capacitors Discharge:

R_{X1} and R_{X2} are designed for safety considerations. In general, they must be selected so that the series combination of (R_{x1} + R_{x2} = 2R_x) form with the X2 EMI capacitors a time constant less than 1 s. In our case, two 1−MΩ resistors (R_{x1} = R_{x2} = R_x = 1 MΩ) are implemented so that with the selected X2 capacitors, of a 770 nF total capacitance of our evaluation board leads to a 1.54−s discharge time constant which is higher than what is specified but can be easily fixed by modifying the value of Rx1 and Rx2 discharge resistors.

Current Sense Network:

The current sense circuitry consists of a current sensing resistor *R_{sense}* placed between the source of the switching Power MOSFET and GND.

The value of the sense resistor R_{sense} is calculated in order that the maximum inductor peak current reaches the low line OCP threshold for minimum low line voltage.

The design equation for R_{sense} is given by:

$$R_{sense} = \frac{V_{mains,rms,LL,min}V_{OCP,LL,min}}{4\frac{P_{out,max}}{\eta}}\sqrt{2} \qquad \text{(eq. 44)}$$

Numerical example for a 200w application:

$$R_{sense} = \frac{84 \times 0.97}{4 \times \frac{200}{0.93}}\sqrt{2} = 134m\Omega \qquad \text{(eq. 45)}$$

η is the power efficiency, 0.93 corresponding to 93%

Once R_{sense} is set this way, it will work OK for both Low−Line and High−Line conditions. If a version without line level detection is used, the same formula can be used, the only thing to do is just to replace $V_{mains,rms,LL,min}$ by $V_{mains,rms,min}$ and $V_{OCP,LL,min}$ by $V_{OCP,min}$.

R_{sense} losses can be computed using the equation giving the MOSFET conduction losses where R_{sense} replace $R_{DS(on)}$:

$$(P_{R_{sense}})_{max} = \frac{4}{3} \cdot R_{sense} \cdot \left(\frac{(P_{in,avg})_{max}}{(V_{line,rms)LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}}\right) \qquad \text{(eq. 46)}$$

Hence, our 134−mΩ current sense resistor will dissipate about 775 mW at full load, low line.

$$(P_{R_{sense}})_{max} = \frac{4}{3} \times 0.134 \cdot \left(\frac{200/0.93}{90}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 450}\right) = 775mW \qquad \text{(eq. 47)}$$

Zero Current Circuitry:

The ZCD circuitry is show in Figure 1 This is a very classical ZCD circuitry which needs only a RZCD resistor (typically 47 kΩ), placed between auxiliary winding voltage and ZCD pin.

During on−time, the auxiliary voltage is given by:

$$V_{aux} = -\frac{N_{aux}}{N_p}V_{in} \qquad \text{(eq. 48)}$$

During demagnetization time, the auxiliary voltage is given by:

$$V_{aux} = \frac{N_{aux}}{N_p}\left(V_{bulk} - V_{in}\right) \qquad \text{(eq. 49)}$$

During dead−time, the auxiliary voltage is given by:

$$V_{aux} = \frac{N_{aux}}{N_p}\left(V_{drain} - V_{in}\right) \qquad \text{(eq. 50)}$$

There are two internal voltage clamps on the ZCD pin. One which will clamp the ZCD voltage at Vcc + Vbe during demagnetization time and another clamp which is an internal diode which will avoid the ZCD pin voltage to go under −Vbe.

The RZCD resistor purpose is to limit the current absorbed by the two clamps and more particularly the –Vbe clamp which can be dangerous if carrying to much current (risk of latch−up).

If we do not want that either positive ZCD current and negative ZCD current to be more than 1 mA in absolute value, the RZCD value is given by:

$$R_{ZCD} \geq \max\left[\frac{\frac{N_{aux}}{n_p}V_{bulk,max} - V_{CC,off,min} - V_{be}}{1mA}; \frac{\frac{N_{aux}}{n_p}V_{line,max}\sqrt{2} - V_{be}}{1mA}\right] \qquad \text{(eq. 51)}$$

If we calculate with numerical values, we get

$$R_{ZCD} \geq \max\left[\frac{0.1 \times 450 - 8.5 - 0.6}{1mA}; \frac{0.1 \times 305\sqrt{2} - 0.6}{1mA}\right] = \max[35.9k\Omega; 42.5k\Omega] \qquad \text{(eq. 52)}$$

We can see that R_{ZCD} = 47 kΩ satisfies the above equation.

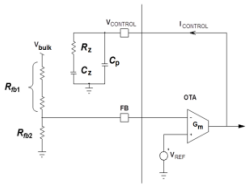
Layout and Noise immunity considerations:

The NCL2801 is not particularly sensitive to noise as it uses proven techniques. However, usual layout rules for power supply design apply. Among them, let us remind the following ones:

- The loop area of the power train must be minimized
- Star configuration for the power ground that provide the current return path
- Star configuration for the circuit ground
- The circuit ground and the power ground should be connected by one single path, no loop is allowed.
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{sense}).
- A 100 or 220−nF capacitor should be placed between the circuit V_{CC} and GND pins, with minimized connection length
- It is recommended to place a filtering capacitor on the FB pin to protect the pin from possible surrounding noise. It must be small however not to distort the voltage sensed by the FB pin. See the corresponding sections for more details

Table 1. SUMMARY OF THE MAIN EQUATIONS

Steps	Components	Formulae	Comments
Step 1 – Key Specifications	f_{line}	Line frequency. It is often specified in a range of 47−63 Hz for 50 Hz / 60 Hz applications.	
	$(V_{line,rms})_{LL}$	Lowest Level of the line voltage, e.g., 90 V or sometimes 84 V	
	$(V_{line,rms})_{HL}$	Highest Level for the line voltage (e.g., 264 V in many countries, 305 V for some lighting applications).	
	$(V_{line,rms})_{boH}$	Brown−Output Line Upper Threshold. The circuit prevents operation until the line rms voltage exceeds this level.	
	$V_{out,nom}$	Nominal Output Voltage.	
	$(\delta V_{out})_{pk-pk}$	Peak−to peak output voltage low−frequency ripple.	
	$t_{HOLD-UP}$	Hold−up Time that is the amount of time output will remain valid during line drop−out.	
	$(V_{out,min})$	Minimum output voltage allowing for operation of the downstream converter.	
	$P_{out,max}$	Maximum output power consumed by the PFC load, that is, 200 W in our application.	
	$(P_{in,avg})_{max}$	Maximum power absorbed from the mains in normal operation. Generally obtained at full load, low line, it depends on the efficiency that, as a rule of a thumb, can be set to 95%.	
	$f_{Co,max}$	Maximum open−loop cross−over frequency	
	$\varphi_{plant,fco,max}$	Plant phase margin	
Step2 – Power Components	Input Diodes Bridge Losses	$P_{bridge} = 2 \cdot V_f \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta}$	V_f is the forward voltage of any diode of the bridge. It is generally in the range of 1 V or less.
	Inductor	$L \leq \frac{\left(V_{line,rms}\right)_{LL}^2}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max}$ $\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}}$ $\left(I_{L,rms}\right)_{max} = \frac{\left(I_{L,pk}\right)_{max}}{\sqrt{6}}$	
	MOSFET Conduction Losses	$(p_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot (V_{line,rms})_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}}\right)$	$R_{DS(on)}$ is the drain−source on−state resistance of the MOSFET
	Bulk Capacitor Constraints	$C_{bulk} \leq \frac{P_{out,max}}{(\delta V_{out})_{pk-pk} \cdot \omega \cdot V_{out,nom}}$ $C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^2 - V_{out,min}^2}$ $(I_{c,rms})_{max} \cong \sqrt{\left(\sqrt{32\frac{\sqrt{2}}{9\pi}} \cdot \frac{(P_{in,avg})_{max}}{\sqrt{(V_{line,rms})_{LL}} \cdot V_{out,nom}}\right)^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2}$	These 3 equations quantify the constraints resulting from the low−frequency ripple $(\delta V_{out})_{pk-pk}$ that must be kept below 8%), the hold−up time requirement and the rms current to be sustained.

<table>
<tr><td rowspan="3">Step3 – Bulk Voltage Monitoring and Regulation Loop</td><td>Resistor Divider</td><td>$$R_{fb2} = \frac{2.5}{I_{FB}}$$
$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right)$$
$$C_{fb1} \leq \frac{1}{150 \cdot (R_{fb1} \| R_{fb2}) \cdot f_{line}}$$</td><td>I_{FB} is the bias current that is targeted within the resistor divider. Values in the range of 50 μA to 100 μA generally give a good trade−off between losses and noise immunity.
C_{fb} is the filtering capacitor that can be placed between the FB pin and ground to increase the noise immunity of this pin.
  </td></tr>
<tr><td>Compensation</td><td>$$G_0 = \frac{(V_{mains,max,HL})^2 K_m K_{mult,HL}}{4 V_{bulk,nom}} \cdot \frac{V_{regul,range}}{V_{CTRL,range}} \cdot \frac{R_{load,min}}{R_{sense}}$$
$$R_{load,min} = \frac{(V_{bulk,nom})^2}{P_{out,max}}$$
$$G_{plant,fco,max} = 20\log_{10}\left|\frac{G_0}{1 + i2\pi f_{co,max} C_{bulk} \frac{R_{load,min}}{2}}\right|$$
$$\varphi_{plant,fco,max} = \text{Phase}\left(\frac{G_0}{1 + i2\pi f_{co,max} C_{bulk} \frac{R_{load,min}}{2}}\right)$$
$$K_{factor} = \tan\left(\frac{\pi}{360} \cdot \left(\varphi_m - \varphi_{plant,fco,max}\right)\right)$$
$$R_z = \frac{V_{bulk,nom}}{10^{\left(\frac{G_{plant,fco,max}}{20}\right)} \cdot G_m \cdot V_{ref}}$$
$$C_z = \frac{K_{factor}}{2\pi R_z f_{co}} \qquad C_p = \frac{C_z}{2\pi C_z K_{factor} R_z f_{co} - 1}$$</td></tr>
<tr><td>OVP and UV</td><td>Soft and fast OVP thresholds are based on part option used. Ratio based on nominal output voltage
$V_{out.UVP.x} = K_{FB} \cdot V_{UVP.x}$</td><td>OVP and UV are sensed by the feedback network (K_{FB})</td></tr>
<tr><td>Step4 – Input voltage sensing</td><td>Input Voltage Sensing</td><td>$$K_m = 6.622m$$
$$(V_{line,rms})_{boH} = \frac{V_{BOH}}{K_m \sqrt{2}}$$
$$(V_{line,rms})_{boL} = \frac{V_{BOL}}{K_m \sqrt{2}}$$
$$(V_{line,rms})_{HL} = \frac{V_{HL}}{K_m \sqrt{2}}$$
$$(V_{line,rms})_{LL} = \frac{V_{LL}}{K_m \sqrt{2}}$$</td><td>Input voltage is sensed through the MULT pin $(V_{line,rms})_{boH}$ line rms level above which the circuit starts operating. The circuit stops switching when line rms level falls under $(V_{line,rms})_{boL}$.
When line rms voltage goes above $(V_{line,rms})_{HL}$ we enter High Line state and when line rms voltage below $(V_{line,rms})_{LL}$ we enter Low Line state</td></tr>
</table>

Step5 – Current sense network	Current Sense Resistor	$R_{sense} = \frac{V_{mains,rms,LL,min} V_{OCP,LL,min} \sqrt{2}}{4 \frac{P_{out,max}}{\eta}}$ $\left(P_{RCS}\right)_{max} = \frac{4}{3} \cdot R_{sense} \cdot \left(\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}} \right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,nom}} \right)$	$(V_{line,rms})_{LL}$ is the line rms voltage lowest level in normal condition (e.g., 90 V). $V_{out,nom}$ is the output nominal level (e.g., 450 V). $(P_{in,avg})_{max}$ is the maximum input power of your application.
	Zero Current Detection	$R_{ZCD} \geq \max \left[\frac{\frac{N_{aux}}{n_p} V_{bulk,max} - V_{CC,off,min} - V_{be}}{1mA} ; \frac{\frac{N_{aux}}{n_p} V_{line,max} \sqrt{2} - V_{be}}{1mA} \right]$	RZCD is placed between the auxiliary winding and the ZCD pin. Two conditions must be met as shown. One is current flowing into the pin, and the other out of the pin.

CONCLUSIONS

This paper summarizes the key steps when dimensioning a NCL2801−driven PFC stage. The proposed approach being systematic, it can be easily applied to other applications.

REFERENCES

More details on the circuit operation can be found in its data sheet [4].

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4. NCL2801 data sheet
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