AND9923/D

FAN6390 Highly Integrated Secondary-Side Adaptive USB Type-C Charging Controller with USB-PD

ON Semiconductor®

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APPLICATION NOTE

Introduction to Application Note of FAN6390MPX

- Step−by−step Design Procedure
- PCB Layout Recommendation

Features of FAN6390MPX

- USB Type−C Rev 1.3 Compatible
- Support up to 60 W Output Power
- Constant Voltage (CV) and Constant Current (CC) Regulation with Two Operational Amplifiers of Open−Drain Type for Dual−Loop CV/CC Control
- Charge Pump Circuit to Enhance SR Driving Voltage for High Efficiency
- Small Current Sensing Resistor (5 mΩ) for High Efficiency
- N−Channel Back to Back MOSFET Control as a Load Switch
- Built−in Output Capacitor Bleeding Function for Fast Discharging
- Precise Voltage & Current Control for Minimum Step Size Via 10−bit DAC
- 10−bit ADC for Monitoring Voltage, Current and Temperature
- Auto Re−start Protection Mode Option to Disable Load Switch for 2 Seconds
- Support Protections: Output Over−Voltage Protection, Under−Voltage Protection, External Over Temperature Protection via NTC, Internal Over Temperature Protection, Cable Fault Protection and CC Lines Over Voltage Protection

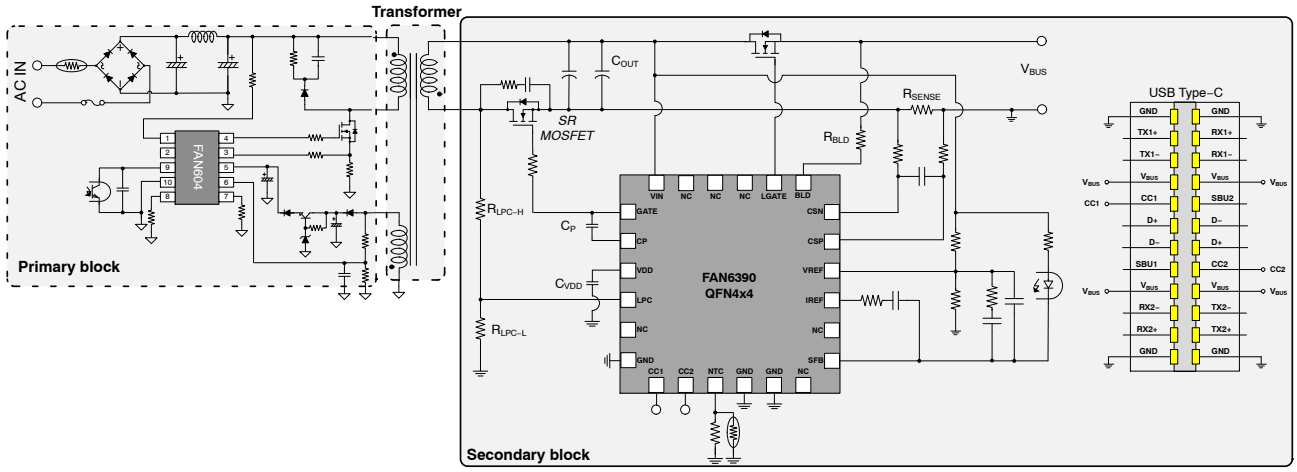

Figure 1. Typical Application

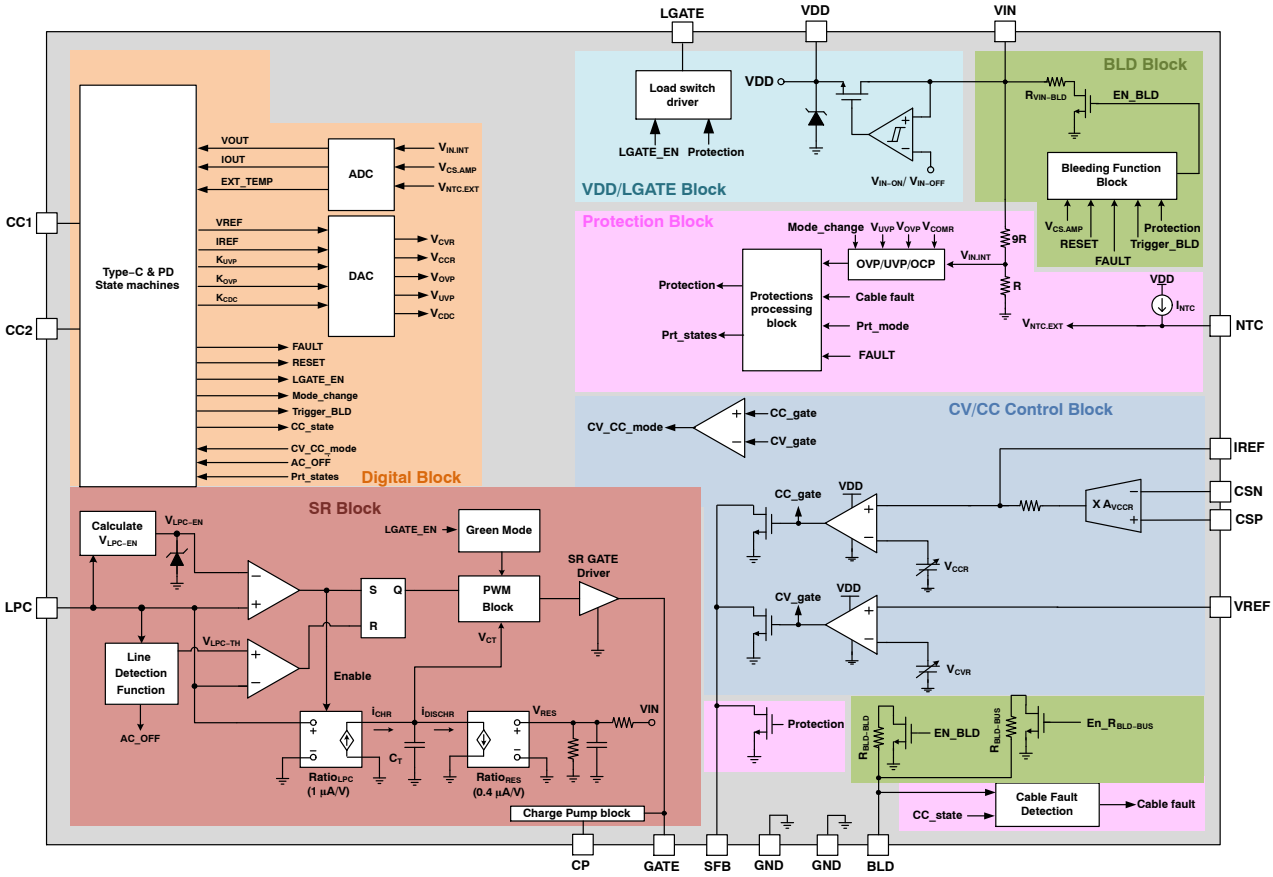

Figure 2. Functional Block Diagram

STEP−BY−STEP DESIGN PROCEDURE

System Specifications and Device Selection

FAN6390MPX has line−up according to output nominal currents. The first step of system design needs to select a device. FAN6390MPX incorporates many valuable functions and some functions are only compatible with FAN604 series of ON Semiconductor. Therefore, it is strongly recommended to select one of FAN604 as a primary controller. As FAN6390MPX is state machine based which provides several kinds of trim function as Table 1, we use FAN6390MPX trim which has specific function trim for a 60 W output power design. Table 3 is bill of materials. Figure 3 and Figure 4 are design circuits.

Table 1. SUMMARY TABLE OF ALL KINDS OF TRIM FUNCTION

Function	All Trims	FAN6390MPXMPX Trim
Cable Fault (Note 1)	0: Disabled 1: Enabled	“1” is selected. “0” is for compliance box test.
Internal RES Ratio = $1/Ratio_{RRES}$	00: 0.14 (for N_P/N_S = 7.5~10) 01: 0.18 (for N_P/N_S = 9.5~13) 10: 0.11 (for N_P/N_S = 6.5~7.5) 11: 0.10 (for N_P/N_S = 5~6.5) Note: N_P and N_S are primary and secondary transformer turns	“10” is selected.
Cable Compensation for PDO	00: 150 mV/A 01: 50 mV/A 10: 100 mV/A 11: Disabled	“00” is selected. “11” is used for PD compliance box test that additional cable compensation on DFP is no need.
Current Sensing	1: 10 mΩ 0: 5 mΩ	“0” is selected. (Smaller current sensing resistor has better efficiency but could be more expensive. In order to trade off cost and efficiency for flexible design, two kinds of popular current sensing resistors are provided.)
Support PD2.0 or 3.0	0: Enable PD2.0 1: Enable PD3.0	“1” is selected. (FAN6390MPX series support only PDO power profile via PD2.0 trim and PDO plus APDO(PPS) power profile via PD3.0 trim.)
Default 5 V Adjustment	0: 5.0 V 1: 5.2 V	“0” is selected. (Two kinds of default 5 V adjustment for flexible design)
Adjustable Output Profile	8 kinds of output power profile can be selectable as list1.	“000” is selected.
Protection Modes (Note 1)	0: Auto−restart after 2sec 1: Latch protection. System re−start up	“0” is selected.
Output OVP	PDO case and PPS case 00: 120% 01: 125% 10: 130% 11: 115%	“00” is selected.
Output UVP (Note 2)	PDO case: 00: 65% 01: 60% 10: 70% 11: Disable PPS case: disable	“10” is selected.
PDO Current Mode (Note 3)	00: 5 V (107% CC), 9/15/20 V (120 % CC) 01: 5/9/15/20 V (107% CC) 10: 5/9/15/20 V (120% CC)	“00” is selected. “10” is used for PD compliance box test.
Output Power	Output power range from 15 W~60 W 000000: 15 W 000001: 16 W ... 111111: 60 W	“111111” is selected.

1. Function explanation refers to section Protection Mode Function Explanation.
2. Based on compliance spec PPS case is current limit. Output voltage could be lower than the requested PPS voltage command during current limit. In order to operate at current limit region, FAN6390MPX disable UVP and operates until $V_{IN−OFF}$.
3. Except of PDO, all APDO power profiles are 100% CC.

Table 2. UP TO 8 KINDS OF OUTPUT POWER PROFILES SELECTED BY TRIM

Power Profile Trim	Output Profile Trim		
	15 W ≤ P ≤ 27 W	**27 W < P ≤ 45 W**	**45 W < P ≤ 60 W**
000	• 5 V • 9 V • 12 V (Note 4) If PD3.0 trim activated • PPS 5 V • PPS 9 V	• 5 V • 9 V • 12 V • 15 V If PD3.0 trim activated • PPS 5 V • PPS 9 V • PPS 15 V	• 5 V • 9 V • 15 V • 20 V If PD3.0 trim activated • PPS 9 V • PPS 15 V • PPS 20 V
001	• 5 V • 5.5 V • 6.0 V • 7.0 V • 8.0 V • 9 V • 10.0 V	• 5 V • 5.5 V • 6.0 V • 7.0 V • 8.0 V • 9 V • 15 V	• 5 V • 5.5 V • 6.0 V • 7.0 V • 9 V • 15 V • 20 V
010	• 5 V • 6.0 V • 7.0 V • 8.0 V • 9 V If PD3.0 trim activated • PPS 5 V • PPS 9 V	• 5 V • 6.0 V • 7.0 V • 9 V • 15 V If PD3.0 trim activated • PPS 9 V • PPS 15 V	• 5 V • 6.0 V • 9 V • 15 V • 20 V If PD3.0 trim activated • PPS 15 V • PPS 20 V
011	• 5 V • 5.5 V • 6.0 V • 6.5 V • 7.0 V • 8.0 V • 9 V	• 5 V • 5.5 V • 6.0 V • 6.5 V • 7.0 V • 9 V • 15 V	• 5 V • 5.5 V • 6.0 V • 6.5 V • 9 V • 15 V • 20 V
100	• 5 V • 5.6 V • 9 V • 11 V	• 5 V • 5.6 V • 9 V • 11 V • 15 V	• 5 V • 5.6 V • 9 V • 11 V • 15 V • 20 V
101	• 5 V • 9 V • 14.5 V	• 5 V • 9 V • 14.5 V • 15 V	• 5 V • 9 V • 14.5 V • 15 V • 20 V
110	• 5 V • 9 V • 11 V	• 5 V • 9 V • 11 V • 15 V	• 5 V • 9 V • 11 V • 15 V • 20 V
111		• 5 V • 9 V • 15 V • 20 V	

4. 12 V can be possible to enable or disable by trim.

Table 3. BILL OF MATERIALS (BOM)

Designator	Qty	Part Number & Value	Designator	Qty	Part Number & Value
ZD1, ZD2	2	VCUT05B1−DD1	C16	1	SMD Capacitor 0603 X7R ±10% 470P 25 V
D6	1	NC	C2	1	SMD Capacitor 0805 X5R ±20% 226P 25 V
R6	1	NC	C3	1	SMD Capacitor C0805 106P 50 V K X5R Murata
R4	1	SMD Resistor 0603 46 kΩ ±1%	C4	1	SMD Capacitor 0805 X7R ±10% 104P 50 V
R32	1	SMD Resistor 0603 20 kΩ ±1%	C13	1	NC
R9	1	SMD Resistor 0603 2.2 kΩ ±1%	C12	1	SMD Capacitor 0805 X7R ±10% 221P 100 V
R13, R39, R40, R22	4	SMD Resistor 0603 0 Ω ±5%	C23	1	SMD Capacitor 0603 X7R ±10%
R15	1	SMD Resistor 0603 100 Ω ±5%			220P 50 V
R16, R24, R25	3	SMD Resistor 0603 10 Ω ±5%	C22	1	SMD Capacitor 0603 X7R ±10% 220P 50 V
R28, R29	2	SMD Resistor 0603 1 kΩ ±5%	C9	1	SMD Capacitor 1206 X7R ±10% 471P 1 KV
R21	1	SMD Resistor 0603 1.5 kΩ ±5%	R7	1	SMD 0805 Inductor 10 μH
R23	1	SMD Resistor 0603 100 kΩ ±5%	NTC1	1	SMD NTC 0603 100 kΩ ±1%
R38	1	SMD Resistor 0603 10 kΩ ±5%	BR1	1	Bridge rectifier 2KBP06M
R34	1	SMD Resistor 0603 220 kΩ ±1%	Q1,Q6	2	KS1008YBU
R41	1	SMD Resistor 0603 50 Ω ±1%	Q2	1	FCPF380N65FL1
R39, R40, R44	3	SMD Resistor 0603 0 Ω ±1%	Q3	1	NVMFS6B03NL
R37	1	SMD Resistor 0603 13.3 kΩ ±1%	Q4	1	FDMS7580
R33	1	SMD Resistor 0603 120 kΩ ±1%	Q5	1	FDMS7580
R36	1	SMD Resistor 0603 7.15 kΩ ±1%	U1	1	FAN604H
R30	1	SMD Resistor 0603 169 kΩ ±1%	U2	1	FAN6390MPX
R1	1	SMD Resistor 0805 10 kΩ ±5%	U3	1	Photo Coupler EL1018
R8	1	SMD Resistor 0805 51.1 kΩ ±1%	D5, D7	2	SMD diode FFM107M
R5, R10	2	SMD Resistor 0805 75 kΩ ±1%	D3	1	SMD diode FFM104M
R2, R3	2	NC	D1, D4	2	SMD diode 1N4148WS
R11, R12	2	SMD Resistor1206 604 kΩ ±1%	F1	1	Fuse 250V3.15A MST
R26	1	SMD Resistor1206 50R Ω ±1%	C6, C7	2	Aluminium Electrolytic Capacitor 47 μF 400 V 105°C
R14, R20, R35	3	SMD Resistor1206 33 Ω ±5%	C17, C19	2	Conductive Polymer Aluminum Solid Capacitors 470uF/35V 10*13mm PZ AISHI
R17	1	SMD Resistor1206 1.5R Ω ±1%	C31	1	Aluminium Electrolytic Capacitor 22 μF 50 V 5 × 11 mm 105°C
R18	1	SMD Resistor1206 1.6R Ω ±1%	CY1	1	Y1Capacitor 222P/250 V ±20%
R19	1	SMD Resistor1206 0.5R Ω ±5%	C1	1	TVR10471KSY
R31	1	SMD Resistor1206 0.005 Ω ±1%	LF2	1	TRN0003 900 μH
C5, C14	2	SMD Capacitor 0603 X7R ±10% 102P 50 V	L2	1	TRN0083 1.6 μH
C8	1	SMD Capacitor 0603 X7R ±10% 22P 50 V	LF1	1	Wurth 744822233 3.3 mH
C10	1	SMD Capacitor 0603 X7R ±10% 471P 25 V	D2	1	SMD ZENER MMSZ5253B
C15	1	SMD Capacitor 0603 X7R ±10% 105P 50 V	TX1	1	Transformer RM10

Table 3. BILL OF MATERIALS (BOM) (continued)

Designator	Qty	Part Number & Value	Designator	Qty	Part Number & Value
C30	1	SMD Capacitor 0603 X7R ±10% 104P 50 V	TH1	1	SCK053
C21	1	SMD Capacitor 0603 X7R ±10% 103P 25 V	J1	1	TYPE C USB 317JD24BZTF3N0A3
C20	1	SMD Capacitor 0603 X7R ±10% 472P 25 V	Q2	1	Heat sink MCH0452
C18	1	SMD Capacitor 0603 X7R ±10% 472P 25 V			

Schematics

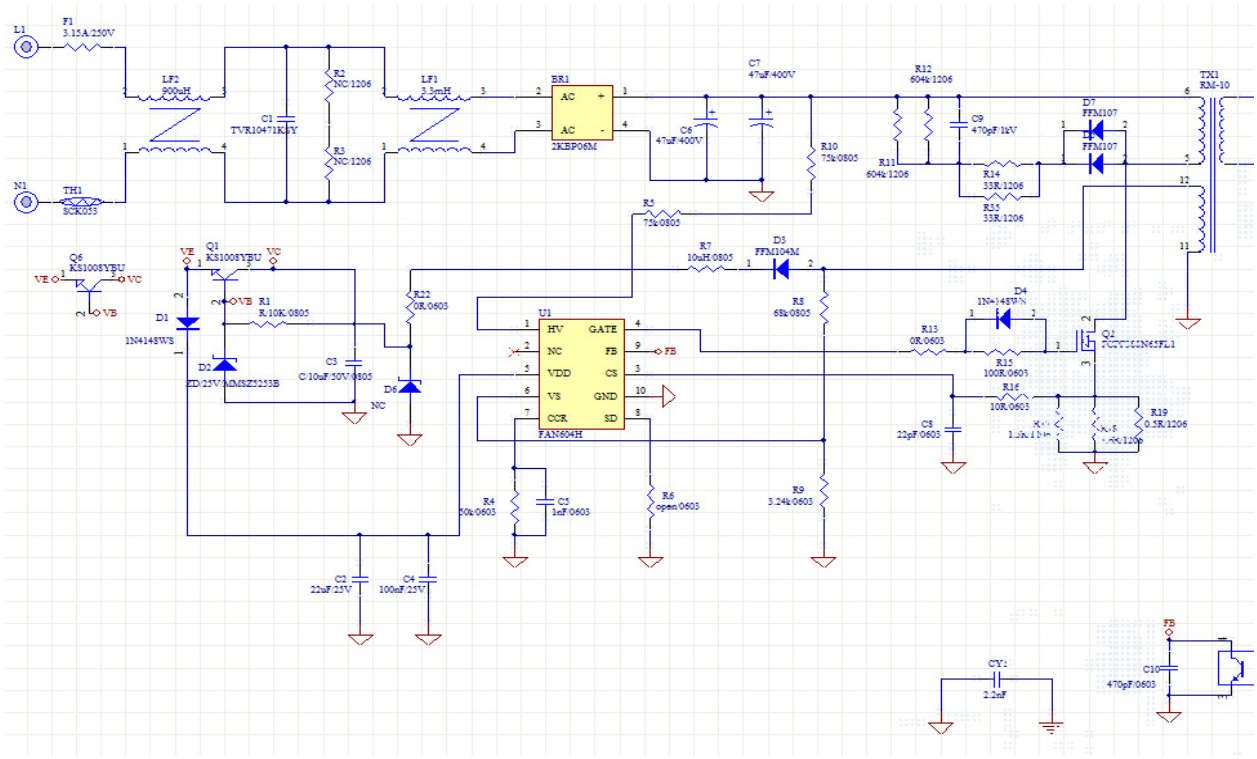

Figure 3. Primary Circuit Schematic

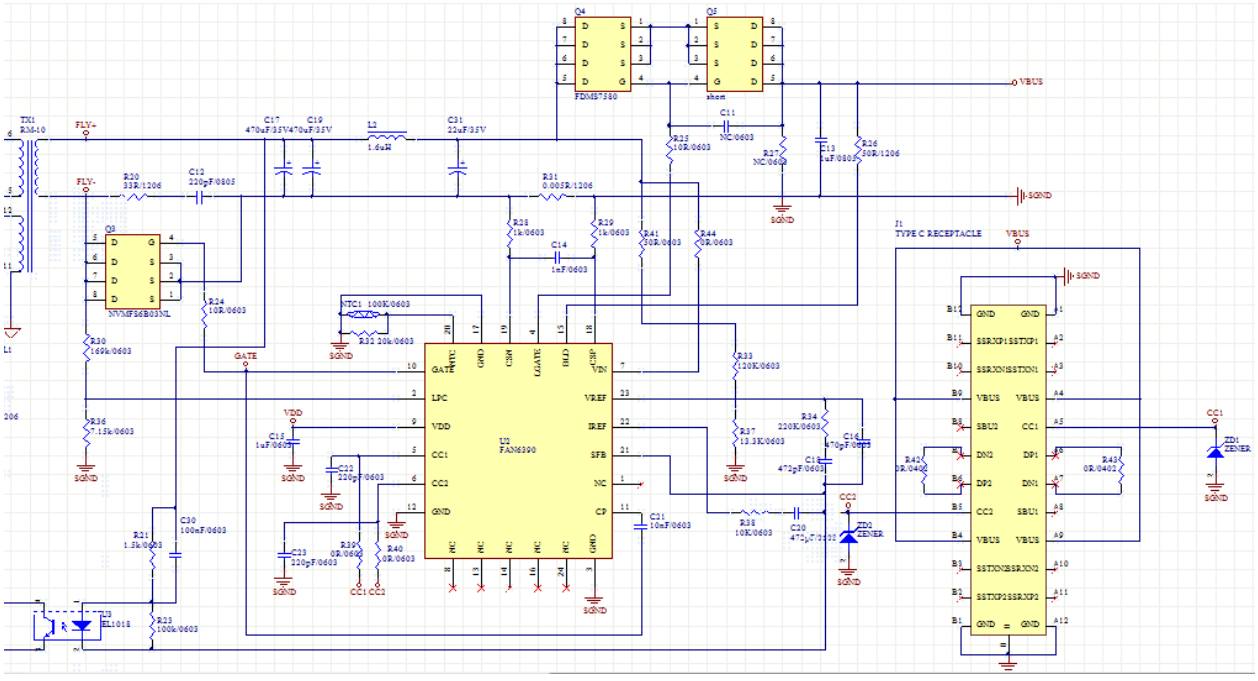

Figure 4. Secondary Circuit Schematic

Power Stage Design Including Transformer Design

Application note of FAN604 series supports power stage design and transformer design. In order to optimize operation of synchronous rectifier for 60 W output power design, the recommended transformer turn ratio and LPC resistors are introduced in section Synchronous Rectifier Design Considerations.

VREF Resistor Array Design

VREF pin is connected with resistor array to regulate output voltage. According to FAN6390 internal reference voltage of V_{CVR}, it is 1/10 of external output voltage so that the recommended ratio of ($R_{REF\_L} + R_{REF\_H}$)/ R_{REF_L} is 10. Based on the calculation of output voltage, typically R_{REF_L} range is around 5~20 kΩ. 13.3 kΩ is selected so R_{REF_H} can be derived as 120 kΩ by eq. 2.

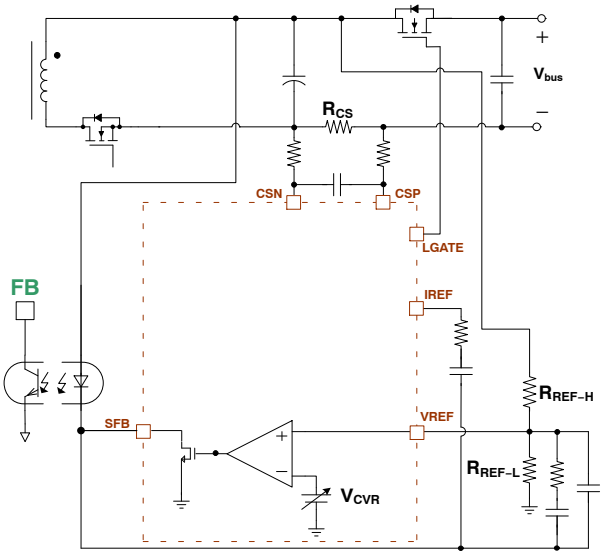

Figure 5. VREF Resistor Array Configuration

$$V_{bus} = V_{CVR}\left(\frac{R_{REF-H} + R_{REF-L}}{R_{REF-L}}\right) \quad \text{(eq. 1)}$$

$$R_{REF-H} = \left(\frac{R_{REF-L}\,V_{bus} - R_{REF-L}\,V_{CVR}}{V_{CVR}}\right) \quad \text{(eq. 2)}$$

Sensing Resistor Design

FAN6390MPX can select either 10 mΩ or 5 mΩ for current sense resistor depend on different trim. In this 60 W design example, 5 mΩ was used in order to reduce sensing resistance loss. However, practical constant current (CC) could be different than target level, for example even designed 3 A target CC but real result could be 2.9 A or 3.1 A. In this case root cause would be high possible that current sensing PCB pattern is too long or two current sensing lines are not balanced and so on. This is because the sensing resistance is too small and minor addition of PCB pattern would change the total resistance. To avoid this it is recommended to follow the PCB layout as guided in the PCB Layout Recommendation. The eq. 3 supports optimizing sensing resistor based on practical constant current value.

$$R_{CS\_Optimized} = \frac{I_{OUT\_CC\_Practical}}{I_{OUT\_CC\_Target}} \times 5\ m\Omega \quad \text{(eq. 3)}$$

Synchronous Rectifier Design Considerations

For the 60 W design example, the system specifications are as follows:

- Input voltage range: 85 ~ 264 Vac and 50 ~ 60 Hz
- 3 A outputs. **PD**: 5, 9, 15, 20 V. **PPS**: 9, 15, 20 V
- Minimum output voltage in CC range: 3.3 V

Determine the Resistors on LPC

FAN6390 uses ON proprietary SR control method, so called LPC (Linear Predict Control), and need to decide several resistances to make secure the stable operation.

Figure 7 shows voltage divider is used for LPC pin by dividing V_{DET} voltage and another RES voltage divider embedded inside chip adjusted by trim is used by dividing the output voltage. When designing the LPC resistors, it is needed to determine the ratio of LPC resistors ($Ratio_{RLPC}$ = ($R_1 + R_2$)/R_2) if it can meet following condition 1, 2 and 3 based on the selected ratio of RES resistors ($Ratio_{RRES}$ = (R_3 + R_4)/R_4) by trim and the voltage scaled−down ratio K ($Ratio_{RLPC}$/$Ratio_{RRES}$).

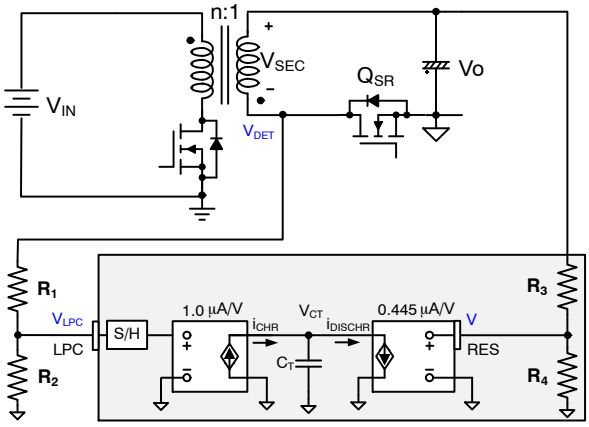

Figure 6. Typical Application Circuit for LPC Pins

1. *Determine the Voltage Scaled−down Ratio K:*
   The basic idea of the LPC is to estimate the instant when the magnetizing current of the transformer goes back to its initial condition after completing one switching cycle by emulating the operation of the magnetizing inductor current. Two voltage−controlled current sources and an internal timing capacitor C_T are used to emulate the charging and discharging of the magnetizing inductor.
   The current which charges the internal capacitor C_T while V_{LPC} is high is given by eq. 4.

$$i_{CT1} = \frac{\frac{V_{IN}}{n} + V_o}{Ratio_{RLPC}} \times 10^{-6} - \frac{V_o}{Ratio_{RRES}} \times 0.445 \times 10^{-6} \quad \text{(eq. 4)}$$

Whereas, the current discharges the internal capacitor C_T while V_{LPC} is low is given by eq. 5.

$$i_{CT2} = \frac{V_o}{Ratio_{RRES}} \times 0.445 \times 10^{-6} \quad \text{(eq. 5)}$$

The current−sec balance of CT which is equivalent to the volt−sec balance of the magnetizing inductor is as follows:

$$\left(\frac{\frac{V_{IN}}{n} + V_o}{Ratio_{RLPC}} - \frac{0.445V_o}{Ratio_{RRES}}\right) \times T_{ON.PWM} = \frac{0.445V_o}{Ratio_{RRES}} \times T_{ON.SR} \quad \text{(eq. 6)}$$

where $T_{ON,PWM}$ is the turn−on time of the primary side main switch and $T_{ON,SR}$ is the turn−on time of the SR MOSFET. Below eq. 7 is obtained as follows by substituting the voltage scaled−down ratio K ($Ratio_{RLPC}/Ratio_{RRES}$) to eq. 6.

$$\left(\frac{2.25}{K} \times \left(\frac{V_{IN}}{n} + V_O\right) - V_O\right) \times T_{ON.PWM} = V_O \times T_{ON.SR} \quad \text{(eq. 7)}$$

By setting K = 2.25, the voltage−sec balance equation is obtained. Thus, the C_T voltage decreases to zero when the SR current decreases to zero. Considering the tolerance of the resistor dividers and internal circuit, the coefficient K should be slightly larger than 2.25 to guarantee that the SR gate is turned off before the SR current reaches zero.

2. *Determine the Range of LPC Ratio:*
There are three conditions to determine the range of LPC ratio, as depicted in Figure 7 and Figure 8
   a. At minimum input voltage with full load condition, V_{LPC} should be greater than the SR enabled threshold voltage at High/low line, $V_{LPC-HIGH}$, as follows:

$$\frac{V_{DET\_85Vac(min)}}{Ratio_{RLPC}} > V_{LPC-HIGH-L(max)} \quad \text{(eq. 8)}$$

$$\frac{V_{DET\_220Vac(min)}}{Ratio_{RLPC}} > V_{LPC-HIGH-H(max)} \quad \text{(eq. 9)}$$

Where $V_{DET\_85Vac(min)}$ and $V_{DET\_220Vac(min)}$ are the minimum V_{DET} at high/low line when the input voltage is minimized considering the ripple on the primary side input capacitor C_{DL} depending on the load condition. It can be described as follows:

$$V_{DET\_85Vac(min)} = \frac{V_{IN\_85Vac(min)}}{n} + V_{o(min)} \quad \text{(eq. 10)}$$

$$V_{DET\_220Vac(min)} = \frac{V_{IN\_220Vac(min)}}{n} + V_{o(min)} \quad \text{(eq. 11)}$$

where V_O is the output voltage, n is the turns ratio of the transformer, and $V_{IN\_85Vac(min)}$ and $V_{IN\_220Vac(min)}$ are the minimum input voltage on C_{DL} applied to the primary side of the transformer at 85 or 220 Vac. Thus,

$$Ration_{RLPC} < \frac{\frac{V_{IN\_85Vac(min)}}{n} + V_{o(min)}}{V_{LPC-HIGH-L(max)}} \quad \text{(eq. 12)}$$

$$Ration_{RLPC} < \frac{\frac{V_{IN\_220Vac(min)}}{n} + V_{o(min)}}{V_{LPC-HIGH-L(max)}} \quad \text{(eq. 13)}$$

   b. At low line input (85 Vac) or high line input (220 Vac), V_{LPC} should be less and greater than V_{LINE-L} and V_{LINE-H} respectively to ensure the operation range at low line, as follows:

$$\frac{V_{DET-85Vac(max)}}{Ratio_{RLPC}} < V_{LINE-L(min)} \quad \text{(eq. 14)}$$

where

$$V_{DET-85Vac(max)} = \frac{\sqrt{2}V_{IN\_85Vac}}{n} + V_{o(max)}$$

$$\frac{V_{DET-220Vac(min)}}{Ratio_{RLPC}} > V_{LINE-H(max)} \quad \text{(eq. 15)}$$

3. Inside the LPC circuit there is a clamp circuit to avoid V_{LPC} to being greater than 4.525 V in order to make sure it is within the safe operation range and suggest not be greater than V_{DD}−0.6 V. This should be taken into consideration when system working at high line AC input since V_{LPC} is greater than it is at low line AC

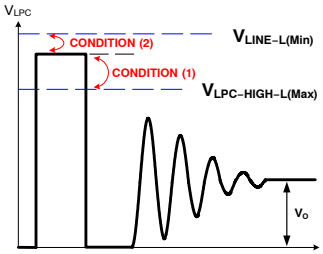

Figure 7. Conditions for Low Line 85 Vac Determining $Ratio_{RLPC}$

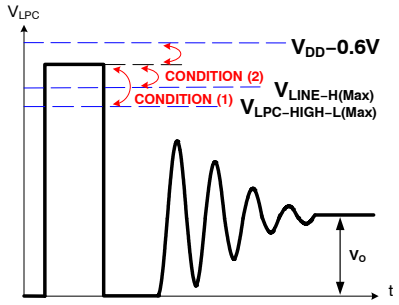

Figure 8. Conditions for High Line 220 Vac Determining $Ratio_{RLPC}$

Design Example

Typically input bulk capacitance and system power ratio is 2 μF for 1 Watt. Considering capacitance tolerance, design 60 W system using input bulk caps C_{in} = 84 μF which charging time ratio over a half line cycle period is 0.21 (D_{ch}), the output voltage ripple is ±5%, the voltage drop due to the load cable is assumed to be 0.21 V, and the estimated efficiency of the converter is 90%. Then minimum input bulk capacitance voltage $V_{IN\_Vac(min)}$ at universal AC input can be obtained as follows:

$$V_{IN\_Vac(min)} = \sqrt{\left(2 \times Vac^2 - \frac{(V_o + 0.4) \times I_o}{\eta} \times \frac{1 - D_{ch}}{C_{in} \times f_{L,min}}\right)} \quad \text{(eq. 16)}$$

where $f_{L,min}$ is the minimum line frequency. Therefore, select K = 2.7 in order to have proper dead time for safe operation with internal RES ratio = 0.11, then the $Ratio_{RLPC}$ is obtained as follows:

$$K \times Ratio_{RRES} = Ratio_{RLPC} = 2.7 \times 9.09 = 24.54 \quad \text{(eq. 17)}$$

At low line 85 Vac the first and second conditions for the range of $Ratio_{RRES}$ are obtained with given turns ratio n = 7 and Vo = 3.3~20 V as follows:

$$\frac{V_{IN\_85VDC(min)}}{n} + V_o > V_{LPC-HIGH-L(max)} \quad \text{(eq. 18)}$$

$$\frac{V_{IN\_85Vac(max)}}{n} + V_o > V_{LINE-L(min)} \quad \text{(eq. 19)}$$

where $V_{IN\_85Vac(max)} = \sqrt{2} \times 85Vac$

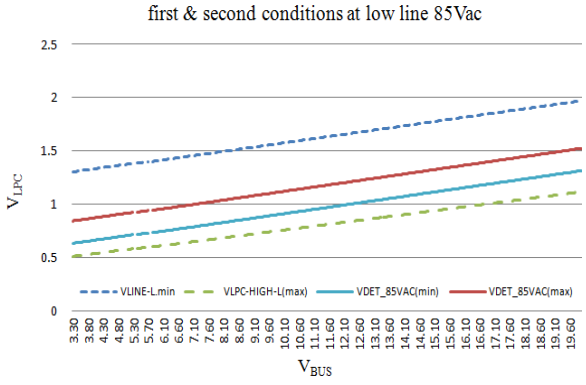

Figure 9. First & Second Conditions at 85 Vac

At high line 220 Vac the first, second and third conditions for the range of $Ratio_{RRES}$ is obtained with given turns ratio n = 7 and Vo = 3.3~20 V as follows:

$$\frac{V_{IN\_220Vac(min)}}{n} + V_o > V_{LPC-HIGH-H(max)} \quad \text{(eq. 20)}$$

$$\frac{V_{IN\_220Vac(min)}}{n} + V_o > V_{LINE-H(max)} \quad \text{(eq. 21)}$$

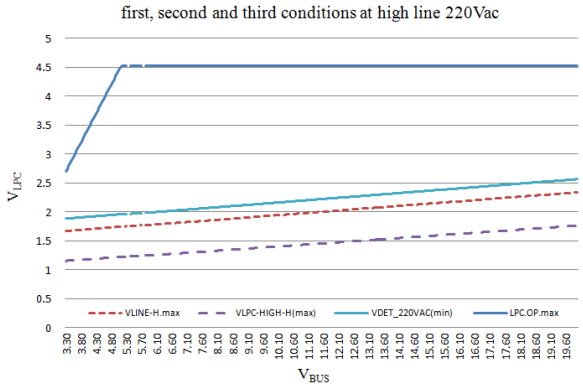

Figure 10. First, Second and Third Conditions at 264 Vac

As $Ratio_{RLPC}$ = 24.54, select R_2 = 169 kΩ and R_1 can be calculated as follows:

$$R_1 = R_2 \times (Ratio_{RLPC} - 1) \quad \text{(eq. 22)}$$

Selecting Capacitor on BUS and Bleeder Resistor Design (BLD Pin)

Based on USB PD specification, when source got hard reset command or cable is detached, output voltage should be discharged to vSafe0V within tSafe0V. To decrease the output voltage at this moment FAN6390 activates bleeder circuit at BLD pin. Bleeder circuit is made like that internal FET is connected to the GND and the FET is turned on when bleeding is needed. The amount of bleeding current is decided by the serial resistance between BLD pin and external voltage source. As long as load switch is turned on the bleeder will consumes the energy C_{out}. If it is assumed that load switch is turned on all the time then needed resistance to discharge the output voltage within tSafe0V can be found out at equation 23.

$$R_{BLD} < \frac{tSafe0V}{C_{out} \times \ln\frac{V_{BUS.Max}}{vSafe0V}} \quad \text{(eq. 23)}$$

Where, vSafe0V is the safe operating voltage at “zero volts”, tSafe0V is the time to reach vSafe0V max, C_{BUS} is capacitance before load switch, R_{BLD} is the external resistor connected between BLD pin and output voltage, $V_{BUS.MAX}$ is the maximum voltage that adaptor can make. When refer to USB PD specification, the maximum tSafe0V is 650 ms, the maximum vSafe0V is 0.8 V and $V_{BUS.MAX}$ is 20 V in 60 W design case. Then as equation 24, R_{BLD} is calculated to be less than 230 Ω when output capacitance C_{out} is 840 μF. However, FAN6390MPX internal bleeding switch resistance is 30 Ω around, which had better take into consideration as well. Overall it is 80 Ω around as RBLD is 50 Ω for this design in order to achieve fast discharge and meet PD specification.

$$R_{BLD} < \frac{650\ ms}{840\ \mu F \times \ln(20\ V/0.7\ V)} = 230\ \Omega \quad \text{(eq. 24)}$$

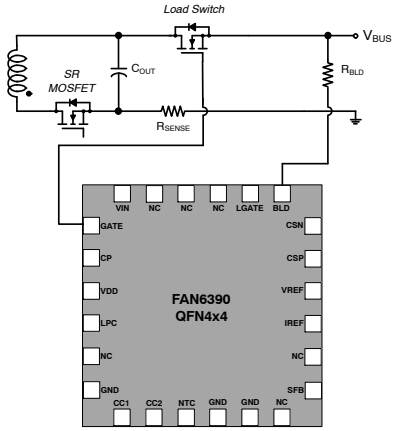

Figure 11. BUS Line Capacitor and Bleeding Resistor Connection

CC Line Capacitance Design (CC Pin)

FAN6390 CC pin is used to transmit BMC (Biphase Mark Coding) signal for PD communication. Based on USB−PD spec, the DFP (Downstream Facing Port) or UFP(Upstream Facing Port) system shall have capacitance within specific range, 200~600 pF, when not transmitting on the line. In a real design, 220 pF is used at each CC pin.

VDD Capacitance Design (VDD Pin)

FAN6390 VDD pin needs an external capacitor, C_{VDD}, typically 1 μF at least, as the energy storage element to stabilize the operation.

CP Capacitance Design (CP Pin)

Generally, SR driving voltage is powered by V_{DD} through V_{IN} and it drives internal circuits and SR MOSFET through GATE pin. The GATE driving voltage can't be higher than V_{BUS}. Accordingly when output voltage is low then gate voltage could be not enough to fully turn on FET especially when output voltage is low. When FET is not fully turned on then high conduction loss is inevitable and decreases the total system efficiency. In order to achieve higher' efficiency and lower thermal stress at SR MOSFET at low output voltage with high output current application, GATE voltage boosting function was added at CP pin as Figure 16.

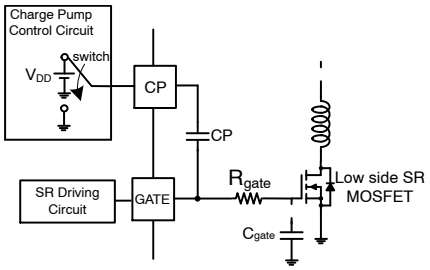

Figure 12. Charge Pump Control Circuit

Non logic MOSFET, that have conventional gate on threshold, is around 4 V(max) of gate threshold voltage. FAN6390's internal charge pump works as Figure 13 to raise gate voltage, V_{OH}. During blanking time the switch inside Charge Pump Control Circuit will switch to GND in order to have CP charge via SR Driving Circuit. After blanking time, the switch will connect to V_{DD} to boost V_{OH}. The V_{OH} will be clamped to 5.5 V(max) to ensure the voltage no higher than pin maximum rating to ensure driving circuit safe operation. Basically, proper CP capacitance is needed to achieve better system efficiency. While CP capacitance is larger, the higher is V_{OH} voltage that will have smaller MOSFET R_{ds-on}. However, charging current from SR Driving Circuit takes longer time to charge C_{gate} and CP.

In the end of blanking time larger CP has lower V_{OH} level that impact V_{OH} rising rate to late turn on MOSFET. R_{gate} used for EMI solution also will reduce SR Driving Circuit charging current to slow down V_{OH} rising rate as well.

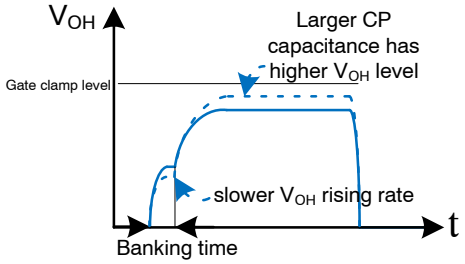

Figure 13. Timing Flow of Charge Pump

Below summarize all kinds of CP and R_{gate} combination results which needs to trade off for EMI and efficiency

- CP capacitance increase → Slower V_{OH} rising rate but greater V_{OH}
- CP capacitance decrease → Faster V_{OH} rising rate but less V_{OH}
- Rgate increase → Slower V_{OH} rising rate and lower V_{OH} with better EMI
- Rgate decrease → Faster V_{OH} rising rate and higher V_{OH} but suffer EMI

As real test Figure 14 and Figure 15 using CP = 2.2 nF and 10 nF are half and double size of C_{gate} = 5.32 nF (typ.) of MOSFET NVMFS6B03NL respectively with 10 Ω R_{gate}. At 3.3 V V_{BUS} which is the minimum output voltage, the V_{OH} is 4.16 V and 4.97 V with CP = 2.2 nF and 10 nF respectively that allow user to use non logic MOSFET for to achieve cost effective.

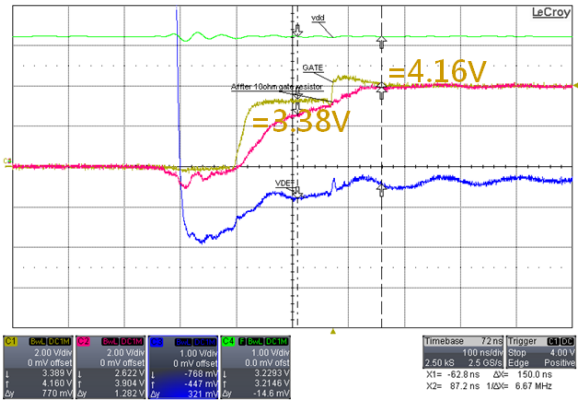

Figure 14. V_{OH} Level with CP = 2.2 nF (ch1: GATE pin; ch2: MOSFET Vgs; ch3: VDET: ch4: VDD)

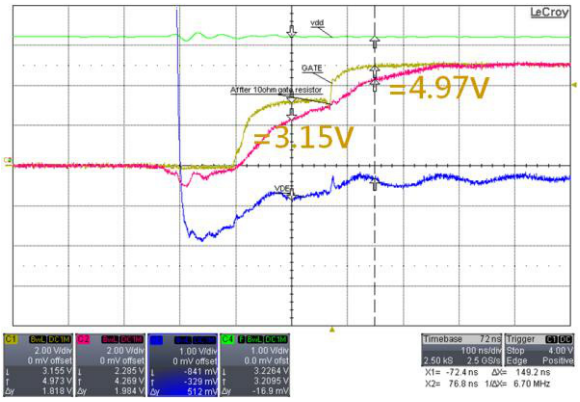

Figure 15. V_{OH} Level with CP = 10 nF (ch1: GATE pin; ch2: MOSFET Vgs; ch3: VDET: ch4: VDD)

NTC Protection Temperature Level Design

FAN6390 assigns NTC pin to detect external hot spot through NTC thermal resistor paralleled with a normal resistor as Figure 16. In order to ensure system safe operation, as Figure 21 FAN6390 has warning and protection temperature which are defined as ADC threshold value. FAN6390 detects external V_{NTC} voltage to react to warning through PD message to sink device or enters protection mode.

According to eq. 25, which is temp v.s. R_{NTC} calculation formula, the external V_{NTC} value is decided. Based on the recommend R_P and R_{NTC}, the typ. value of warning and protection temperature is 100°C and 110°C respectively.

$$R_{NTC} = R_{NTC\ at\ 25} \times e^{B_{25/50}\left(\frac{1}{Temp+273.15}-\frac{1}{25+273.15}\right)} \quad \text{(eq. 25)}$$

Where R_{NTC} is external NTC resistor, $R_{NTCat25}$ is NTC resistor value at 25 Celsius degree and $B_{25/50}$ is NTC resistor B value.

Table 4 shows warning and protection temperature where will be varied according to tolerance of R_p, R_{NTC} and I_{NTC}.

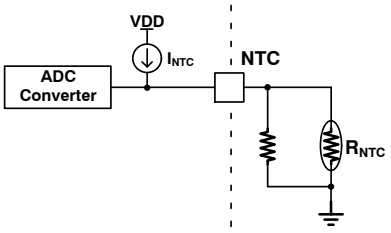

Figure 16. NTC Circuit Diagram

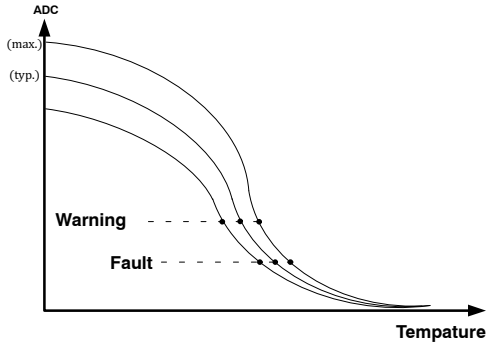

Figure 17. ADC v.s Temperature

Table 4. EXTERNAL OVER TEMPERATURE PROTECTION THRESHOLD

Message	Threshold min./typ./max.	Setting
Warning	94/101/108°C	R_p = 20 kΩ@25°C R_{NTC} = 100 kΩ±1%@25°C ($B_{25/50}$ = 4300 k±1%)
Fault	105/112/119°C	

Cable Fault

In order to avoid the cable line melting caused by the pollution such as low impedance across ground to BUS, FAN6390MPX implement USB BUS line impedance detection. During the $t_{CC\_DEBOUNCE}$ which is debounce time detecting cable attach status, it starts Bus line impedance detecting. If low impedance, less than 2 kΩ, status is measured at the output terminal FAN6390 will enter Auto Restart Mode so the load switch will not turn on. Accordingly no power will be delivered to output side and ensure total system safe.

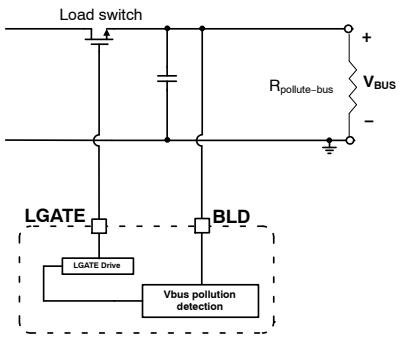

Figure 18. USB Connector Impedance Detection

Compensation Network Design

Since FAN6390MPX support constant current control as well as constant voltage control, compensation network design should consider both controls. Typically two−pole one−zero networks are fine for both constant voltage and constant current controls. In order to fine tune compensation network for better performance, however, many customers selects to add more poles and zeros. This application notes introduces design method not only two−pole one−zero compensation, but compensation networks incorporating more poles and zeros. Figure 19 illustrates feedback network which incorporates two−pole one−zero network. Figure 21 shows a network implementing more poles and zeros.

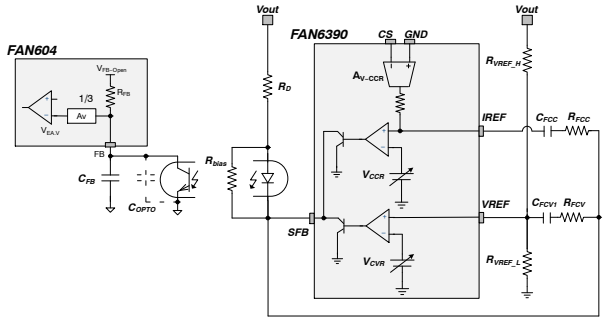

Figure 19. Two−pole One−zero Compensation Network for CV and CC Control

Where, C_{FCV1} and R_{FCV} contribute CV control and C_{FCC} and R_{FCC} contribute CC control.

$$G_{FCV}(s) = \frac{\left(\frac{s}{\omega_{cv\_z1}} + 1\right)}{\frac{s}{\omega_{cv\_p1}}\left(\frac{s}{\omega_{cv\_p2}} + 1\right)} \quad \text{(eq. 26)}$$

$$\omega_{cv\_p1} = \frac{CTR \times R_{FB}}{C_{FCV1} \times R_D \times R_{VREF-H}}$$

$$\omega_{cv\_p2} = \frac{1}{(C_{FB} + C_{OPTO}) \times R_{FB}}$$

$$\omega_{cv\_z1} = \frac{1}{C_{FCV1} \times (R_{VREF-H} + R_{FCV})}$$

$$G_{FCC}(s) = \frac{\left(\frac{s}{\omega_{cc\_z1}} + 1\right)}{\frac{s}{\omega_{cc\_p1}}\left(\frac{s}{\omega_{cc\_p2}} + 1\right)} \quad \text{(eq. 27)}$$

$$\omega_{cc\_p1} = \frac{CTR \times R_{FB}}{C_{FCC} \times R_D \times R_{IN.CC}/R_{CS}}$$

$$\omega_{cc\_p2} = \frac{1}{(C_{FB} + C_{OPTO}) \times R_{FB}}$$

$$\omega_{cc\_z1} = \frac{1}{C_{FCV1} \times (R_{VREF-H} + R_{FCV})}$$

Eq. 26 and eq. 27 are transfer functions of feedback compensation for CV and CC controls, respectively. Since $R_{IN.CC}/R_{cs}$ is much larger than R_{VREF-H}, the first pole and the zero of CC control are positioned at lower frequency than CV control. The other poles of CC and CV controls are positioned at the same frequency. Figure 20 shows typical plots of CV and CC controls.

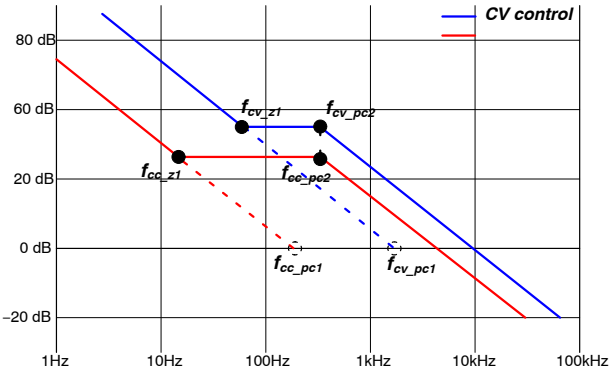

Figure 20. Bode Plot of Two−pole One−zero Compensation Network for CV Control

In order to improve performance such as output ripple in burst mode operation and dynamic response, more poles and zeros can be added as Figure 21. C_{FCV2} adds one pole and one zero for CV control. C_D incorporates one zero for CV and CC controls.

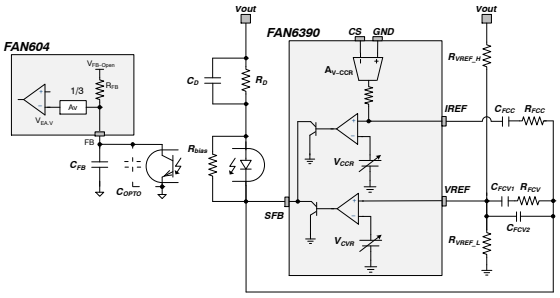

Figure 21. Compensation Network Incorporating more Poles and Zeros

Where, C_{FCV1}, C_{FCV2} and R_{FCV} contribute CV control and C_{FCC} and R_{FCC} contribute CC control

$$G_{FCC}(s) = \frac{\left(\frac{s}{\omega_{cc\_z1}} + 1\right)\left(\frac{s}{\omega_{cc\_z2}} + 1\right)}{\frac{s}{\omega_{cc\_p1}}\left(\frac{s}{\omega_{cc\_p2}} + 1\right)} \quad \text{(eq. 28)}$$

$$\omega_{cc\_p1} = \frac{CTR \times R_{FB}}{C_{FCC} \times R_D \times R_{IN.CC}/R_{CS}}$$

$$\omega_{cc\_p2} = \frac{1}{(C_{FB} + C_{OPTO}) \times R_{FB}}$$

$$\omega_{cc\_z1} = \frac{1}{C_D \times R_D}$$

$$\omega_{cc\_z2} = \frac{1}{C_{FCC} \times (R_{IN.CC}/R_{CS} + R_{FCC})}$$

$$G_{FCV}(s) = \frac{\left(\frac{s}{\omega_{cv\_z1}} + 1\right)\left(\frac{s}{\omega_{cv\_z2}} + 1\right)\left(\frac{s}{\omega_{cv\_z3}} + 1\right)}{\frac{s}{\omega_{cv\_p1}}\left(\frac{s}{\omega_{cv\_p2}} + 1\right)\left(\frac{s}{\omega_{cv\_p3}} + 1\right)} \quad \text{(eq. 29)}$$

$$\omega_{cv\_p1} = \frac{CTR \times R_{FB}}{(C_{FCV1} + C_{FCV2}) \times R_D \times R_{VREF-H}}$$

$$\omega_{cc\_p2} = \frac{1}{(C_{FB} + C_{OPTO}) \times R_{FB}}$$

$$\omega_{cc\_p3} = \frac{C_{FCV1} + C_{FCV2}}{C_{FCV1} \times C_{FCV2} \times R_{FCV}}$$

$$\omega_{cc\_z1} = \frac{1}{C_D \times R_D}$$

$$\omega_{cc\_z2} = \frac{b - \sqrt{b^2 - 4ac}}{2a}$$

$$\omega_{cc\_z3} = \frac{b - \sqrt{b^2 - 4ac}}{2a}$$

where,

$a = R_{FCV} \times R_{VREF-H} \times C_{FCV1} \times C_{FCV2}$

$b = R_{VREF-H} \times C_{FCV1} \times R_{VREF-H} \times C_{FCV2} + R_{FCV} \times C_{FCV1}$

$c = 1$

C_D adds one zero for CC control loop as well as CV control loop. The added zeros enhance bandwidth of CV and CC control loops. C_{FCV2} can control phase margin at nearby bandwidth frequency, and it helps to improve stability. In order to design overall system compensation loop, control−to−output transfer function is required. It can refer AN−4193, the Design Guideline for Flyback Travel Adapter using FAN604.

VS Resistor Array Design Guideline of Primary Side Controller

FAN604 series, Fairchild Offline Quasi−Resonant PWM Controller, monitors output voltage through Voltage Sense (VS) pin. Below eq. 30 shows the relationship between output voltage and VS pin voltage.

$$\frac{R_{VS\_H}}{V_{VS\_L}} = (V_{BUS-Foldback} + V_F) \times \frac{N_{AUX}}{N_{SEC}} \times \frac{R_{VS\_L}}{R_{VS\_H} + R_{VS\_L}} - 1 \quad \text{(eq. 30)}$$

Where, V_F is voltage drop on SR MOSFET, N_{AUX} is the number of turns on auxiliary winding, N_{SEC} is the number of turns on secondary winding, R_{VS_H} is the upper side resistor on VS pin, and R_{VS_L} is the lower side resistor on VS pin and $V_{BUS\_Foldback}$ is a target foldback level of output.

As the minimum PPS voltage is 3.3 V(typ.) and V_{IN-OFF} is 3.0 V(max.) as UVP threshold in PPS mode. Following Eq. 31 we design 2.7 V as primary fold back level which is lower than V_{IN-OFF} to ensure PPS operation range.

$$\frac{R_{VS\_H}}{V_{VS\_L}} = (2.7\ V + 0.15\ V) \times \frac{N_{AUX}}{N_{SEC}} \times \frac{1}{V_{S-UVP-L}} - 1 \quad \text{(eq. 31)}$$

PCB Layout Recommendation

Printed Circuit Board (PCB) layout and design are very important for switching mode power supplies where the voltage and current change with high speed. Good PCB layout minimizes Electro−Magnetic Interference (EMI) and prevents excessive noise from surge or Electro−Static Discharging (ESD). As shown in Figure 22, the main power flows through Load Switch, R_{SENSE}, and SR MOSFET. It is recommended that Y−cap is directly connected to power ground.

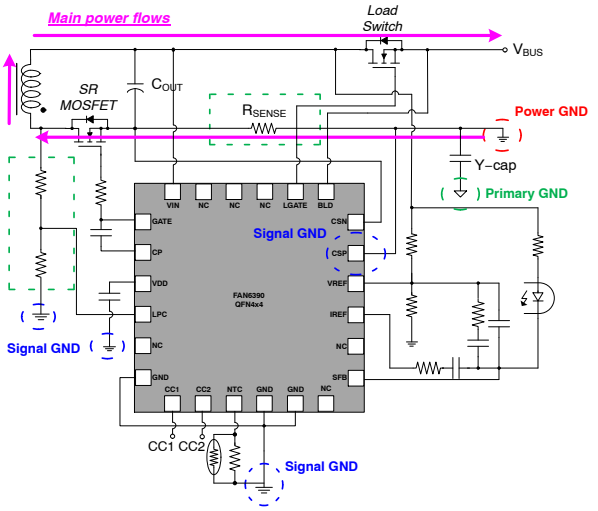

Figure 22. Power Ground and Signal Ground

1. *Sensing Resistor Layout Guide Line*
   The sensed voltage via R_{SENSE} is very small value. In order to avoid offset voltage or avoid inducing switching noise on the sensed voltage, RSENSE should be connected between ground of C_{OUT2} and power ground. And R_{SENSE} should be positioned as close as possible to CS pin and GND pin. Figure 22 and Figure 23 show some examples of good and bad connections.

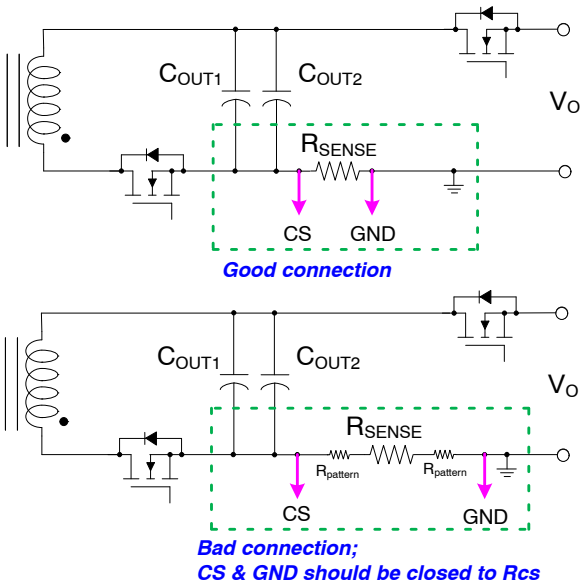

Figure 23. Examples of Sensing Resistor Connections

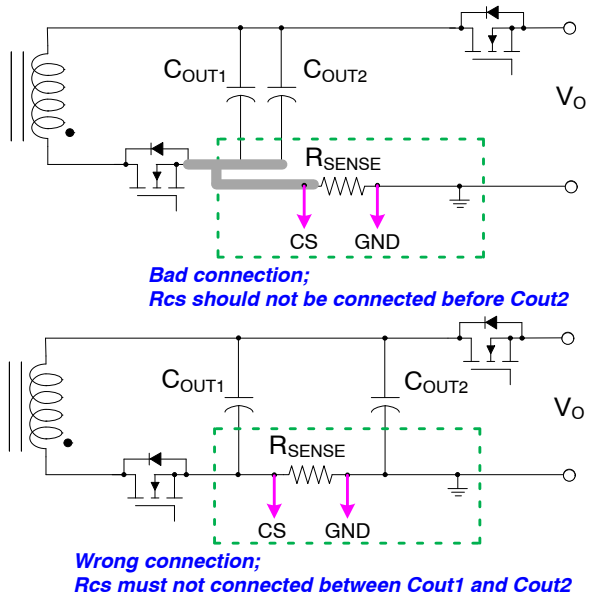

Figure 24. Examples of Sensing Resistor Connections

If synchronous rectifier is not enabled normally even though output load condition is much larger than green mode level, the PCB layout for R_{SENSE} should be improved. If it is difficult to improve more due to PCB layout limitation, it is recommended to add RC filter on CS pin as Figure 25. Typically $R_{CS-filter}$ 1 kΩ and $C_{CS-filter}$ 1 nF are recommended.

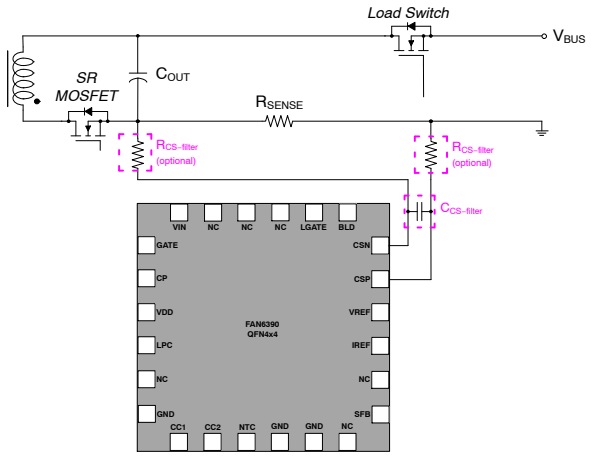

Figure 25. RC filter on CS pin

Switching Noise Avoid Layout Guide Line

Switching noise interfere Synchronous Rectifier operation. In order to avoid interference, R_{LPC-H} and R_{LPC-L} should be positioned close to FAN6390, and power path should be apart from LPC path. Figure 27 shows bad PCB layout example for LPC resistor array. R_{LPC_H} is positioned on the bottom layer and FLY− pattern is positioned on the top layer. FLY− pattern is overlapped with R_{LPC_H}. This PCB layout makes abnormal operation of synchronous rectifier. Based on the same idea, the GATE driving path shouldn't overlap with feedback voltage reference and current reference path as well.

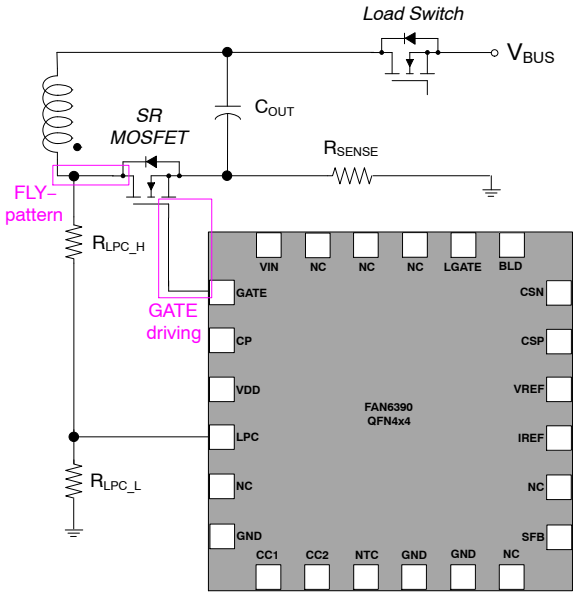

Figure 26. LPC Resistor Array Circuit Diagram

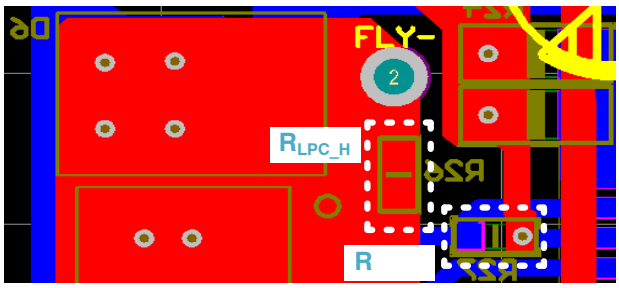

Figure 27. Bad PCB Layout Example; Overlap between Power Pattern (FLY−) and the Upper Side Resistor (R_{LPC_H}) Layout

Figure 28 shows good PCB layout example for LPC resistor array. R_{LPC_H} and R_{LPC_L} are positioned on the bottom layer, and there is no overlap between LPC resistor array layout and power signal patterns.

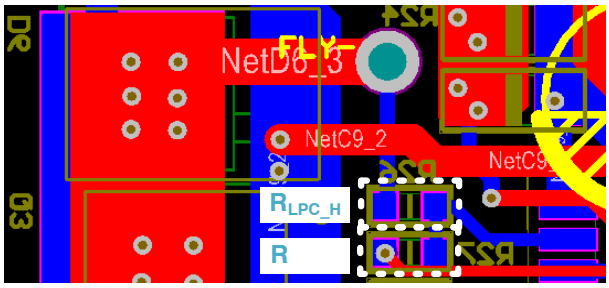

Figure 28. Good PCB Layout Example; No overlap between Power Signal Patterns and LPC Resistor Array (R_{LPC_H} & R_{LPC_L}) Layout

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