VE-Trac™ Dual Technical Guide

AND9988/D

This document is intended to be a guide to explain the technical details of the product features and capabilities. It is also designed to provide reference circuits and application related notes to ensure that the product is used in an optimal manner for its intended end use.

APPLIES TO THE FOLLOWING PARTS

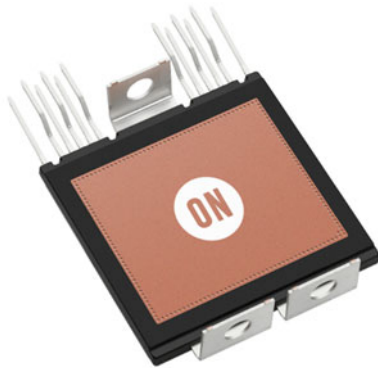|	
NVGxxxA75L4DSxx	750V FS4 family
NVG450A120L5DSx	1200V UFS family

Figure 1. Shunt Type Switch

INTRODUCTION

The VE−Trac Family of power modules is an automotive qualified line of products specifically designed for EV−traction inverters. The product line is broadly classi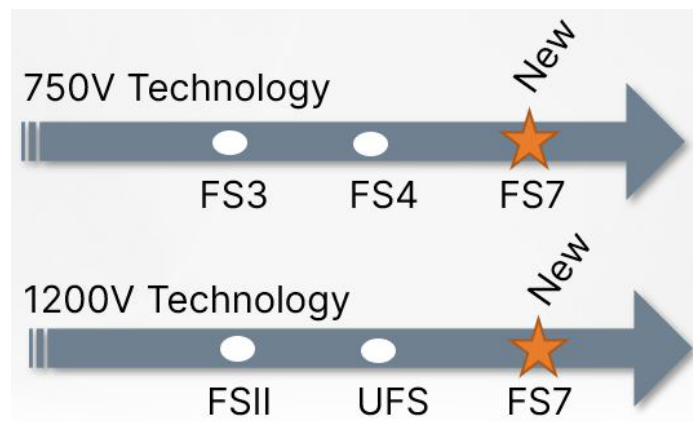fied into two platforms (i) Dual (ii) Direct. Each platform has its own advantages, but this document's scope is limited to understanding the datasheet parameters and device characteristics of the Dual product line. It also includes a design guide and recommendations for using the product effectively. A separate document 'VE−Trac Dual Assembly Guide' provides details related to assembling the power module in an assembly.

VE−Trac Dual product features:

- Transfer molded packaging offers the possibility of low $/kW option.
- Continuous 175°C operation enables higher power density.
- Wire bond free package improves reliability.
- On−chip current sense offers faster and simpler OCP implementation.
- On−chip temperature sense enables faster response and closer to true T_{vj}
- Scalability – simpler mechanical layout for paralleling modules

TECHNICAL DETAILS

onsemi's latest generation of IGBTs and Diodes are incorporated into the VE−Trac products. The 1200 V VE−Trac products use the FSII IGBT technology and the 750 V products use the latest 4th Generation of IGBTs from **onsemi**.

Chip Technology in VE−Trac modules

Figure 2. Chip Technologies

This new generation of Field Stop (FS) IGBTs with a high density cell structure and an optimized double layer shows remarkable device performance under static and dynamic conditions with strong latch−up ruggedness. The design of the chip uses sub−micron trench and mesa active with a narrow mesa width.

Package Design

The VE−Trac Dual is a dual side cooled package i.e. it is necessary to actively cool both sides of the package to get maximum performance from the module. It uses a flip−chip arrangement with a heat spreading spacer over the collector, sandwiched between two DBCs, as shown in Figure 3.
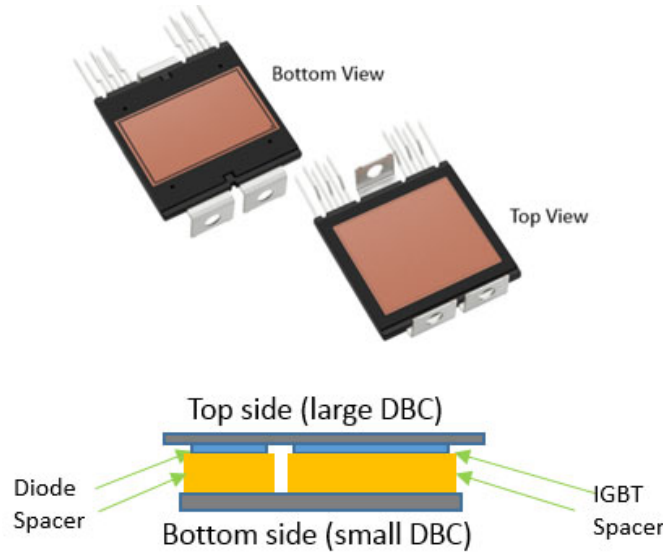

Figure 3. Illustration of Dual Side Cooling Concept

The DBC material uses Zirconia toughened Al_2O_3 for top and bottom to electrically isolate the devices from the cooler. The signal leads and terminals are oxygen free copper with tin electro−plating. An epoxy mold compound (EMC) is used to further isolate the module and provide mechanical robustness. All materials used in the power module meet UL flammability rating class 94V−0. All VE−Trac Dual modules have a common pin−out assignment as shown in Figure 4.

Pin #	Pin	Pin Function Description
1	N	Low Side Emitter
2	P	High Side Collector
3	H/S COLLECTOR SENSE	High Side Collector Sense
4	H/S CURRENT SENSE	High Side Current Sense
5	H/S EMITTER SENSE	High Side Emitter Sense
6	H/S GATE	High Side Gate
7	H/S TEMP SENSE (CATHODE)	High Side Temp sense Diode Cathode
8	H/S TEMP SENSE (ANODE)	High Side Temp sense Diode Anode
9	~	Phase Output
10	L/S CURRENT SENSE	Low Side Current Sense
11	L/S EMITTER SENSE	Low Side Emitter Sense
12	L/S GATE	Low Side Gate
13	L/S TEMP SENSE (CATHODE)	Low Side Temp sense Diode Anode
14	L/S TEMP SENSE (ANODE)	Low Side Temp sense Diode Cathode
15	L/S COLLECTOR SENSE	Low Side Collector Sense

Figure 4. Pin Assignments for all VE−Trac Dual Modules

One of the advantages of the Dual package design is its low parasitic inductance. Ls_{CE} is the parasitic stray inductance between the high side collector and the low side emitter. The precise value is provided in the data sheet for each specific module. The measurement is made according to IEC 60747−15. A typical measurement circuit is shown in Figure 5, where Ls_{CE} is equal to $V_{step} / (\Delta i_{DUT}$ between t2 and t1 / (t2 − t1)).
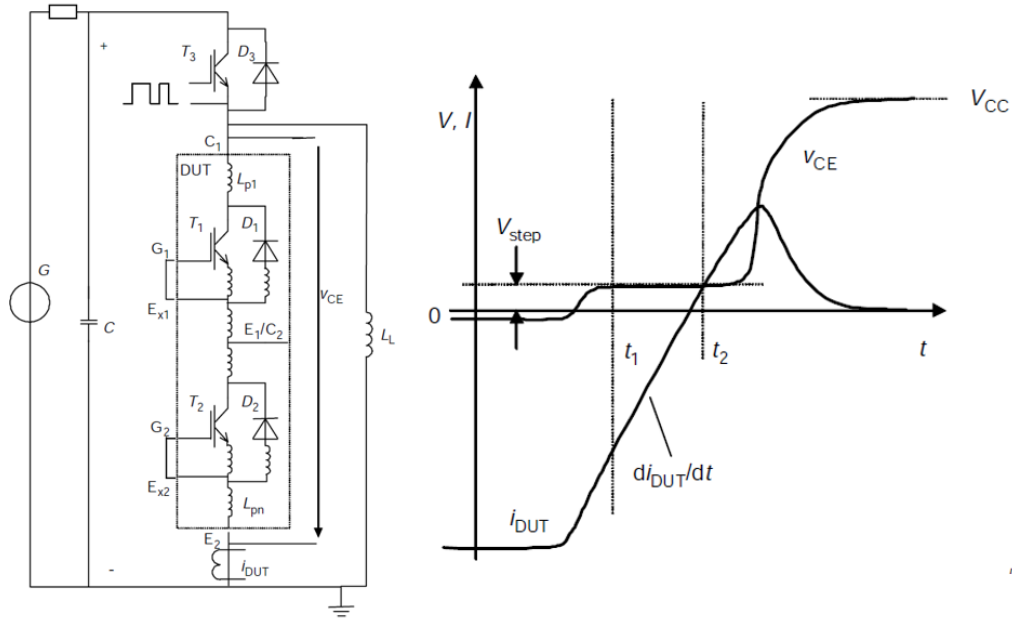
Figure 5. Parasitic Stray Inductance Measurement Circuit as Shown in IEC 60747−15

Creepage and Clearance

All VE−Trac Dual modules comply with the required creepage and clearance distances as summarized in the table below. The module offers basic isolation, pollution degree 2 and a Comparative Tracking Index (CTI) value > 600.

Table 1. CREEPAGE AND CLEARANCE PARAMETERS

Parameter	Value
CLEARANCE POWER TERMINAL – POWER TERMINAL	3.4 mm
CLEARANCE POWER TERMINAL – SIGNAL PIN	3.1 mm
CLEARANCE SIGNAL PIN – SIGNAL PIN	3.0 mm
CLEARANCE SIGNAL PIN – REF. COOLER	10.2 mm
CLEARANCE POWER TERMINAL – REF. COOLER	7.0 mm
CREEPAGE POWER TERMINAL – POWER TERMINAL	6.2 mm
CREEPAGE SIGNAL PIN – SIGNAL PIN	5.8 mm
CREEPAGE POWER TERMINAL – SIGNAL PIN	5.9 mm
CREEPAGE POWER TERMINAL – REF. COOLER	5.22 mm
CREEPAGE SIGNAL PIN – REF. COOLER	5.22 mm

Table 1 summarizes the creepage and clearance distances between the various pins of the module and also between the reference cooler to the different module pins. Figure 6 illustrates the various distances noted in Table 1. Great care should be taken not to violate the minimum clearance and creepage requirements when assembling the power module to heatsinks and using fasteners to secure cables or bus bars to the module terminals. Please refer to the 'Assembly Guide' for details and check the specific data sheet of your product for exact values.
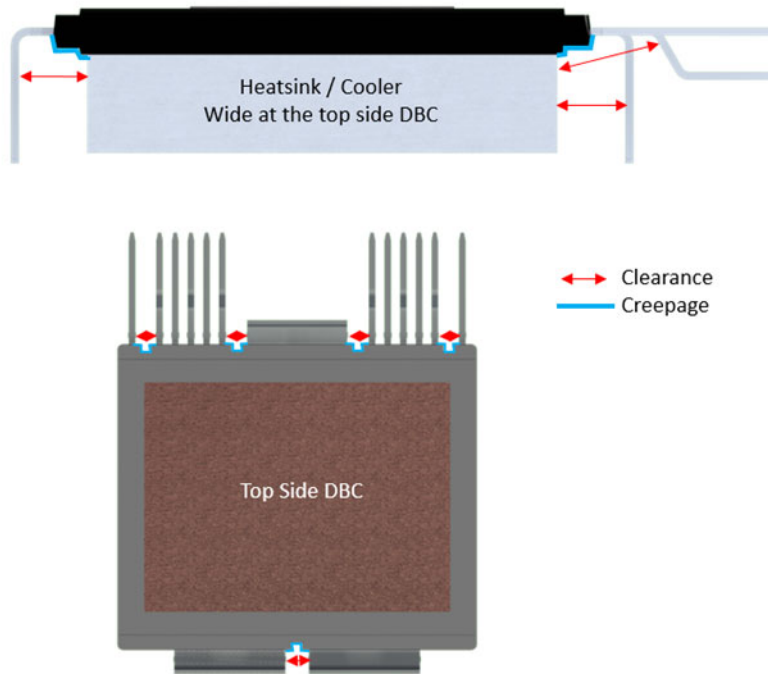
Figure 6. Illustration of the Creepage and Clearance Distances

THERMAL PERFORMANCE

Double sided cooling offers unmatched performance and power density in the end application. Below are thermal parameters as shown in the data sheet:

Table 2. EXAMPLE THERMAL PARAMETERS AS SHOWN IN THE DATASHEET FOR VE−Trac DUAL PRODUCTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
IGBT.$R_{th,J-C}$	Effective Rth, Junction to Case	-	0.06	tbd	°C/W
IGBT.$R_{th,J-F}$	Effective Rth, Junction to Fluid, λ_{TIM}=6 W/m-K, F=660N 8L/min, 65°C, 50/50 EGW, Ref. Heatsink		0.13	tbd	°C/W
Diode.$R_{th,J-C}$	Effective Rth, Junction to Case	-	0.11	tbd	°C/W
Diode.$R_{th,J-F}$	Effective Rth, Junction to Fluid, λ_{TIM}=6 W/m-K, F=660N 8L/min, 65°C, 50/50 EGW, Ref. Heatsink		0.23	tbd	°C/W

Since the power dissipation is uneven through the top and bottom side of the power module the Rth_{J-C} and Rth_{J-F} values noted in the data sheets are the total equivalent measured values for the power module. The Rth_{J-F} is measured using a reference cooler and will vary with different heatsink designs, flow rate, coolant temperature, coolant type and clamping force.

Thermal Measurements

Unlike conventional single side direct cooled module, the Dual module dissipates the heat from top and bottom side. The heatsink for the Dual module is shown in Figure 7. This reference heatsink made with pin−fin structure balances high thermal performance with the need to maintain low pressure drop.

The Dual module has a DBC on both TOP and BOT side, so in addition to the Zth_{J-F}, the thermal resistance from junction to case can be measured. The thermal resistance of the IGBT or diode is defined as:

$$R_{th-JC} = \frac{T_J - T_C}{P_V} \qquad \text{(eq. 1)}$$

The Rth_{J-C} of the IGBT and diode are measured by Thermal Dual Interface Method (TDIM). The Thermal impedance measurements were carried out using a MicRed Power tester. Due to the presence of the spacer the heat dissipation is not symmetrical for top and bottom substrates. This additional spacer between die and substrate increases Rth_{J-C} for that side. The equivalent Rth_{J-C} of the die is calculated by paralleling the Rth_{J-C}, TOP and Rth_{J-C}, BOT.

$$R_{thj-c}(DSC) = \frac{R_{th-JC,TOP} \cdot R_{th-JC,BOT}}{R_{th-JC,TOP} + R_{th-JC,BOT}} \qquad \text{(eq. 2)}$$

Where Rth_{J-C},TOP is the thermal resistance from junction to top substrate and Rth_{J-C},BOT is the thermal resistance from junction to bottom substrate.

The Rth_{J-C} can be extracted by the TDIM method. The TDIM method requires two thermal impedance curves. These are measured in two steps.

      a. Thermal impedance from junction to fluid (Rth_{J-F}) is measured by using a thermal interface material (TIM) between the module and the heatsink.

      b. In the second step, Rth_{J-F} is measured without a TIM between the module and the heat sink.

The point of separation of these two curves gives the equivalent Rth_{J-C}. In a similar way thermal resistance from junction to the top substrate (Rth_{J-C},TOP) and the bottom substrate (Rth_{J-C},BOT) are measured.

The VE−Trac Dual module was mounted onto liquid cooled heatsink with a TIM material, a clamping torque of 1 Nm is applied to the heatsink terminals to generate the 660N of clamping force and this ensures optimal thermal contact between the module and the heatsink. Note that the torque specification will vary with different heatsink designs. The TIM material chosen is Honeywell PTM 7000, it is a phase change material with a thermal conductivity of 6.5 W/m.K. The material is available in paste or pad form and all the measurements are done with the 200 μm pad die cut to the required specifications in the 'Assembly Guide'. The mounting instructions and screwing sequence for the Dual modules are shown in Figure 7.
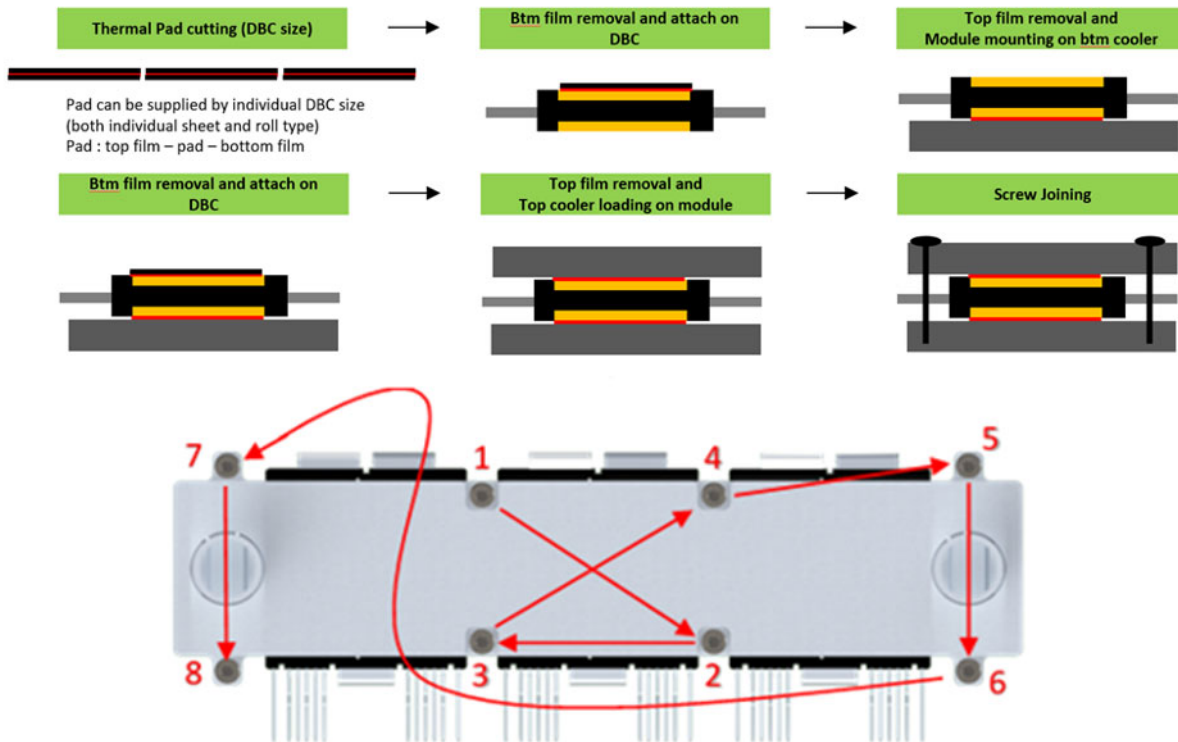

Figure 7. Thermal Measurement Setup and Sequence

To obtain the impedance curves, a heating current (250 − 400 A depending on chip size) with a sense current of 100 mA (I_M) is applied to the device under test (DUT), until it reaches to the thermal steady state condition (30 sec). During the heating phase, the collector emitter voltage drop is monitored which is used to calculate the heating power of the IGBT or the diode. Once the module reaches the thermal steady state condition, the heating current is switched off or reduced to the level of sense current I_M. The corresponding voltage variations (Vce, Vf) of the DUT are recorded by MicRed Power tester. The electrical disturbances at the beginning of the measurements (voltage transients) were corrected by the T3ster master software. The cooling transient curves of the IGBT and diode are then converted into junction temperatures by the following equations:

$$V_{TSP}(T) = -\frac{T_{VJ}}{K_{IGBTV} \text{ or } K_{Diode}} + V_o \qquad \text{(eq. 3)}$$

$$Z_{jF}(t) = \frac{T_J(t) - T_C}{P_H} \qquad \text{(eq. 4)}$$

Here Tc is considered as inlet Fluid temperature. The cooling curves of an IGBT and diode, are the collector emitter voltage (Vce) and forward voltage drop (Vf) as a function of Junction temperatures. The calibration curve of the IGBT is obtained by heating up the Dual module from 20°C to 120°C at a constant sense current of 100 mA (I_M) and a gate emitter voltage (V_{GE}) of 15 V. The corresponding thermal curves and structure functions for the IGBT and diode are shown below:
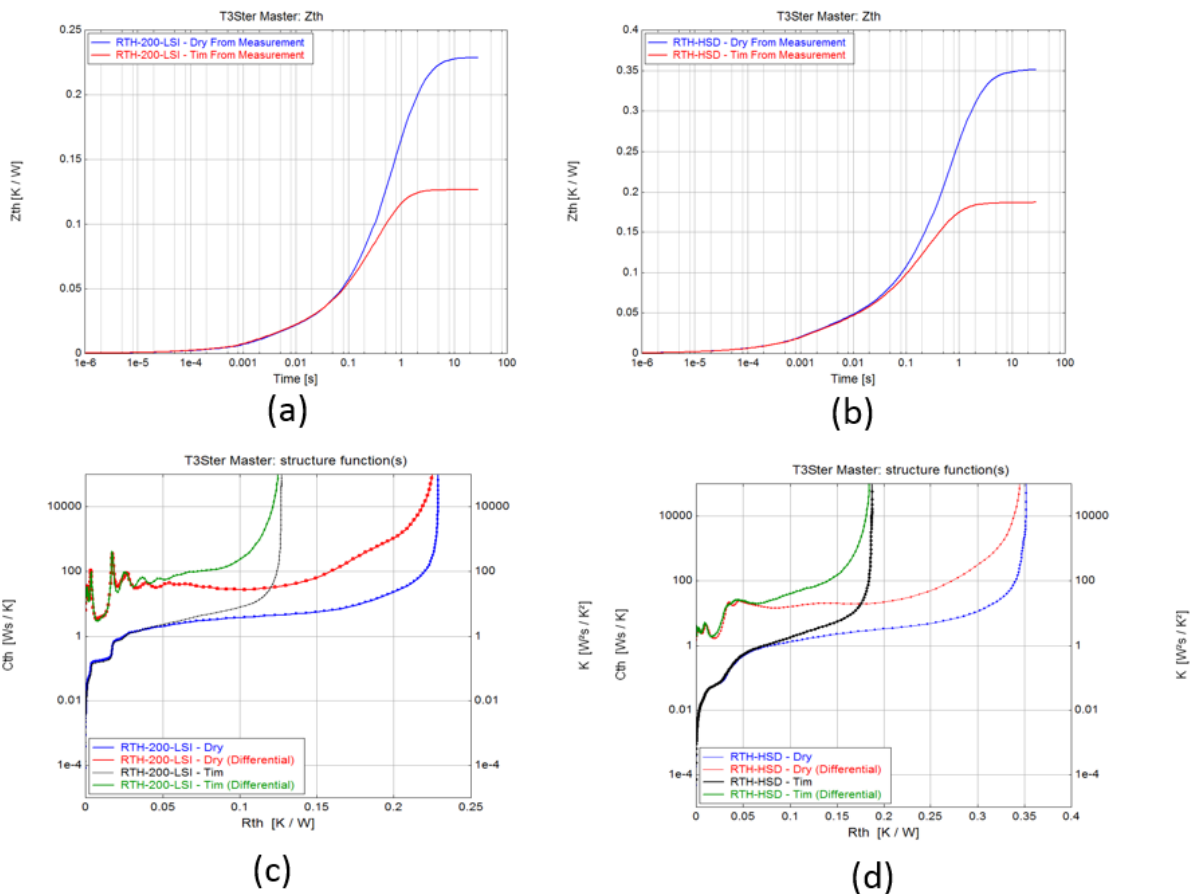

Figure 8. (a) Thermal impedance for IGBT (a) and Diode (b) with and without TIM with the Corresponding Structure Functions for the IGBT(c) and Diode (d)

The point of separation of the two impedance curves (with TIM and Without TIM) defines the Rth,J−C. The detailed explanation of the measuring Rth,J−C is explained in JESD51−14−JEDEC standard. The transient thermal impedance of IGBT or diode are specified using structure functions shown in Figure 8. In general, the thermal capacitance of a structure function represent the heat propagating into a material layer of certain volume and the thermal resistance remains relatively constant. The increase in thermal resistance, indicates the heat crossing a boundary between two layers of different thermal properties.

Thermal Modeling

The information needed to develop circuit level or mathematical model for the power module is provided below. This includes the equivalent thermal impedance and

thermal capacitance for a Foster thermal network for the electrical equivalent models and math expressions. The information provided in the table below is also provided in the respective data sheet for the product. The table also includes the cross coupling thermal resistance between the IGBT and the free−wheeling diode (FWD) for the same side

and also to the opposing side. It also shows the values between the high side IGBT and the low side IGBT devices. The strongest coupling to consider is between the IGBT and its FWD. Consult application note on thermal modeling for more accurate Foster network for specific products.

Table 3. EQUIVALENT FOSTER THERMAL NETWORK FOR THE 750V, 800A VE−TRAC DUAL

Nodes	IGBT		Diode	
	Rth	Cth	Rth	Cth
Node 1	0.01	0.04	0.08	1.61
Node 2	0.06	15.84	0.02	413.18
Node 3	0.01	0.54	0.03	0.05
Node 4	0.05	3.50	0.09	9.53
Total	0.13	19.91	0.23	424.38
x−coupling Rth IGBT <−> Diode IGBT <−> IGBT	0.021 (same side) n/a		0.005 (opposing side) 0.007 (opposing side)	

ELECTRICAL PERFORMANCE

This section explains the maximum, static and dynamic electrical parameters of the IGBT and Diode inside the module. Maximum values of these parameters should not be exceeded, otherwise it will cause damage to the semiconductor. In addition, please note that the temperature condition is 25°C, unless it is specified otherwise.

Maximum Ratings − IGBT

Operating Junction Temperature, T_{vj}

This is the junction temperature range where the device is guaranteed to operate without physical or electrical damage. Unlike other competing modules that include a continuous rating and a temporary higher rating, VE−Trac Dual specifies a single temperature range for continuous operation. T_{vj} range −40°C to 175°C.

Safe Operating Area of IGBT

The maximum allowed peak Collector to Emitter Voltage (V_{CES}) is specified at a junction temperature of 25°C. Please

note this value has a positive temperature coefficient, meaning at lower temperatures the maximum allowed peak Collector to Emitter is also lower. There are two plots in the data sheet that should be checked to ensure safe operation of the module. The first plot is the Maximum V_{CE} rating over temperature as shown in Figure 9b. This determines the absolute maximum allowed peak blocking voltage between the IGBT Collector−Emitter across the operating temperature range. Note that at −40°C the maximum V_{CE} rating is 715 V.

The second plot to consider is the Reverse Bias Safe Operating Area (RBSOA). This shows the peak V_{CE} allowed as a function of collector current at 150°C for the power module (see Figure 9a). It shows the ideal SOA for the chip and also the module, which includes the module parasitic inductance. However, it's important to also consider all the parasitic inductance in the power loop to determine the true SOA for the module in the end application.
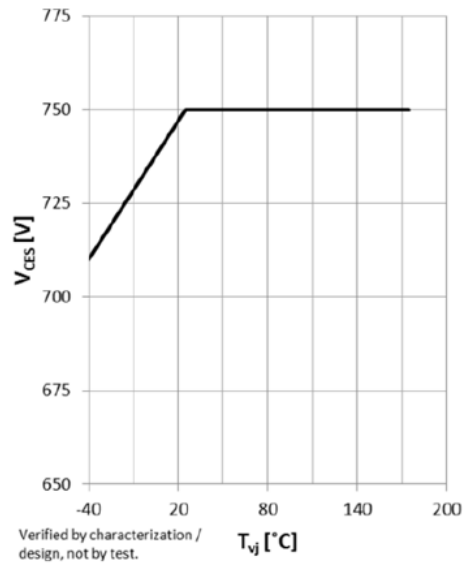
Reverse Bias Safe Operating Area
$V_{GE} = +15/-8V, R_{Goff} = 15\Omega, T_{vj}=150°C$
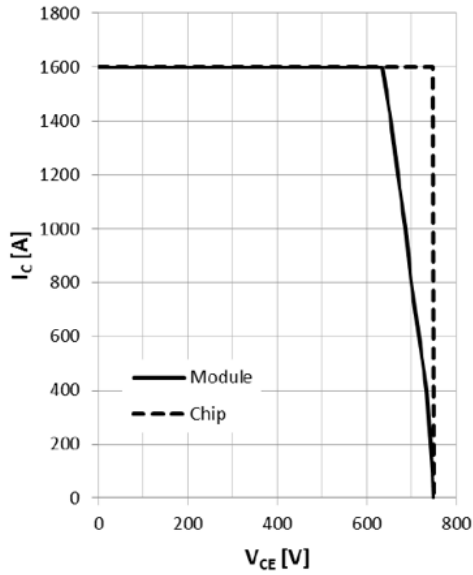
Maximum allowed Vce
$I_{CES}=1mA, T_{vj} \leq 25°C; I_{CES}= 30mA, T_{vj}> 25°C$

(a)

(b)

Figure 9. RBSOA (a) and Vce versus Temperature (b) plot for the 750 V, 800 A Module

Lastly, the SOA plot should be checked for pulsed application. The IGBT module must not be used in the linear mode. This plot is not included in the data sheet. Figures 10 and 11 shows the plot for the different module types.
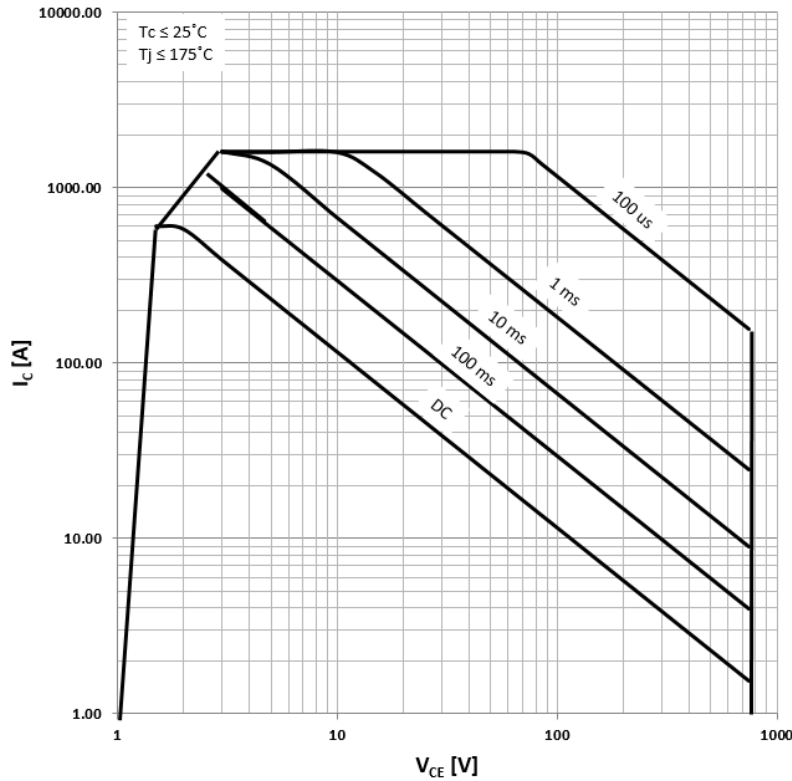
Figure 10. SOA for 750 V, 800 A Power Module
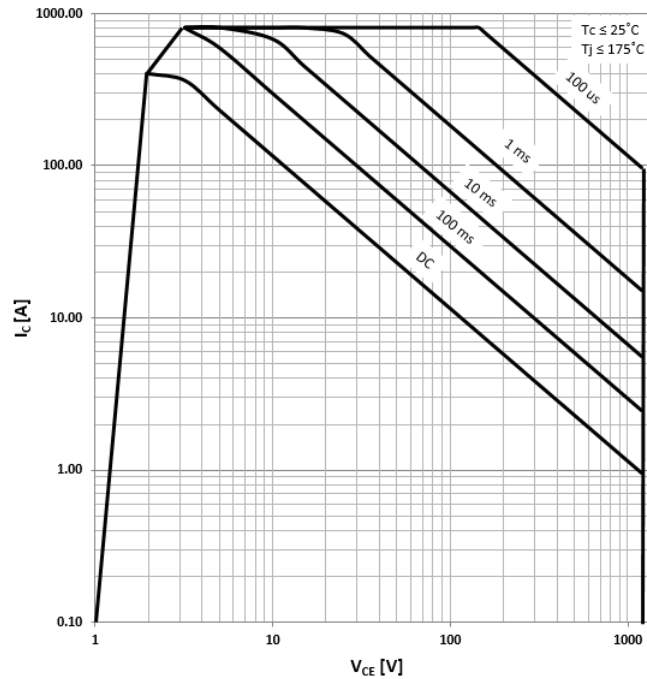
Figure 11. SOA for 1200 V, 400 A Power Module

Continuous DC Collector Current, Ic nom

The Continuous DC Collector is continuous DC current allowed when using the reference heatsink which results in $R_{th,J-F}$ value specified in the data sheet. Ic nom is determined by three factors: Vcesat(as a function of T_{vj} and Ic), IGBT Junction to Fluid thermal resistance $R_{th,j-f}$ and Max Operating Junction temperature. A design margin is also applied to determine the final Ic nom value and it is verified by characterization testing where Tvj is determined according to IEC60747−15.

Maximum Pulsed Collector Current, ICRM

VE−Trac Dual modules specify ICRM as 2X of IGBT rating current at room temperature. When the fluid temperature is higher, pulse width should be determined by power dissipation and transient thermal impedance Zth to make sure Tvj is not exceeding 175°C.

Short Circuit Withstand Time, SCWT

SCWT of VE−Trac Dual modules is specified and verified according to AQG324 Type 1 short circuit (HSF:hard−switch−fault), while the modules also passed Type 2 short circuit. The short circuit characteristics depend heavily on application specific parameters such as temperature, stray inductances/resistance and gate driver. During a short circuit event, the IGBT has to withstand high junction temperature due to high power dissipation and turns off safely. Below figures show short circuit test setup.
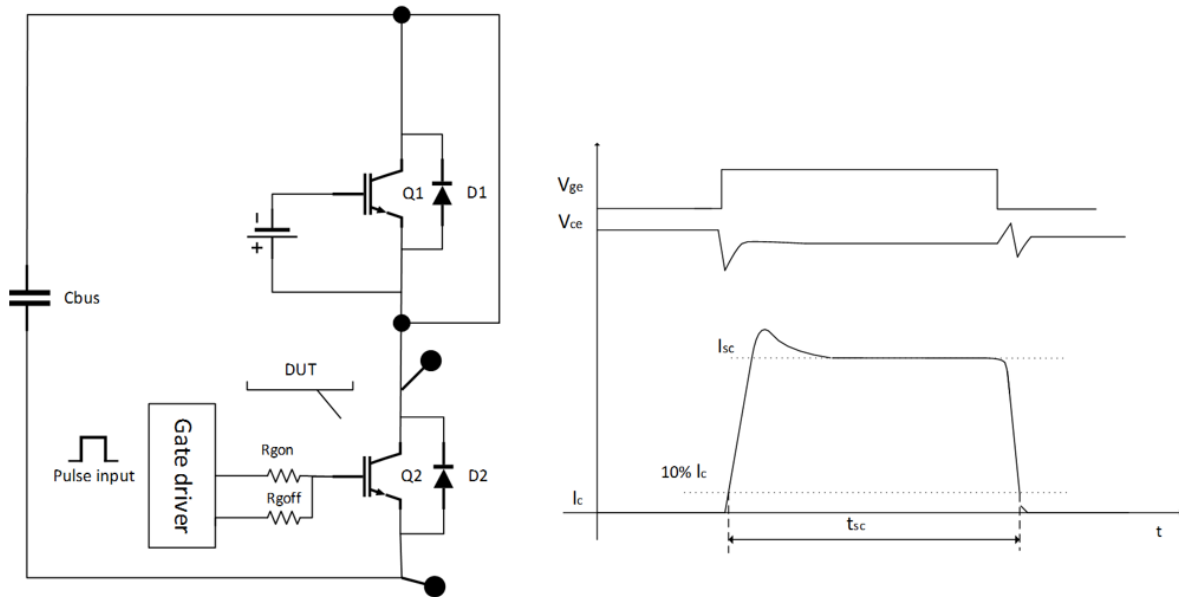
Figure 12. Short Circuit Measurement Circuit and SCWT is Defined as Time Interval from 10% Rising Edge Isc to 10% Falling Edge

Maximum Ratings – Diode

Repetitive Peak Voltage, VRRM

VRRM Voltage is max allowed reverse biased voltage for the diode. As IGBT and Diode are anti−parallel connected, diodes have to withstand the same voltage as the IGBT. The collector−Emitter voltage ratings in the data sheet will also apply for the anti−parallel diode.

Continuous Forward Current, I_F

Similar method of rating as the IGBT Ic nom. The continuous DC current rating for the diode is a little lower than the IGBT due to the higher $R_{th,J-F}$ value specified in the data sheet for the Diode. I_F value and it is verified by characterization testing where junction temperature is determined according to IEC60747−15.

Repetitive Peak Current, I_{FRM}

VE−Trac Dual modules specify I_{FRM} as 2X of I_{FN}. When the fluid temperature is higher, pulse width should be determined by power dissipation and transient thermal impedance Zth to make sure the Junction temperature is not exceeding 175 °C

Surge Current Capability, I^2t value

Diode surge current is in the form of a half sine wave of 10ms or 8.3ms (50 or 60Hz), where its peak current is denoted as I_{surge}. The device is able to withstand this current without being damaged in the event of malfunctions provided this does not occur too often in the diode service life. Instead of peak current, the datasheet specifies this characteristic in the form of I^2t value, given by:

$$\int_0^{tp} Idt = I_{surge}^2 * \frac{tp}{2} \qquad \text{(eq. 5)}$$

Where t_p is the pulse width.

Static Characteristics

IGBT Output characteristics, Vcesat

Vcesat is the voltage drop across collector to emitter for a specified gate voltage and temperature which is used to calculate IGBT's conduction losses and compare the losses from different suppliers. It is a temperature dependent parameter, as shown in Figure 13. Above the crossover, Vcesat exhibits positive temperature coefficient while below the crossover, it shows negative temperature coefficient. Positive temperature coefficient is beneficial in a way that it helps achieve better current sharing for paralleling operation.

Collector to Emitter Leakage Current, I_{CES}

I_{CES} is the leakage current from collector to emitter when IGBT is turned off. It is highly related to the IGBT chip size and features a positive temperature coefficient −−− I_{CES} increases when temperature is increasing.

Gate to Emitter leakage current, I_{GES}

The absolute maximum value of gate to emitter leakage current is typically specified at a gate voltage of 20V while collector and emitter are grounded.

Threshold Voltage, V_{th}

V_{th} indicates at what Vge voltage level the IGBT starts to conduct. It is tested by shorting Gate and Collector and applying a specified current source (e.g 500 mA) to collector.

Diode Forward Voltage, V_F

Diode forward voltage is measured when IGBT is in off−state. A forcing current is applied to the power pins of the module and the V_F is measured through sensing pins.

This helps eliminate the voltage drop effect along the current path (e.g wire, terminals) except the diode itself. Datasheet provides V_F in a table with specified condition and curves at different temperatures and current.
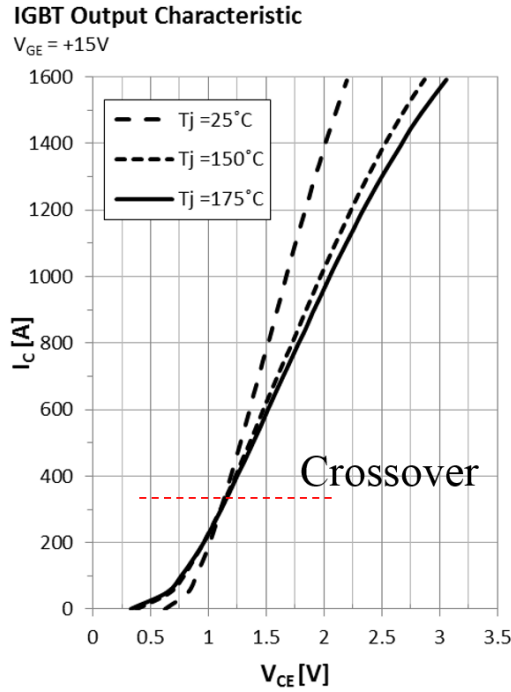
IGBT Output Characteristic

$V_{GE} = +15V$

Figure 13. Typical IGBT Output Characteristic Curve Showing the Crossover from NTC to PTC

Dynamic Characteristics

Parasitic Capacitances, Cies Coes Cres

As inherent parts of an IGBT device, several parasitic capacitances play a role in the device's dynamic characteristics including: input capacitance Cies, output capacitance Coes and reverse transfer capacitance Cres.
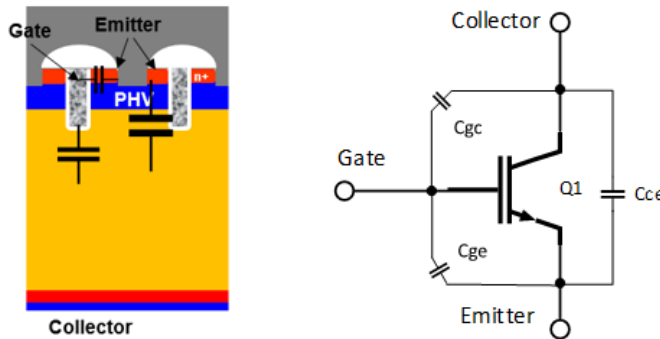
Figure 14. Parasitic Capacitance in an IGBT

Input Capacitance, Cies=Cge+Cgc

Input capacitance is formed by parallel combination of gate−to−emitter and gate−to−collector. The gate−to−emitter consists mainly of the metal−oxide−semiconductor capacitance and is generally constant. However gate−to−collector capacitance is voltage VCE dependent.

Output Capacitance, Coes=Cce+Cgc

Output capacitance is formed by parallel combination of collect−to−emitter and gate−to−collector, both of which are voltage dependent and varies with different collector−to−emitter voltages.

Reverse Transfer Capacitance, Cres=Cgc

Made up of gate−to−collector capacitance, reverse transfer capacitance plays an essential role in gate driving of the IGBT, as it provides negative feedback from collector to gate and is responsible for the gate voltage plateau. Specifically, during IGBT turning on, the fast falling of collector−to−emitter voltage forms a considerable current from collector to gate through Cres which counteracts the rising of the gate voltage. Similarly, during IGBT turning off, the fast rising of collector−to−emitter voltage draws current from gate through Cres which counteracts the falling the gate voltage. Coes and Cres tend to decrease when V_{CE} voltage is increasing while Cies is mostly stable across different V_{CE} voltages. Figure 15 shows a typical Capacitance vs VCE Curve for a 750 V VE−Trac Dual IGBT.
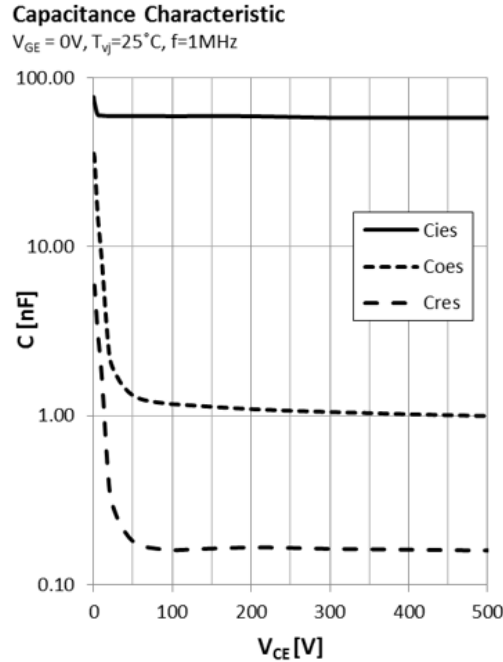
Figure 15. Typical Parasitic Capacitance Curves versus Vce

Gate Charge, Q_G

Though input capacitance is useful, gate charge provides a more convenient way in determining the average driving power for the IGBT. Specifically, the driving power is determined by following equation:

$$P_{gd} = fs * Q_G * \left(V_{ge(on)} - V_{ge(off)} \right) \qquad \text{(eq. 6)}$$

Where f_s is switching frequency, $V_{ge(on)}$, $V_{ge(off)}$ are on−state gate−to−emitter voltage and off−state gate−to−emitter voltage respectively.

Besides a Q_G value at a certain V_{ge} condition, the datasheet also provides a Q_G curve where different Q_G vs V_{ge} information can be found. Refer to below figure for a typical Q_G curve. See section on gate drive to see how Q_G is used to determine gate driver requirements.
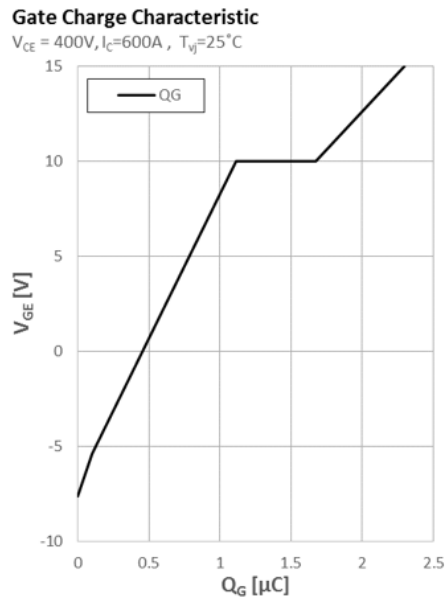
Figure 16. Typical Gate Charge Plot for the IGBT

IGBT Switching Characteristics

IGBT switching characteristics are one of the major focuses in improving IGBT performance as switching losses constitute substantial part of overall losses. The circuit diagram used in characterizing IGBT switching behavior is shown in Figure 17.

IGBT Switching Characteristics are given in two types: one type is measured in time dimension−−−delay time and rise/fall time, this information is useful in determining an appropriate dead time between turn−on and turn−off of high and low side IGBTs in a half bridge configuration. Another type is measured in losses −−− turning on/off losses at room and high temperatures under a given condition, such as Bus voltage, Gate resistance and Gate voltages etc. This information is useful in estimating switching losses in real application and compare performances of devices from different suppliers.
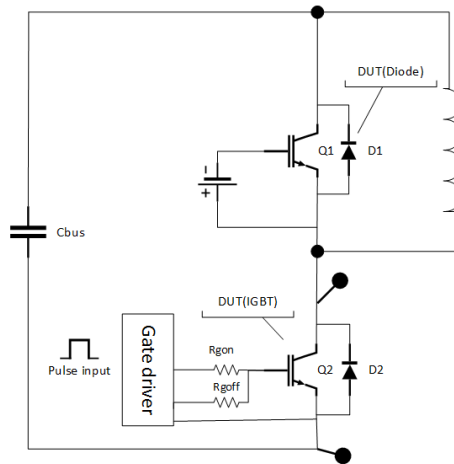
Figure 17. Double Pulse Test (DPT) Circuit Used to Measure Switching Characteristics

The definitions for IGBT switching characteristics are explained as below:

a. Turn on delay time, $T_{d.on}$
Time interval from the moment when gate−emitter voltage reaches to 10% of rated value to the moment when collector current reaches 10% of its nominal value.

b. Turn off delay time, $T_{d.off}$
Time interval from the moment when gate−emitter voltage drops to 90% of rated value to the moment when collector current drops to 90% of its nominal value.

c. Rise time, T_r
Time it takes for collector current to rise from 10% to 90% of its nominal value.

d. Fall time, T_f
Time it takes for collector current to fall from 90% to 10% of its nominal value.

e. Turn−on switching losses E_{on},
Turn−on switching losses are integral of power−−Collect−to Emitter voltage multiplying Collector current−−−− over the time interval starting when the collector current reaches 10% of its final value and ending when collector−emitter voltage drops to 2% of IGBT's off−state value, illustrated as below equation:

$$E_{on} = \int_{t1}^{t2} V_{CE} * I_C * dt \qquad (eq. 7)$$

f. Turn−off losses, E_{off}
Turn−off switching losses are integral of power−−Collect−to Emitter voltage multiplying Collector current −−−− over the time interval starting when collector−emitter voltage reaches 10% of its final value and ending when collector current drops to 2% of IGBT's on−state value, illustrated as below equation:

$$E_{off} = \int_{t3}^{t4} V_{CE} * I_C * dt \qquad (eq. 8)$$

Below in Figure 18 illustrates how those times and losses are defined:
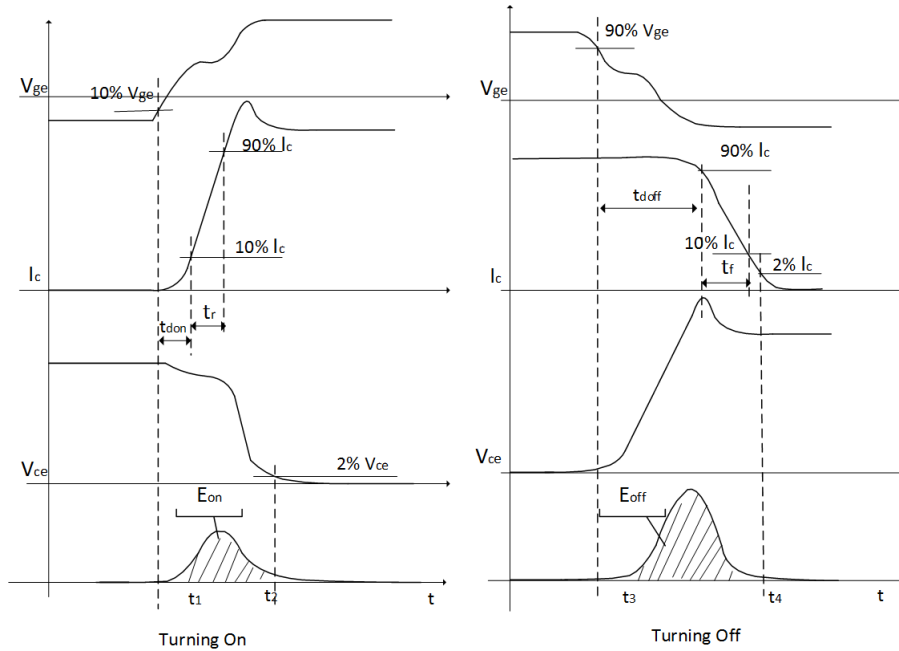
Figure 18. Switching Definitions for the IGBT

Diode Switching Characteristics

When the diode is switched from forward current carrying to reverse voltage blocking by turning−on of the opposite side IGBT, it enters the Reverse Recovery State. Refer to Figure 19 for double pulse testing configuration and definition of diode reverse recovery parameters.
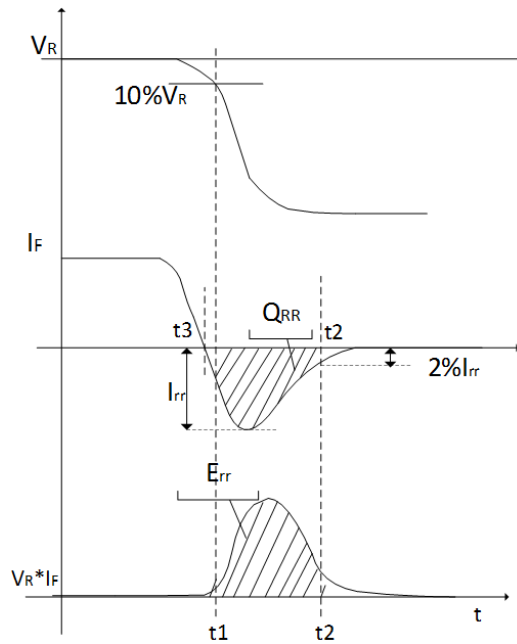
Figure 19. Switching Definitions for the Diode

a. Reverse Recovery Current, I_{rr}
Reverse recovery current is the peak current when the diode current is commutated from forward conducting to reverse bias. It depends on the initial forward diode current and current slope rate−−di/dt.

b. Reverse Recovery Charge, Q_{rr}
Reverse recovery charge is the amount of charge that is recovered from the diode during turning off. It is calculated by integrating the reverse recovery current over the time period starting when diode current crosses zero and ending when diode reverse current return to 2% of its peak reverse current(I_{rr}). Shown as below equation:

$$Q_{rr} = \int_{t3}^{t2} I_F dt \qquad \text{(eq. 9)}$$

c. Reverse Recovery Energy, E_{rr}
Diode reverse recovery energy are integral of power—Diode reverse voltage multiplying diode reverse current −−−− over the time interval starting when reverse voltage reaches 10% of its final value and ending when reverse current returns to 2% of its reverse recovery peak current, illustrated as below equation:

$$E_{rr} = \int_{t3}^{t2} V_R * I_F dt \qquad \text{(eq. 10)}$$

INTEGRATED SENSORS

All VE−Trac Dual modules consist of on−chip or integrated sensors to implement protection functions for device temperature and current.
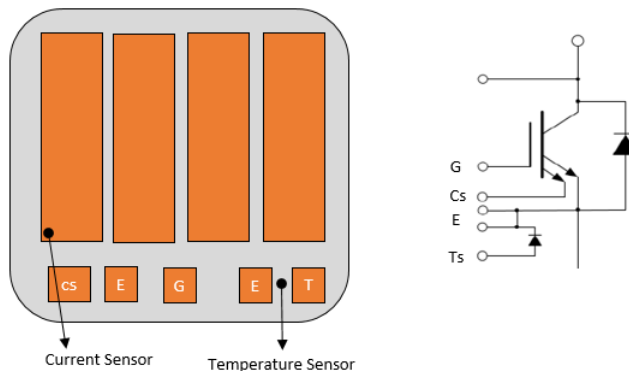
Figure 20. Location of the Integrated On−chip Temperature and Current Sensors

Temperature Sensor

The On−Chip temperature sensor of VE−Trac Dual consists of a string of four polysilicon diodes connected in series and terminals brought out of the package for external connections. To determine the junction temperature of the IGBT chip, the temperature sense diode needs to be biased by a constant current source between 200 μA – 1000 μA. The temp sense diode forward voltage drop Vf.ts which is temperature dependent, is used to determine IGBT junction temperature. Figure 20 shows the temperature sensor location on the IGBT die. Using the on−chip temperature sensor for Over Temperature (OT) protection in lieu of the traditional thermistor mounted on the DBC has two distinct advantage (i) Faster response and (ii) Accuracy to the true Tvj of the IGBT. The scope capture below (Figure 21) shows the comparison between temperature sense diode and a thermistor on a DBC to a step change in collector−Emitter current.
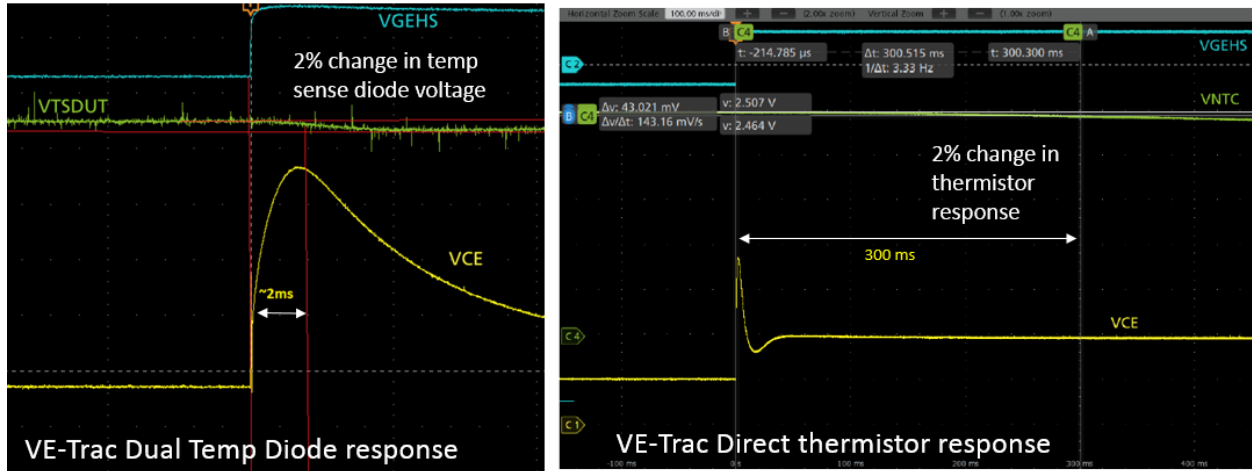
Figure 21. On−chip Temperature Sensor Response Time versus Thermistor Response

In Figure 21 the plot on the left shows the IGBT virtual junction temperature (Tvj) determined using the indirect VCE method as described in IEC 60747−9 and the data compared to the sense diode temperature with a bias current of 250uA. Note that the temperature determined by the VCE method is the average peak junction temperature of the IGBT chip across the entire chip. The variation in junction temperature between the different junction locations on the chip can be as much as 10°C. So, the plot compares the average peak TvJ determined by the VCE method to the peak temperature of the sense diode, which is located in the hottest part of the chip. However, the presence of the pads for the sensors itself acts has a heatsink and will tend to lower the sensor temperature from true junction peak Tvj. But the temperature determined by the on chip sensor is much closer to the true Tvj when compared to using a thermistor located on the DBC to determine the Tvj. This difference in accuracy is shown in Figure 22 on the right where the error is plotted over the power dissipated in the IGBT.

The on−chip temperature sense diode in the VE−Trac[TM] Dual offers a faster responding and more accurate method for determining the IGBT junction temperature.
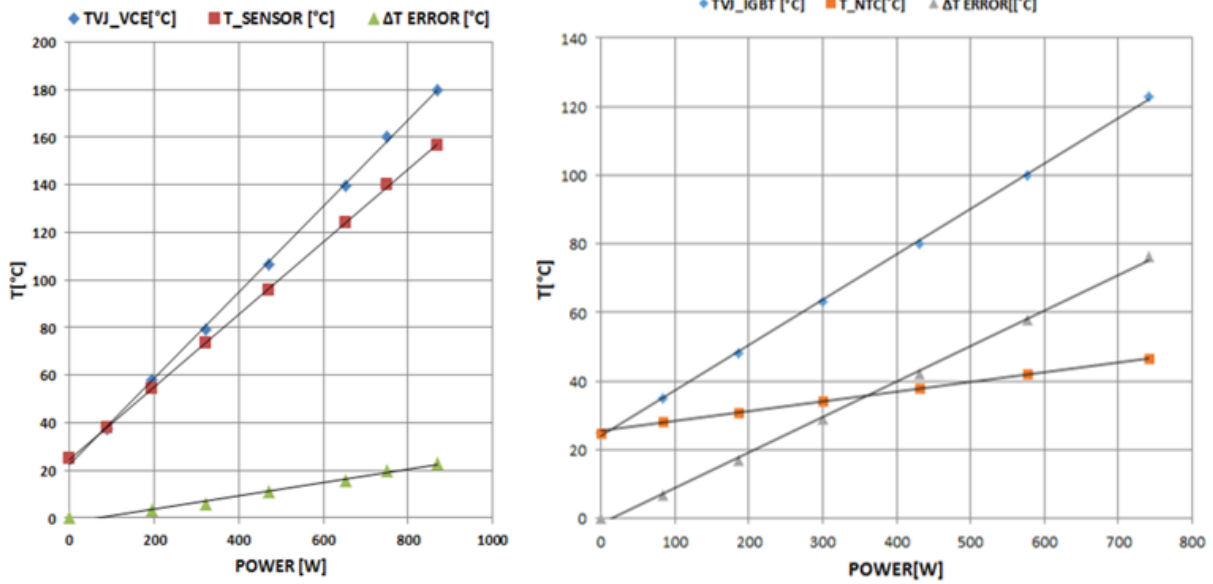
Figure 22. Comparison of Tvj Determined with Vce Method Compared to On−chip Sensor (Left) and Thermistor (right)

The temperature sense diode must be biased with a precision constant current source to obtain an output voltage for all operating conditions. Figure 24 shows the recommended precision constant current source circuit for 1 mA using a precision programmable constant current source (LT3092). In this circuit the reference constant bias current can be programmed by two resistors R1 and R2 shown in the circuit. It is also possible to implement the circuit for other bias currents. Many new gate drivers provide a lower constant bias current for temp sense.

However, 1 mA is recommended to get a better quality signal at the higher temperature range where detection is critical for over temperature protection. The user should determine the best bias current for their specific application. However, it is necessary to calibrate the sensor to the correct bias current to develop the correct relationship between the IGBT Tvj and temperature sense diode reading. Figure 23 shows example calibration data for the 750 V, 800 A module at 1 mA bias current using a thermal chamber.
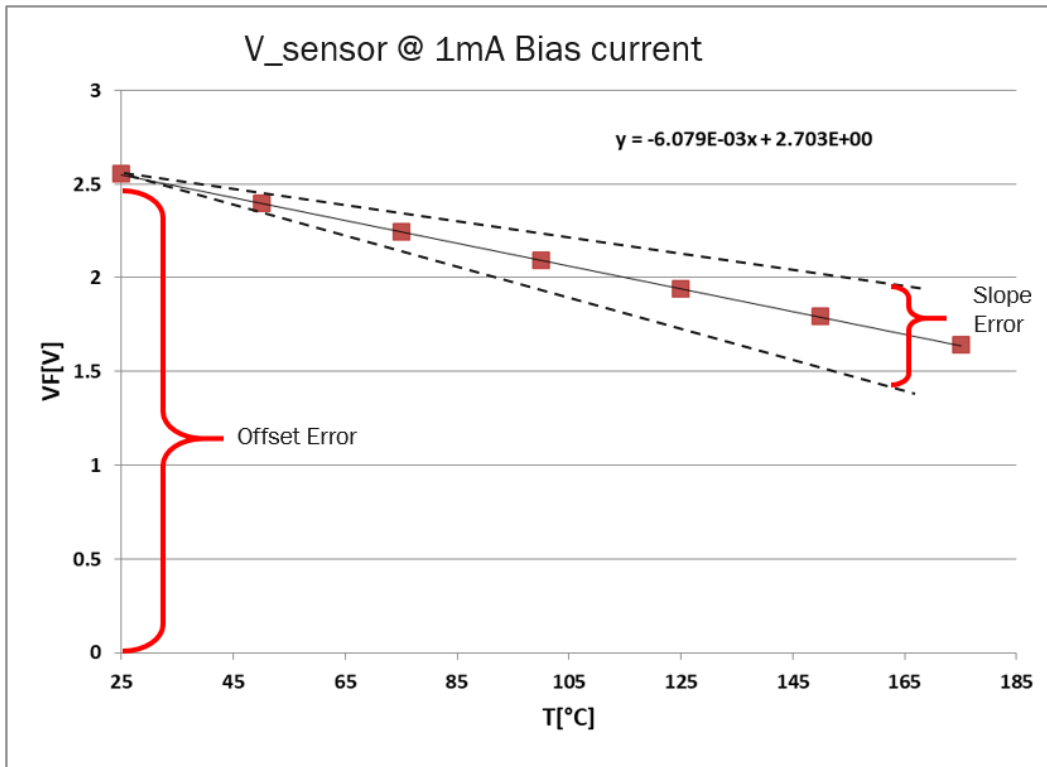
Figure 23. Calibration Data for the Sense Diode in a 750 V, 800 A Module at 1 mA Bias Current
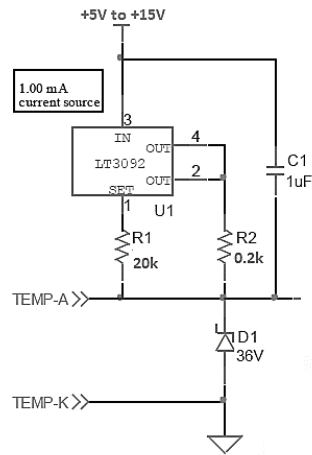
Figure 24. Example Current Bias Circuit for the Temperature Sense Diode

Measurement of junction temperature of IGBT using temperature diode has two factors to be considered – Slope and Offset error as shown in Figure 23. The offset error is the single biggest source of error in the temperature reading and its min/max values are provided in the product data sheet. It is recommended that the offset error be minimized with a single point calibration in the detection circuit.

With accurate reading from the sensor it is possible to establish a relationship between the true Tvj and the sensor reading as shown in Figure 25.
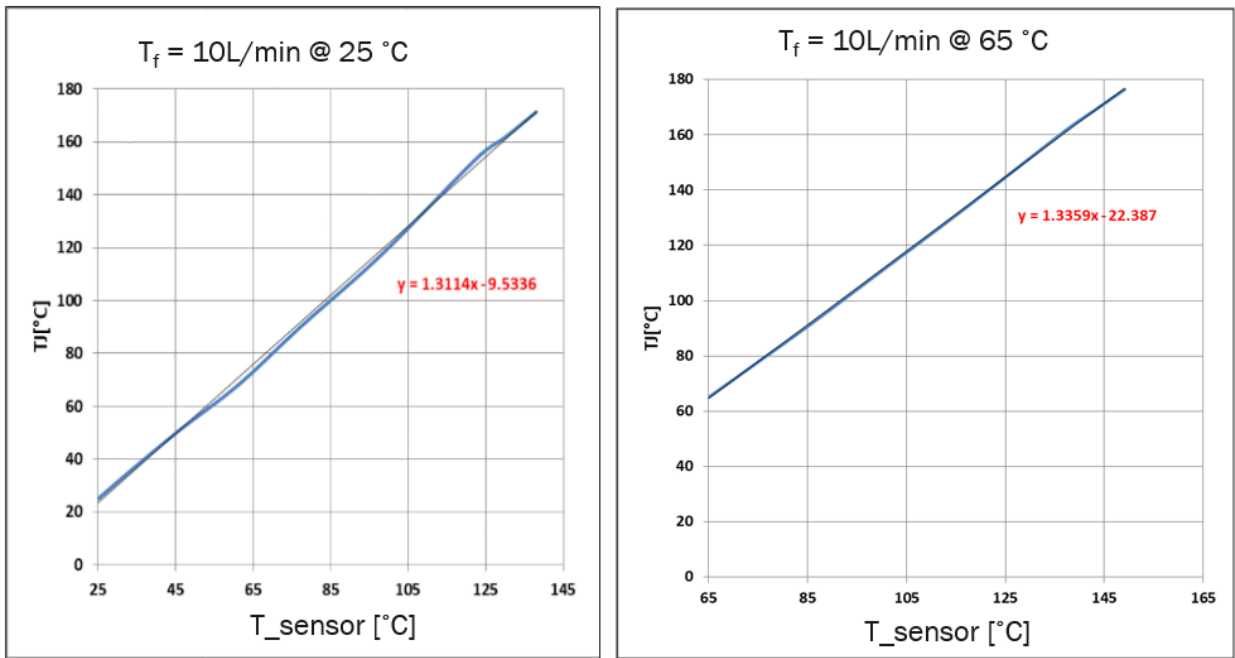
Figure 25. Example Relationship Between Tvj and Temperature Sense Diode Reading

Example implementation of an Over Temperature (OT) protection circuit that will monitor the temperature sense diode voltage Vf.ts continuously and trigger protection once the threshold exceeds a reference value as shown in . The fault signal will be generated and sent to the controller of the inverter to initiate IGBT gate shutdown. The temperature sense voltage (Vf.ts) is filtered by first order RC (R632 and C136) filter to reduce switching noise and feedback to the non−inverting input of the comparator and reference threshold which is programmable via resistor R635. During normal operation the comparator output will be high and when the device exceeds the threshold during operation the comparator output goes low indicating a fault.
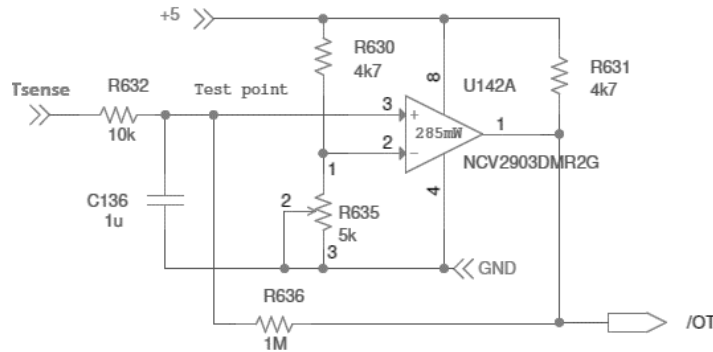
Figure 26. Example Over Temperature (OT) Protection Circuit

The fault signal can be transmitted to the low voltage digital side of the gate driver or the controller via optical isolators for fault management or to implement temperature dependent controls.

Current Sensor

The On−Chip integrated current sensor in the 750 V 800 A VE−Trac Dual IGBT module employs a current mirror output. The current mirror is constructed by segmenting off a portion of the main emitter cells and providing a separate external bonding pad connection. The Current mirror group of cells provides a low level current that is proportional to the main emitter current. The sense ratio for Sense current to main current is 1:10,000. Figure 27 shows the equivalent circuit of the current sense.
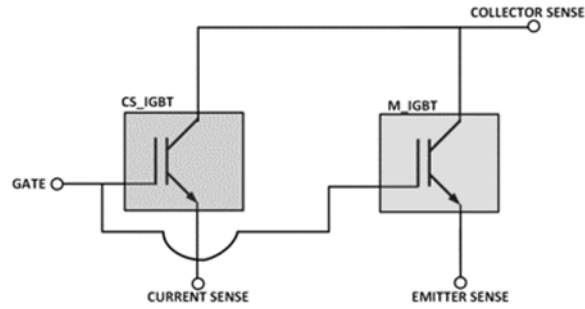
Figure 27. Equivalent Circuit of the Current Sensor

One of the most common methods to measure the sense current signal is to use a shunt resistor. The resistance Rshunt is connected between the current sense and emitter sense pin of the power module. This method is ideal for a protection function where we only need to detect if the IGBT is exceeding a preset current threshold. Figure 28 shows the implementation of the shunt resistance, where Vsense = Isense x Rshunt.
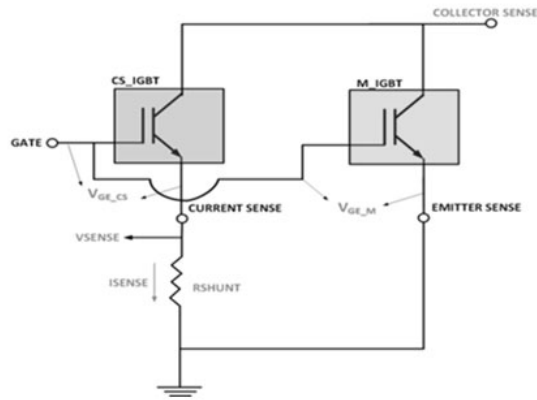

Figure 28. Simple Method to Sense Current Feedback with a Shunt Resistor

The voltage developed across it is directly proportional to the main emitter current. This is a low cost approach to implementing over current protection, but this method has some limitations. The sensing current depends not only on the main emitter current but also the temperature and the effective gate to emitter voltage. Ideally, to have equal VGE the Rshunt value must be low, but too low a value and it becomes difficult to detect the signal. VGE_M is the Main IGBT and VGE_CS is for Current sense IGBT. Figure 29 shows the variation of Vsense measured using Rshunt of 10 Ω at different temperatures. The recommended value for Rshunt is between 0.5 Ω and 10 Ω.
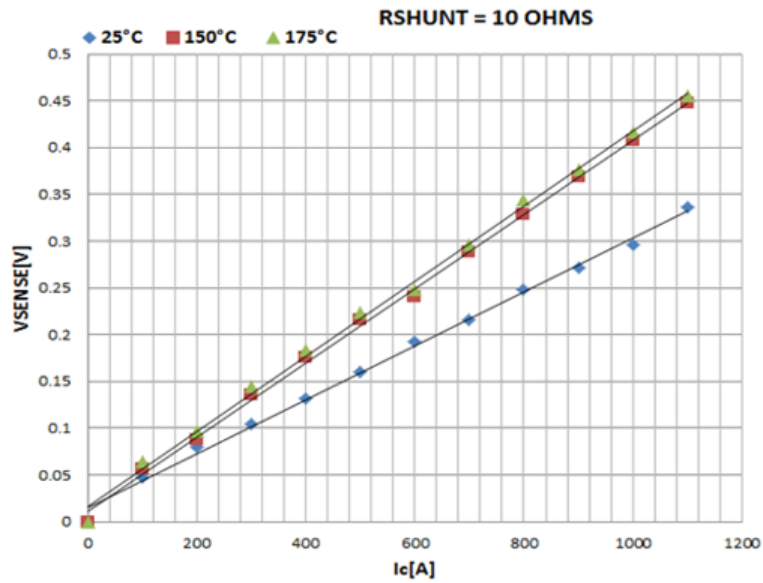
Figure 29. Current Sense Response with a 10 Ω Shunt Resistor at Various Temperatures.

Another method for detecting the current is to use a transconductance amplifier as shown in Figure 30. Here Vsense = Isense x RF. Because of the trans−conductance amplifier's virtual ground concept, both sensing IGBT VGE_CS and Main IGBT VGE_M are at the same potential and hence the Vsense output only depends on the sense ratio and is less dependent on temperature variations. Figure 31 shows the variation of Vsense measured using the transconductance amplifier method at different temperatures. As seen in the figure there is very little variation with temperature when employing this method to detect the current signal.
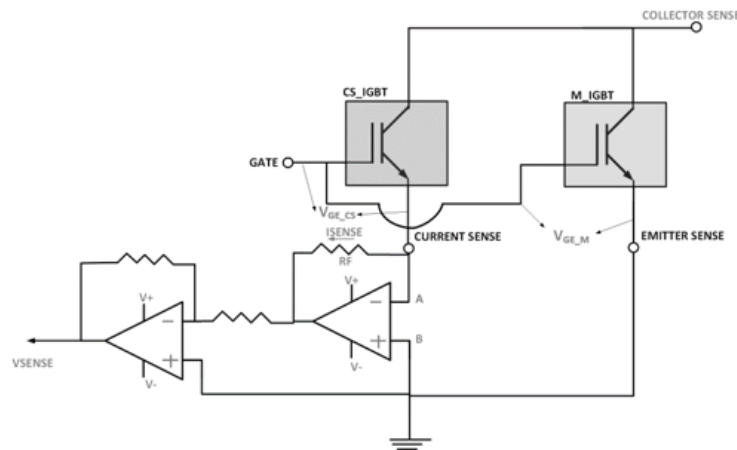
Figure 30. Implementation of Transconductance Amplifier Method to Sense Current Feedback
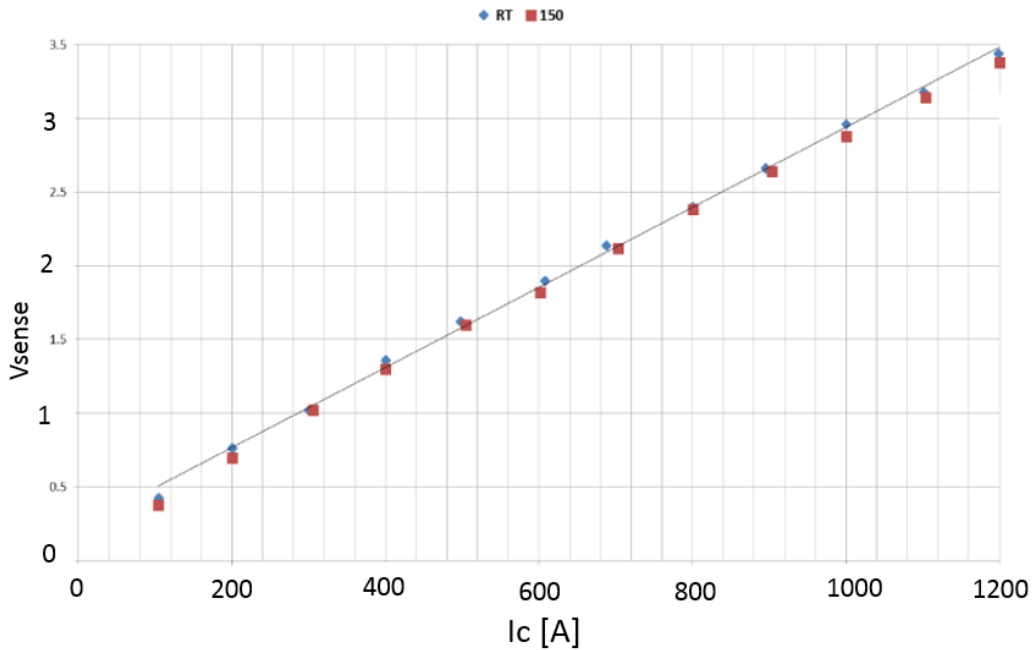
Figure 31. Current Sense Feedback Using the Transconductance Amplifier Method at Different Temperatures

Using the on−chip current sensor for OCP in lieu of the traditional Desat circuit has two distinct advantage (i) Faster response and (ii) No need to have a high voltage blocking diode on the driver board. In the test described below, the OCP threshold was set at 550 A. The Protection circuit detected fast and turn−off initiated within 240 ns, which is much faster than the conventional Desat method which was measured to be 4.6 μsec. Figure 32 shows the OCP implementation using On chip current sensor. In this circuit the OCP threshold can be adjusted via resistors R107 and R112. I_SNS_OUT = I_in x (R15 + R16).
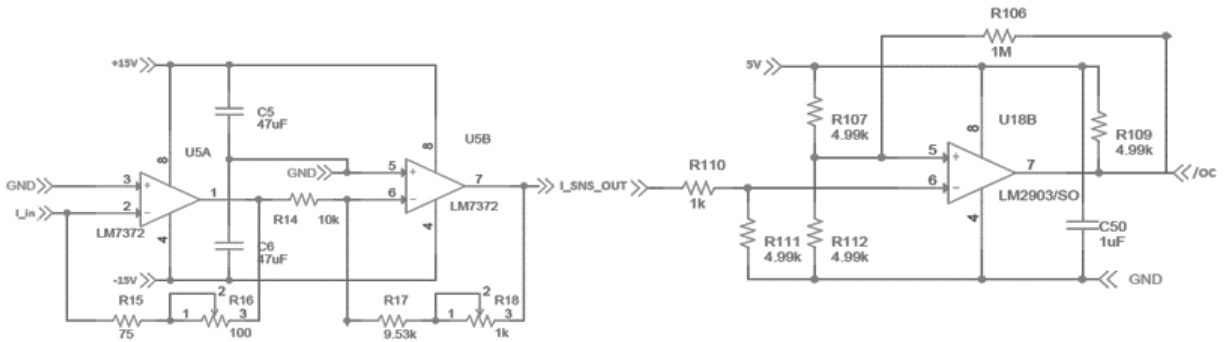
Figure 32. Implementation of OCP.
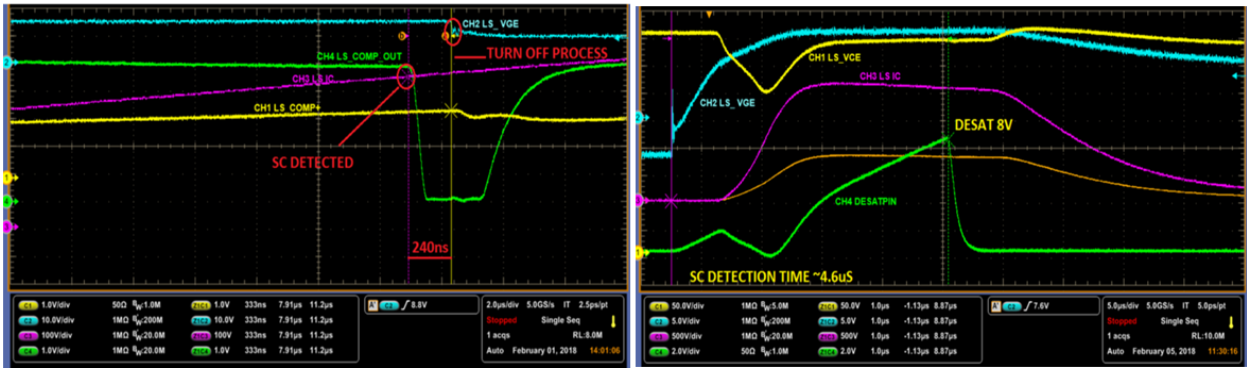
Figure 33. Faster OCP with Current Sense Feedback Compared to Desat Detect

DESIGN CONSIDERATIONS

Several factors should be considered when designing a power converter using the VE−Trac Dual module. This document will cover many of the electrical design requirements. However, many of the mechanical requirements are covered in the assembly guide – a separate document.

Gate Drive

The gate driver turns on and off the IGBT to a defined VGE_ON and VGE_OFF voltage levels. The transition between the two gate voltage levels needs a power to be dissipated in the gate driver. The gate driver power rating should be selected according to driver power required for an IGBT module.

The gate driver power required depends on Q_G – total gate charge of an IGBT module, switching frequency Fsw and the gate driver output voltage swing ΔVGE (VGE_ON − VGE_OFF)

$$P_{gd} = Q_G * F_{SW} * \Delta VGE \qquad \text{(eq. 11)}$$

If an external CGE is connected then the Power required for charging and discharging the external CGE should also to be considered

(eq. 12)
$$P_{gd} = Q_G * F_{SW} * \Delta VGE + CGE * F_{SW} * \Delta VGE2$$

The switching speeds of an IGBT are controlled by charging and discharging rate of the gate capacitances, Higher the peak current, lower are the losses. Other switching factors like overvoltage stress and peak reverse recovery current of freewheeling diode has a direct impact on this. The turn−on and turn−off peak gate currents are controlled by resistors $R_{G,ON}$ and $R_{G,OFF}$ respectively (see Figure 34).
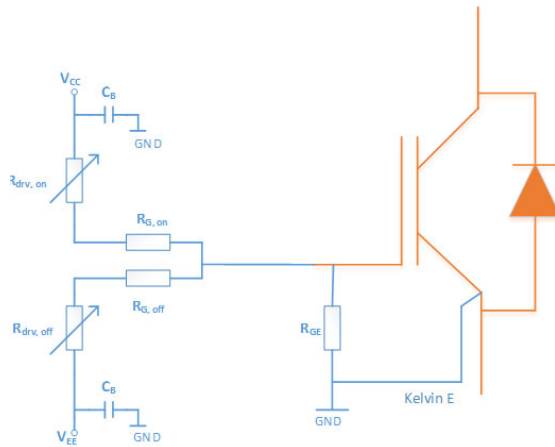
Figure 34. Basic Gate Drive Circuit

(eq. 13)
$$I_{GPEAK-ON} = (V_{CC} - V_{EE})/(R_{G,ON} + R_{G,INT} + R_{drv,on})$$

(eq. 14)
$$I_{GPEAK-OFF} = (V_{CC} - V_{EE})/(R_{G,OFF} + R_{G,INT} + R_{drv,off})$$

The average current needed for switching an IGBT at switching frequency of Fsw and total gate charge Q_G can be calculated as follows:

$$I_{G(AVG)} = Q_G * F_{SW} \qquad \text{(eq. 15)}$$

The gate driver continuous current rating should be > $I_{G(AVG)}$ calculated.

The peak charging and discharging rate of gate currents to the input capacitance of an IGBT module results in power dissipation in the gate resistors. The gate resistor must be sized to handle this power dissipation. The peak charging or discharging current can be approximated as a discontinuous triangular wave.

$$P_{RG} = (2/3) * I_{GPEAK}{}^2 * T_P * F_{SW} * R_G \quad \text{(eq. 16)}$$

Where:

I_{GPEAK}: IGBT Gate drive peak current

T_P: Duration of the pulse usually between 500 ns to 1 μs

Fsw: IGBT switching Frequency

R_G: Gate resistance

Sometimes there is significant ringing on the gate drive loop. The gate driver equivalent circuit with parasitic is as shown below.
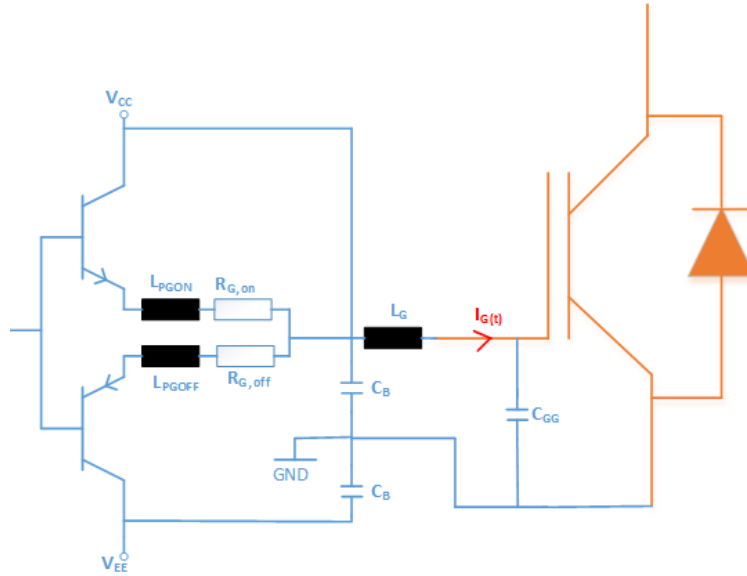
Figure 35. Gate Drive Equivalent Circuit Shown with Parasitics

The gate current is $I_G(t)$ is related to known second order differential equation for RLC circuits. During turn −on L_T and R_T represent total inductance and resistance in the turn−on path

$$L_T = L_{PGON} + L_G \quad \text{(eq. 17)}$$

$$R_T = R_{G,ON} + R_{GINT} \quad \text{(eq. 18)}$$

The minimum value of R_T required for non−oscillation or for over damped condition is $R_T = R_{G,ON} + R_{GINT} > 2 * S_{QRT}(L_T/C_{GG})$

During turn−off L_{TF} and R_{TF} represent total inductance and resistance in the turn off path of the gate loop.

$$L_{TF} = L_{PGOFF} + L_G \quad \text{(eq. 19)}$$

$$R_{TF} = R_{PG,OFF} + R_{GINT} \quad \text{(eq. 20)}$$

The minimum value of R_{TF} required to prevent oscillation or for over damped condition is $R_{TF} = R_{G,OFF} + R_{GINT} > 2 * S_{QRT}(L_{TF}/C_{GG})$

Uni−Polar versus Bi−polar Drive

The unipolar gate drive switches on the IGBT with voltage VGE_ON (typically +15 V) and turns off the IGBT

voltage with 0V. This arrangement is not recommended for EV traction drive applications, since it tends to increase switching losses and increase EMC susceptibility. However, if a uni−polar drive is desired, the following precautions should be considered:

1. Parasitic Turn on due to miller capacitor and high dv/dt
2. Parasitic turn on via stray inductances

Parasitic turn−on via stray inductance can be common when there is no kelvin emitter sense, in which case the gate driver reference shares the same reference as the power emitter.

In the Inverter half bridge application when the low side IGBT turns−on, a high side IGBT experiences a voltage rise dvce/dt. This causes a displacement current ICGC = CGC*dvce/dt to flow through the miller capacitor and RG,off of the upper IGBT and back into the driver as shown in Figure 36. As a result VGE rises when it exceeds the VGE(th) parasitic turn−on of the high side IGBT. This can result in a shoot−through event i.e short across the DC link.
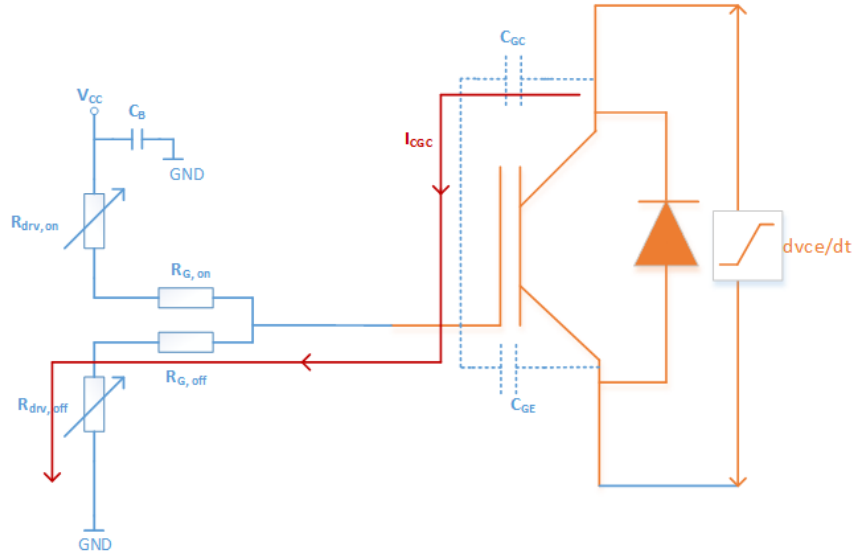
Figure 36. Parasitic Turn−on Due to Miller Capacitor and High dv/dt

$$V_{GE} = I_{CGC} * \left(R_{G,off} + R_{drv,off} + R_{GINT} \right) \quad \text{(eq. 21)}$$

A shoot event through can destroy the module. Thus when designing a gate driver circuit, maximum allowed dv/dt has to be considered. The maximum allowed dv/dt can be calculated as follows:

$$\frac{d_{VCE,max}}{dt} > \frac{V_{th}}{C_{GC} * R_{G,tot}} \quad \text{(eq. 22)}$$

Where Vth is the threshold voltage of IGBT for VE−Trac^TM Dual. Vth is equal to 5.5 V and CGC is the Miller capacitance of the IGBT and is equal to 1.3 nF (for example). Thus from above equation the maximum allowed dv/dt for VE−Trac^TM Dual Side cooling will be

$$\frac{d_{VCE,max}}{dt} > \frac{4.2}{R_{G,tot}} \, (V/ns) \quad \text{(eq. 23)}$$

Where $R_{G,tot}$ is the total gate resistance during turn off event.

In order to increase the robustness of unipolar gate drive against the parasitic miller capacitor turn−on, consider using an Active Miller Clamp circuit where during turn−off the V_{GE} voltage is monitored internally within the gate driver. When the voltage V_{GE} falls below 2 V relative to the emitter reference, the clamp circuit is activated. This clamp switch (see Figure 37) shorts the Gate Emitter terminals of an IGBT and shunts all the miller displacement current into it, thereby reducing the V_{GE} below the threshold voltage V_{GETH}.
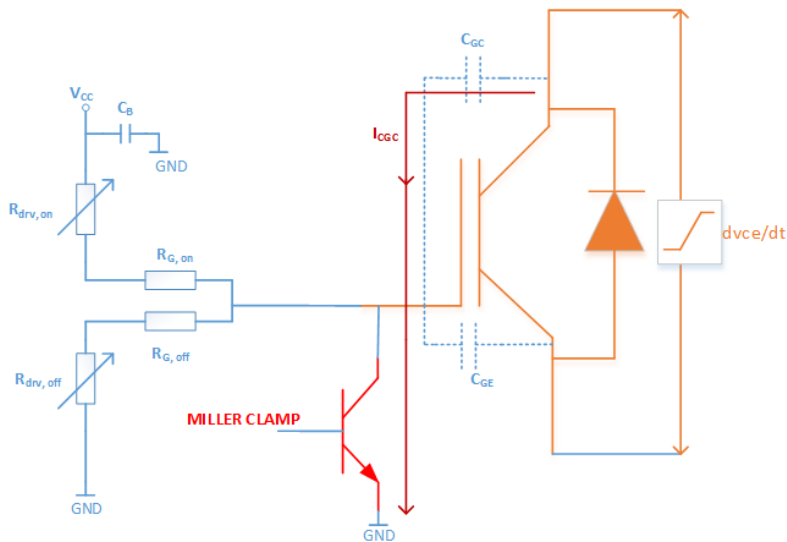
Figure 37. Example Use of Miller Clamp to Prevent Unintended Turn−on

Parallel Operation

The VE−Trac Dual can be paralleled to achieve higher power converter designs. There are four major design considerations when paralleling the Dual modules:

1. Steady state current sharing
2. Dynamic current sharing
3. Gate drive symmetry
4. Balanced cooling

Steady state current imbalance is mainly caused by differences in Vcesat and differences in parasitic resistance in the power circuit. The VE−Trac Dual power module uses IGBTs with positive temperature coefficient, which tend to balance Tvj at higher currents under steady state conditions (see Figure 38). Another way to reduce this imbalance is to use devices with similar Vcesat for paralleling. IGBTs from the same production lot can minimize the influence of process variations.

The variation in resistance in the main power loop can also lead to an imbalance in current at steady state. This effect is more pronounced with emitter resistance than with collector resistance. In order to minimize this effect its important the emitter connections for the paralleled modules are as short and as symmetric as possible. In Figure 39 it is important to make RM1 = RM2 and REL1 = REL2.

Under dynamic conditions module parameters like Vth and Cies have a strong influence on current sharing between modules just before turn−off and right after turn−on. Matching there parameters on paralleled sets of modules is not always practical. But wiring symmetry is also something that influences current sharing in dynamic conditions and can be minimized. In Figure 39 it is best to make LEL1 = LEL2 and LM1 = LM2 which will balance the emitter inductance between the 2 paralleled IGBTs. In practice, this is achieved by placing the two paralleled modules as close as possible and making the main current path as symmetrical as possible. An idealized illustration of the physical layout for the modules are shown in Figure 40.
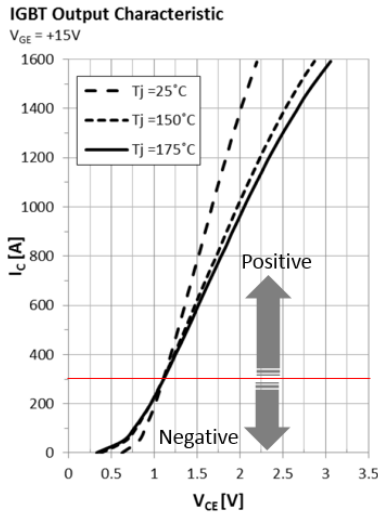
Figure 38. Positive and Negative Temperature Coefficient
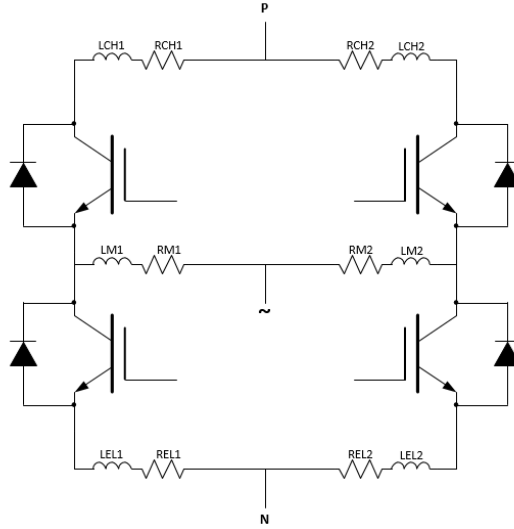
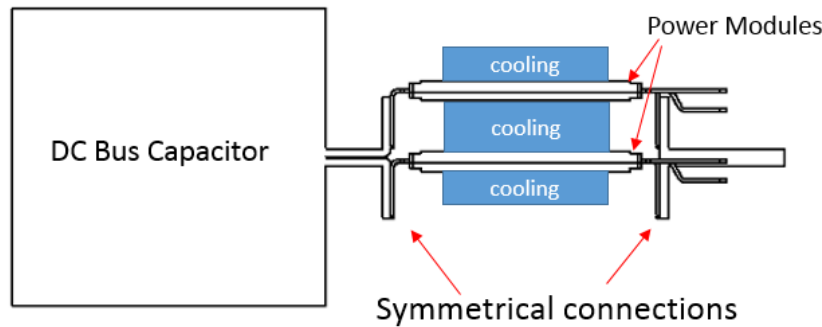Figure 39. Equivalent Paralleled Modules

Figure 40. Idealized Symmetrical Power Connections

The gate drive circuitry is another critical aspect when paralleling modules. Because turn−on and turn−off delays vary from one driver to another, it is recommended that all paralleled modules be driven by the same driver. It is necessary to use separate gate resistors to strike a good balance between gate oscillations and dynamic current sharing. Figure 41 shows a recommended gate drive circuit for two paralleled power modules. The components shown in dotted lines are optional and require some testing in the end application to determine if they help reduce oscillations or make matters worse.
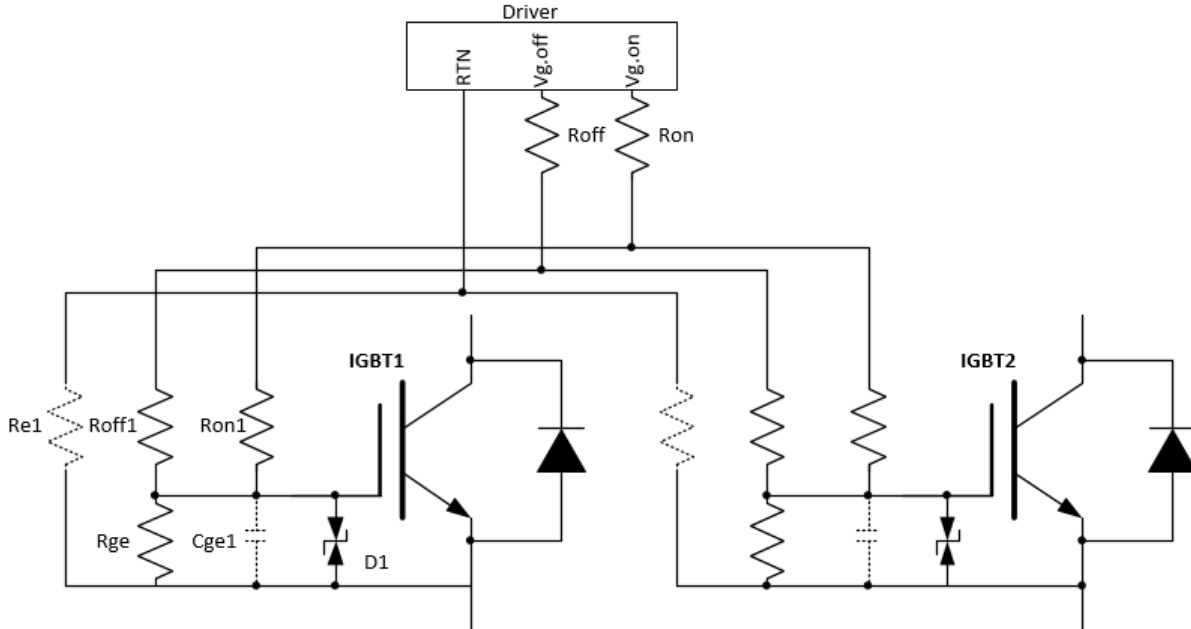
Figure 41. Recommended Gate Circuit for Two Paralleled VE−Trac Dual Modules

RELIABILITY

Qualification Tests

The objective of the qualification tests are to ensure general product quality and reliability. The product use the requirements set in the AQG324 document as its minimum requirements and in some cases will exceed these requirements.

Table 4. STANDARD QUALIFICATION TESTS PERFORMED ON THE VE−TRAC DUAL MODULES. ADDITIONAL TEST ARE DONE TO MEET CERTAIN CUSTOMER SPECIFIC REQUIREMENTS.

Test	Standard	Test Conditions
High Temp Reverser Bias	MIL STD750−1 M1038A	Tj = 175°C, Bias = 80% VCE
High Temp Gate Bias +/−	JESD22 A108	Tj = 175°C, Bias = 100% rating
High Temp / Low Temp Storage Life	JESD22−A101	175°C / −40°C
Temperature Shock	JESD22−A104; Q101	−40°C to 125°C
High Humidity High Temperature Reverse Bias	JESD22−A101	85°C, 85% RH, Bias = 80% rating
Short Circuit Reliability	AEC Q101 − 006	−40°C to +125°C
Power Cycling Test	AQG324	Multiple Pcmin & PCsec conditions defined to meet the requirements in the standard.
Vibration Variable Frequency	AQG324	25−500 Hz/15 min, 10 G, 2 hrs, XYZ
Mechanical shock	AQG324	500 m/s^2, 6−axis
ESD Characterization	AEC Q101−001 and −005	HBM, CDM

Module Life

A lifetime equation is extracted using failure data measured from six different power cycle test conditions. Data from these tests are used to develop the lifetime equation.

A commonly used lifetime equation for power modules is based on equation shown below. The equation may be viewed as a combination of three effects (i) Coffin Manson stress cycle, ΔT^{β_1}, (ii) Arrhenius temperature aging term, $e^{\beta_2/(273+T_{j,max})}$ and (iii) stress duration term, $t_{on}^{\beta_3}$. The sign on exponents are explicitly included in the equation so that the expected impact is clear. For example, a negative sign in front of the β_1 exponent is expected since an increase in ΔT causes a reduction in N_f.

$$N_f = K * \Delta T^{-\beta_1} * e^{\beta_2/(273+T_{j,max})} * t_{on}^{-\beta_3} \quad \text{(eq. 24)}$$

At low ΔT, strains experienced during temperature pulses are elastic (i.e. fully recoverable) whereas at high ΔT, strains are plastic (i.e. result in a permanent set). The ΔT exponent for low ΔT conditions is ~2X higher compared to high ΔT. There is a region where both elastic and plastic deformation may be occurring therefore it is difficult to determine a lifetime model that fits over two different ΔT regimes. At ΔT less than 60°C, an approximation is made to the lifetime equation using the same form as the high ΔT region but with a different exponent for β_1. The lifetime equation for different modules are available on request in a separate document. The equations are a conservative estimate at a 5% probability of failure with a 95% confidence.

VISUAL MARKINGS

The product has a number of visual markings to enable traceability of the materials. It's important to link the traceability from the chip to the inverter to maintain an effective traceability chain.

Traceability and Identification

The figure and table below together describe the all the visual indicators on the module and provide an explanation of the markers. All the 2D codes are 3.78 x 3.78 mm in size. Some of the modules include the temperature sensor calibration information in a 2D code. This data is used to remove temp sense offset error in the sensing circuit. The code includes the temp sense voltage reading for high side (HS) and low side (LS) switch in the half−bridge module. The temperature is coded in degree centigrade with a 10x multiplier (eg. 25.2°C is coded as 252). The temperature sensor reading is coded in mV. The bias current for the temp sensor can vary for different products within the family, so consult the specific product data sheet for the correct value.
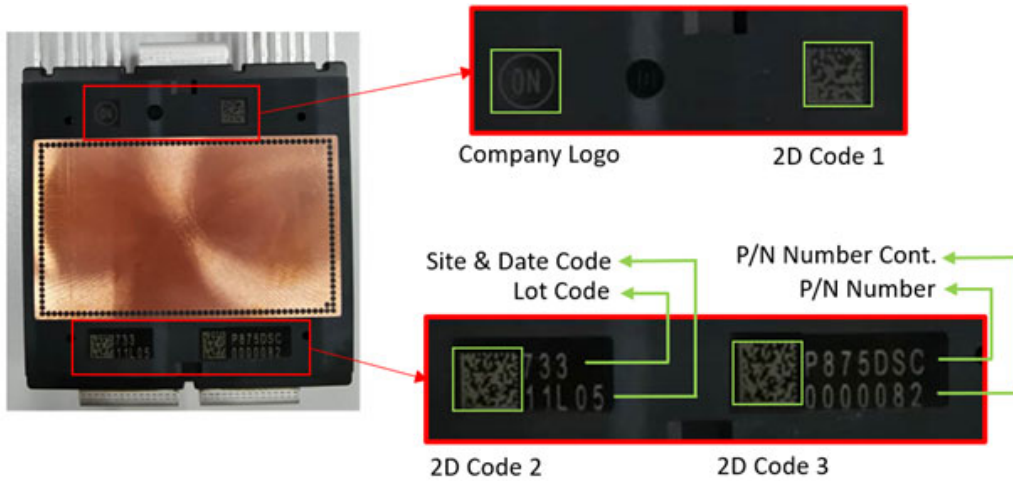

Figure 42. Overview of Product Markings

Table 5. PRODUCT MARKING DETAILS

Marker	Description
Company Logo	**onsemi** Logo
2D Code 1	Assembly Lot Number + S/N (3.78 x 3.78 mm)
2D Code 2	**Temperature sensor calibration data**: (3.78 x 3.78 mm) Temp1 x 10 + T−sense voltage HS + LS ; Temp2 x 10 + T−sense Voltage HS + LS Example: 25222342236;150211381318 25.2°C 2234 mV 2236 mV ; 150.2°C 1138 mV 1318 mV
2D Code 3	P/N + Last 3 digits of LOT number + Trace code (3.78 x 3.78 mm)
Site and Date Code	Assembly location (XX) and date code (YWW)
Lot Code	Last 3 digits of lot number
P/N Number Cont.	Remaining characters of product part number
P/N Number	First 7 Characters of product part number

Storage and Shipping

Transporting and storing the modules requires care to avoid extreme shock, vibration and environments. The recommended storage conditions for the module according to IEC 60721−3−1, class 1K2 should be followed and storage time should not exceed two years. Below is a summary of the recommended storage parameters:

Table 6. MAXIMUM STORAGE CONDITIONS

Parameter	Value	Unit
MAXIMUM AIR TEMPERATURE	40	°C
MINIMUM AIR TEMPERATURE	+5	°C
MAXIMUM RELATIVE HUMIDITY	85	%
MINIMUM RELATIVE HUMIDITY	5	%
CONDENSATION	Not Allowed	
PRECIPITATION	Not Allowed	
ICING	Not Allowed	

◊