LC75843UGA

Application Note

Design method of the LCD system using 1/3-duty LCD panel

ON Semiconductor®

http://onsemi.com

Overview

This application note explains the design method of the LCD (Liquid Crystal Display) system using LCD driver IC (LC75843UGA). The LC75843UGA is the 1/1 to 1/4 duty general-purpose LCD driver that can be used in applications such as automotive display by control with the controller.

In addition, this IC is able to drive up to 100 segments directly, and can also control up to four general-purpose output ports. Moreover, it has a built-in 3ch PWM (Pulse Width Modulation) function for brightness adjustment of LED (Light Emitting Diode). Furthermore, because of built-in the oscillator circuit, it is possible to reduce external resister and external capacitor for oscillation.

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

April, 2014 - Rev.0

LCD System Configuration Example

This application note explains various function explanations and setting method example of serial control data in the LCD system configuration using LCD driver IC (LC75843UGA) as shown below.

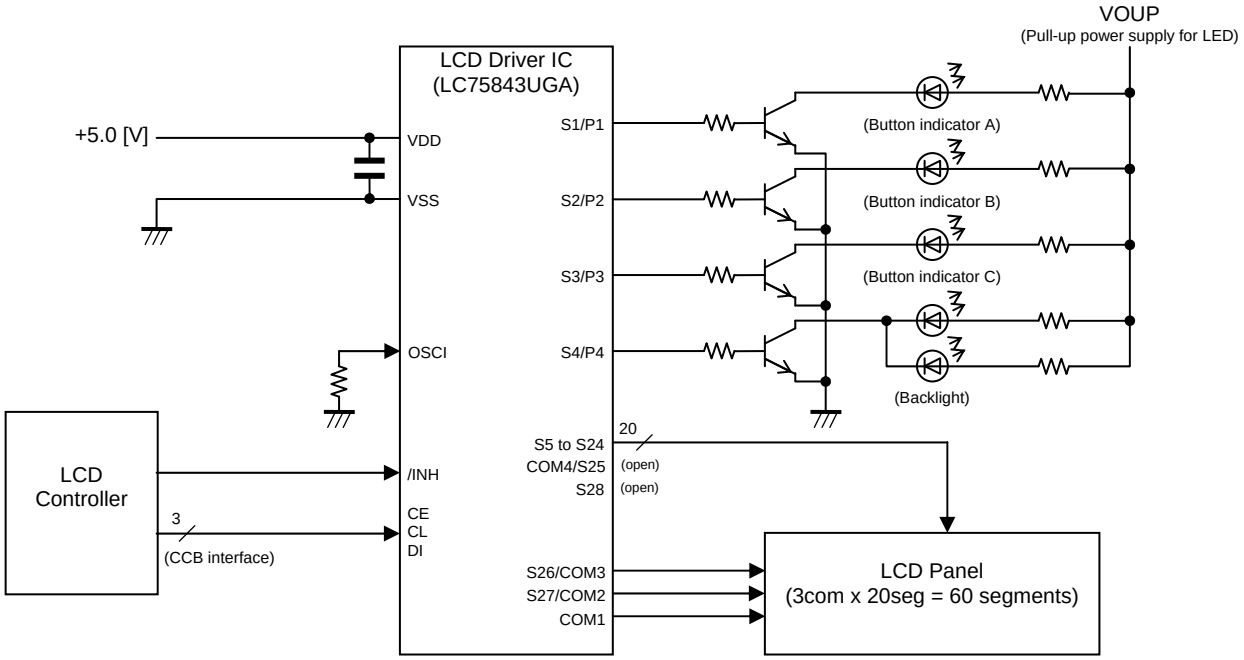


Figure 1. LCD system configuration using LCD driver IC (LC75843UGA)

< Operation specifications of the LCD system >

LCD driver IC (LC75843UGA) specifications	LCD system specifications of Figure 1
Support for static (1/1-duty) or 1/2-duty or 1/3-duty or 1/4-duty drive. (Capable of driving the LCD up to 100 segments directly)	The LCD panel to use has 20-segments and 3-commons. Total display segments are 60-segments. Therefore, LCD drive duty ratio is 1/3-duty.
Built-in LCD drive bias voltage stabilization circuit.	1/3-bias.
Support for up to four general-purpose output ports	The four general-purpose output ports are used.
Support for the PWM output function of a maximum of 3ch.	Control of the LED by PWM function.
Support for clock output function of 1ch.	Unused.
Incorporation of an oscillator circuit (Incorporation of resistor and capacitor for an oscillation), and setting of the “Internal oscillator operating mode” or “External clock input operating mode” is possible by serial control data.	Internal oscillator operating mode is used.
Serial control data input supports CCB* format communication with the system controller. (Support 3.3V and 5.0V operation)	Used. (Controlled by LCD controller)
Adjustment of the frame frequency of the LCD drive waveform is possible by serial control data.	Frame frequency is adjusted, but frequency value is undecided.
Adjustment of the frame frequency of the PWM drive waveform is possible by serial control data.	PWM is controlled, but frequency value is undecided.
Setting of the power saving mode or the all segments turn off mode is possible by serial control data.	Used. (Controlled by LCD controller)
The /INH pin allows the display to be forced off state.	Used. (Controlled by LCD controller)

Pin Assignment

The following figure shows the pin assignment of LCD driver IC (LC75843UGA).

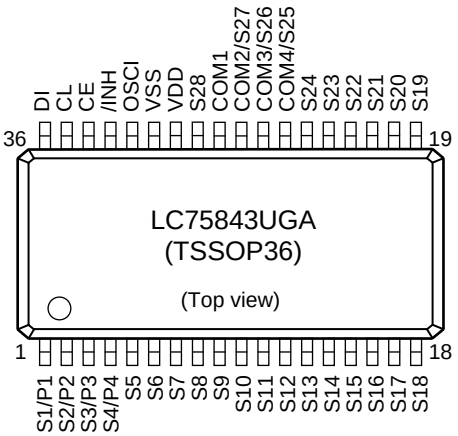


Figure 2. Pin Assignment of LCD driver IC (LC75843UGA)

Table 1. Pin function of LCD driver IC (LC75843UGA)

Pin name	Pin function
S1/P1	General-purpose port output pin. The S1/P1 pin can be used as a segment drive pin by control data (P0 to P2).
S2/P2	General-purpose port output pin. The S2/P2 pin can be used as a segment drive pin by control data (P0 to P2).
S3/P3	General-purpose port output pin. The S3/P3 pin can be used as a segment drive pin by control data (P0 to P2).
S4/P4	General-purpose port output pin. The S4/P4 pin can be used as a segment drive pin by control data (P0 to P2).
S5 to S24	Segment drive output pins.
S28	Segment drive output pin. When “S28 output off mode (DN=0)”, S28 is VSS level output. When “S28 output on mode (DN=1)”, S28 is segment output.
COM1	Common drive output pin.
COM2/S27	Common drive or segment drive output pin. The COM2/S27 pin can be used as a segment drive pin by control data (DT0, DT1).
COM3/S26	Common drive or segment drive output pin. The COM3/S26 pin can be used as a segment drive pin by control data (DT0, DT1).
COM4/S25	Common drive or segment drive output pin. The COM4/S25 pin can be used as a segment drive pin by control data (DT0, DT1).
OSCI	External clock input pin. When “Internal oscillator operating mode (OC=0)”, make sure to connect OSCI to GND. When “External clock input mode (OC=1)”, OSCI is used to input the external clock.
CE	Serial data transfer chip enable input pin.
CL	Serial data transfer synchronization clock input pin.
DI	Serial data transfer data input pin.
/INH	Display off control input pin. /INH=High (VDD) : Display ON /INH=Low (VSS) : Display forced off General-purpose output port pins (S1/P1 to S4/P4) are VSS level. Segment output pins (S5 to S24, and S28) are VSS level. Common output pins (COM1, COM2/S27, COM3/S26 and COM4/S25) are VSS level. The internal oscillator circuit is stopped. External clock input is inhibited. The reception of serial control data is possible. (Registers are updated)
VDD	Logic power supply pin for LCD driver IC. A power supply voltage of +4.5 [V] to +6.3 [V].
VSS	Ground pin. Must be connected all each board to the ground.

Serial Control Data Transfer Explanation

(1) Basic Timing

The LC75843UGA has several internal registers. These internal registers are written by CCB interface (Serial interface). Structure of transfer bits consists of CCB address and instruction data. First eight bits are CCB address (44h). The bit number of instruction data is different depending on an instruction. The serial control data is taken by the positive edge of the CL signal, which is latched by the negative edge of the CE signal. When the number of data in CE=VDD period is different from the defined number (96-bits and 48-bits), IC does not execute the instruction and holds the old state. Even when CL signal stops at high level, the CCB interface can be received. However, serial Control Data transfer timing (transfer form) is different. Therefore, when designing equipment, refer to the “Delivery specification for the LC75843UGA”.

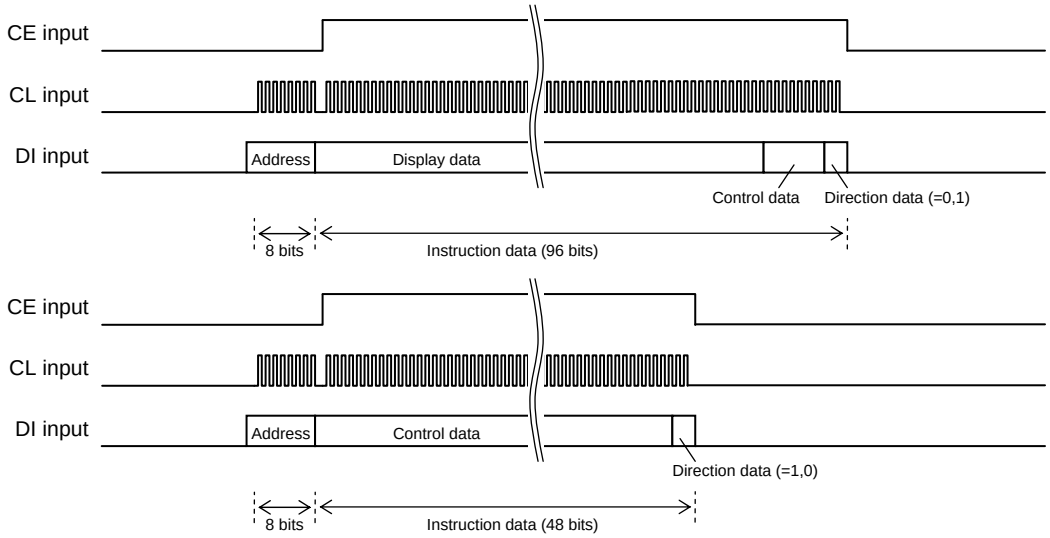


Figure 3. Basic timing when CL signal is stopped at the Low Level

Since the IC internal data is undefined when power supply is first applied, applications should set the /INH pin=Low (VSS) at the same time as power supply is applied to turn off the display (The S1/P1 to S4/P4, S5 to S24, COM4/S25, COM3/S26, COM2/S27, COM1 and S28 pins are outputted at the VSS level), and during this period send serial control data from the controller. The controller should then set the /INH pin=High (VDD) after the data transfer has completed. This procedure prevents meaningless display at power supply on.

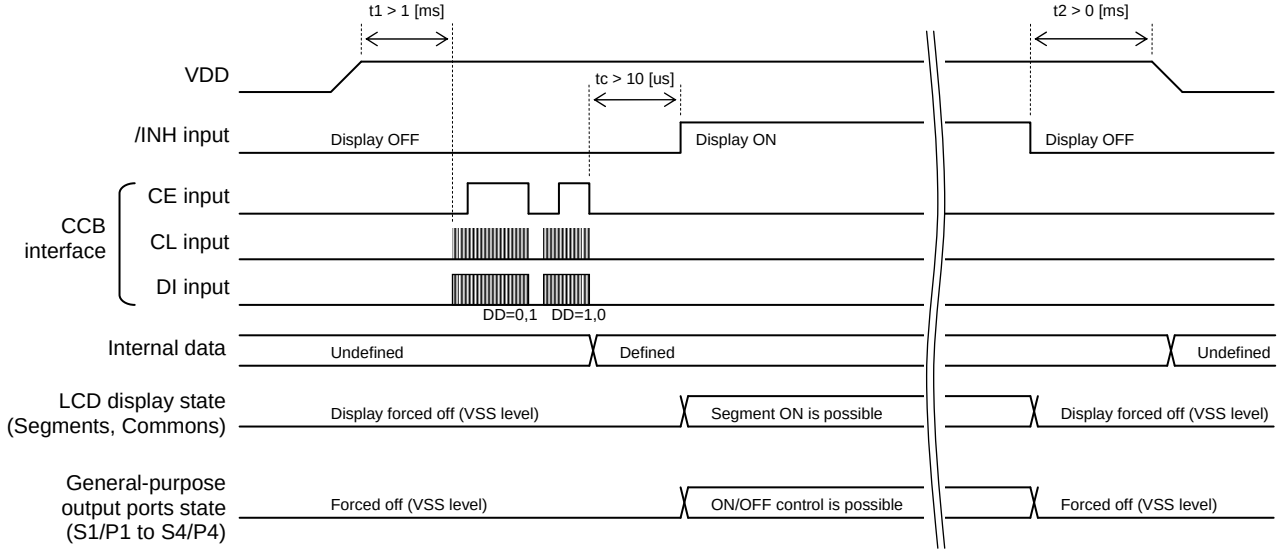


Figure 4. Basic timing of serial control data transfer

(2) Allowable Operating Ranges of the Serial Control Data Transfer

The following figure shows the specifications of the allowable operating ranges when CL signal is stopped at the low level.

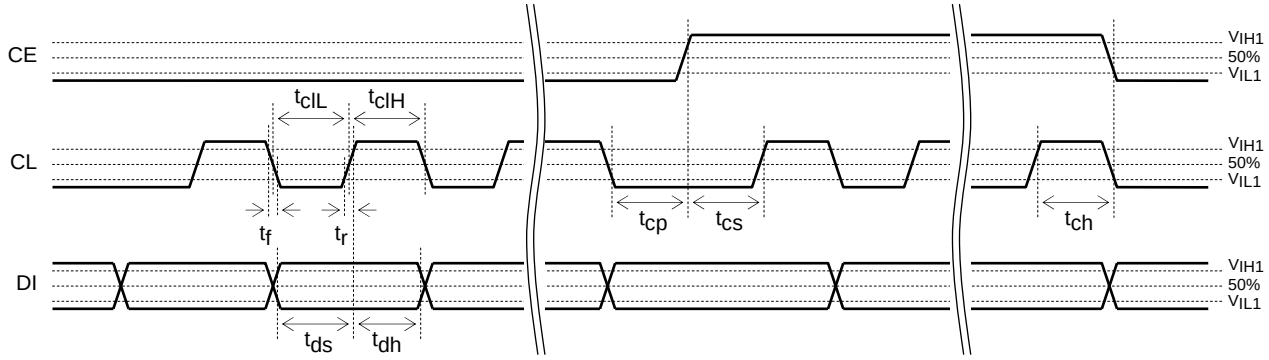


Figure 5. Allowable operating ranges of serial control data transfer

Table 2. Allowable operating ranges

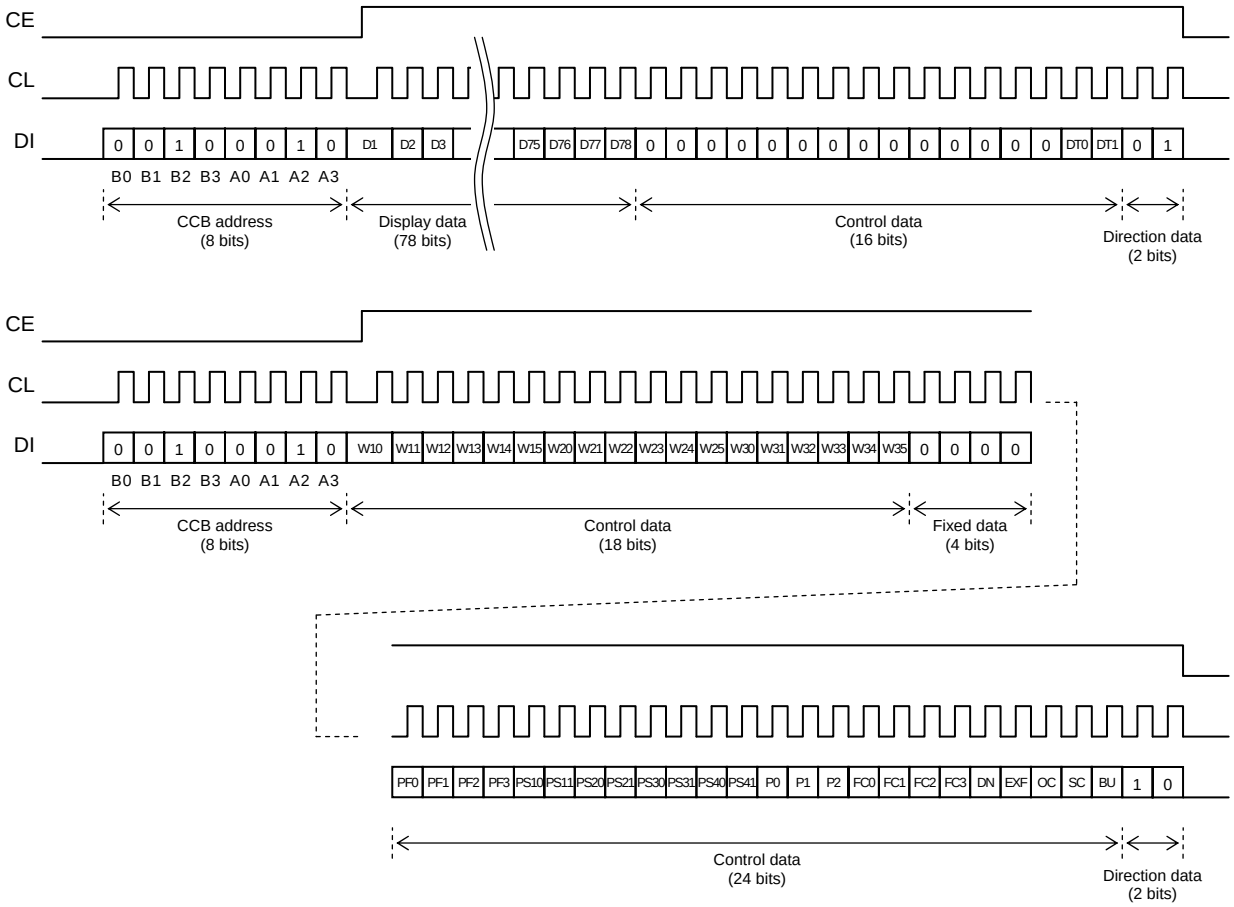
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	VDD	4.5		6.3	V
Input High Level Voltage	V_{IH1}	CE, CL, DI, /INH	0.4 V_{DD}		6.3	V
Input Low Level Voltage	V_{IL1}	CE, CL, DI, /INH	0		0.2 V_{DD}	V
Serial Data Transfer Synchronization Clock Frequency	f_{cl}	CL, $1/(t_{clL}+t_{clH})$			3.125	MHz
Data Setup Time	t_{ds}	CL, DI	160			ns
Data Hold Time	t_{dh}	CL, DI	160			ns
CE Wait Time	t_{cp}	CE, CL	160			ns
CE Setup Time	t_{cs}	CE, CL	160			ns
CE Hold Time	t_{ch}	CE, CL	160			ns
High Level Clock Pulse Width	t_{clH}	CL	160			ns
Low Level Clock Pulse Width	t_{clL}	CL	160			ns
Rise Time	t_r	CE, CL, DI		160		ns
Fall Time	t_f	CE, CL, DI		160		ns
/INH Switching Time	t_c	/INH, CE	10			us

These specifications show an example, and, we have a case to change these specifications without a notice for improvement. Therefore, it is not guaranteed for design as the mass production equipment. When designing equipment, refer to the “Delivery specification for the LC75843UGA”.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

(3) Allotment of Serial Control Data

The following figure shows the serial control data transfer form when the “1/3-duty drive mode” and CL signal is stopped at the low level.



B0 to B3, A0 to A3	: CCB address. (=44h)
D1 to D78	: Display data setting registers.
DT0, DT1	: LCD drive type (Duty ratio, Bias ratio) setting registers.
W10 to W15	: PWM duty setting registers of the PWM output function (ch1).
W20 to W25	: PWM duty setting registers of the PWM output function (ch2).
W30 to W35	: PWM duty setting registers of the PWM output function (ch3).
PF0 to PF3	: PWM output waveform frame frequency setting registers.
PS10, PS11	: General-purpose output port (S1/P1) function setting registers.
PS20, PS21	: General-purpose output port (S2/P2) function setting registers.
PS30, PS31	: General-purpose output port (S3/P3) function setting registers.
PS40, PS41	: General-purpose output port (S4/P4) function setting registers.
P0 to P2	: S1/P1 to S4/P4 output pins function setting registers.
FC0 to FC3	: LCD drive waveform frame frequency setting registers.
DN	: S28 pin function setting register.
EXF	: External clock operating frequency setting register. (When OC=1, EXF is valid.)
OC	: Fundamental clock operating mode setting register.
SC	: All segments turn off mode setting register.
BU	: Power saving mode setting register.

Explanation of the LCD drive control

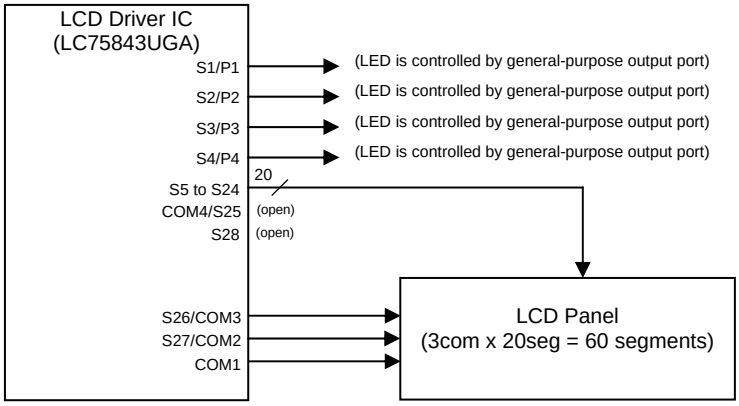


Figure 6. Peripheral circuits configuration example of the LCD driver outputs

(1) LCD Drive Waveform

It is explanation about the drive type of the 1/3-duty and 1/3-bias. The common outputs (COM1, COM2/S27 and COM3/S26) repeat VDD level, VSS level, 1/3 VDD level and 2/3 VDD level in turn. On the other hand, the segment outputs (S5 to S25, and S28) repeat VSS level, VDD level, 2/3 VDD level and 1/3 VDD level by a state of display ON/OFF (Display data setting register is 1/0). When the LCD segment is ON (It interrupt light), the potential difference of segment output and common output becomes VDD level. When the LCD segment is OFF (It penetrate light), the potential difference of segment output and common output becomes lower than 1/3 VDD level. This drive method assigns a third of a frame to control of ON/OFF of one segment. In addition, this drive method uses the 2/3 VDD level and 1/3 VDD level divided in three between VDD and VSS. Thus, this drive method is called the “1/3-duty and 1/3-bias drive”. When set the “1/3-duty drive mode”, the following figure shows the LCD drive waveform.

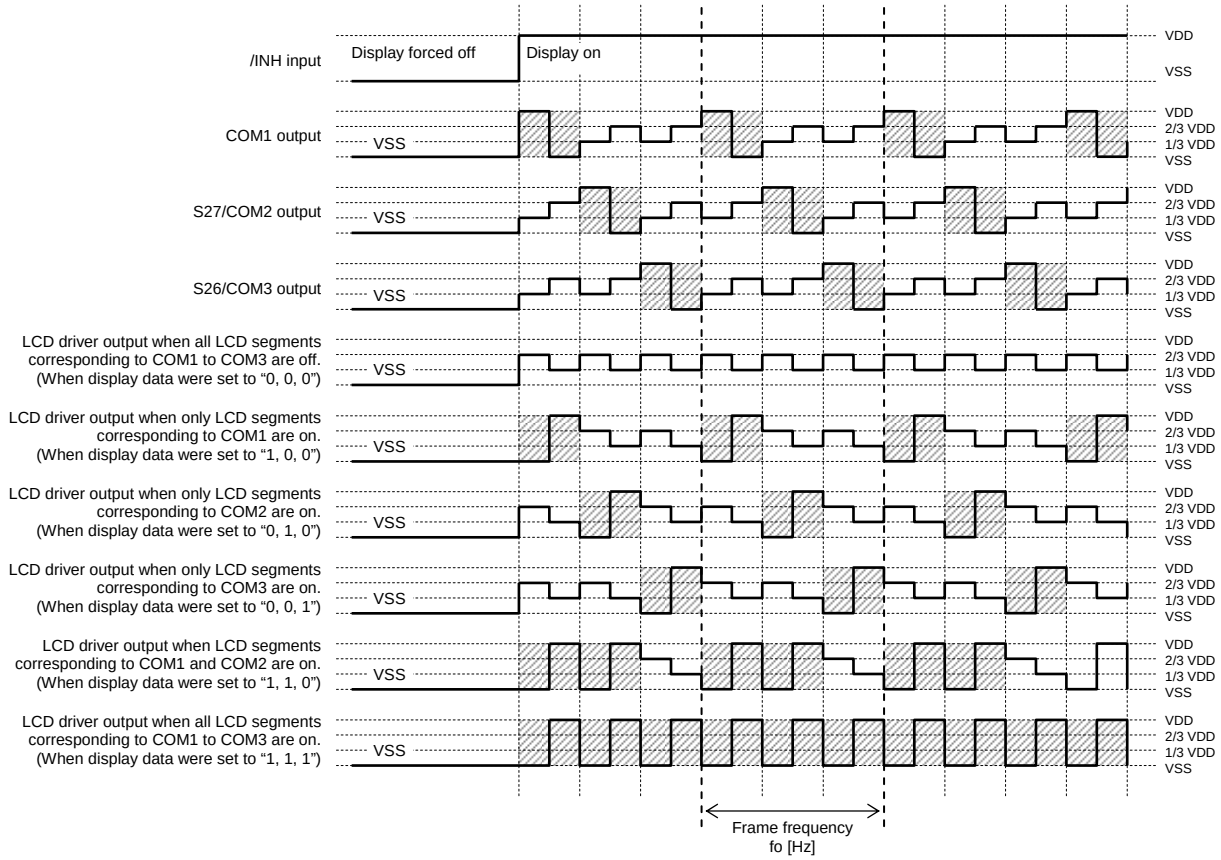


Figure 7. LCD driver output waveform

(2) LCD Drive Type Setting (DT0, DT1)

The registers of the DT0 and DT1 can set the LCD drive type from 1/1-duty to 1/4-duty. The LCD system configuration example is LCD panel of the 1/3-duty drive used. Therefore, this system sets DT0=1 and DT1=0.

DT0	DT1	LCD drive type	Output pins state			
			COM1	COM2/S27	COM3/S26	COM4/S25
0	0	1/4-duty and 1/3-bias drive type	COM1	COM2	COM3	COM4
1	**0**	**1/3-duty and 1/3-bias drive type**	**COM1**	**COM2**	**COM3**	**S25**
0	1	1/2-duty and 1/2-bias drive type	COM1	COM2	S26	S25
1	1	Static (1/1-duty) drive type	COM1	S27	S26	S25

(3) S28 Pin Function Setting (DN)

The DN register can set the “Segment output of the S28 output pin” or “VSS level output of the S28 output pin”. The LCD system configuration example does not use S28 output pin. Therefore, this system sets DN=0.

DN	S28 output pin state
0	**VSS level output**
1	S28 segment output

(4) Display Data Setting (D1 to D78)

The registers from D1 to D78 set the LCD segment ON/OFF, or these registers set the general-purpose output port (P1 to P4) of high level output or low level output. The LCD system configuration example is the “1/3-duty drive mode”, and LCD segments from S5 to S24 used. Therefore, set the LCD display data from D13 to D72. In addition, the pins from S1/P1 to S4/P4 use general-purpose output port function. Therefore, set the general-purpose output ports (P1 to P4) of high level output or low level output by the LCD display data to D1, D4, D7 and D10. About the control method of “Display data setting registers (D1 to D12)”, refer to paragraph (3) of “Explanation of the LED Control by General-purpose Output Ports”.

When set the “1/3-duty drive mode”, the following table shows the relation between the “Display data setting registers (D13 to D72)” and the segment outputs and the common outputs.

Output pin	COM1	COM2/S27	COM3/S26	Notes
S5	**D13**	**D14**	**D15**	
S6	**D16**	**D17**	**D18**	
S7	**D19**	**D20**	**D21**	
S8	**D22**	**D23**	**D24**	
S9	**D25**	**D26**	**D27**	
S10	**D28**	**D29**	**D30**	
S11	**D31**	**D32**	**D33**	
S12	**D34**	**D35**	**D36**	
S13	**D37**	**D38**	**D39**	
S14	**D40**	**D41**	**D42**	
S15	**D43**	**D44**	**D45**	
S16	**D46**	**D47**	**D48**	
S17	**D49**	**D50**	**D51**	
S18	**D52**	**D53**	**D54**	
S19	**D55**	**D56**	**D57**	
S20	**D58**	**D59**	**D60**	
S21	**D61**	**D62**	**D63**	
S22	**D64**	**D65**	**D66**	
S23	**D67**	**D68**	**D69**	
S24	**D70**	**D71**	**D72**	
COM4/S25	D73	D74	D75	Thes display data are unused, and D73 to D75 sets the all “0”.
S28	D76	D77	D78	Thes display data are unused, and D76 to D78 sets the all “0”.

For example, the following table shows the relation between the “Display data setting register” and S5 output pin state.

Display data			S5 output pin state
D13	D14	D15	
0	0	0	All LCD segments corresponding to COM1 to COM3 are off.
1	0	0	LCD segments corresponding to COM1 is on and LCD segments corresponding to COM2 and COM3 are off.
0	1	0	LCD segments corresponding to COM2 is on and LCD segments corresponding to COM1 and COM3 are off.
1	1	0	LCD segments corresponding to COM1 and COM2 are on and LCD segments corresponding to COM3 is off.
0	0	1	LCD segments corresponding to COM3 is on and LCD segments corresponding to COM1 and COM2 are off.
1	0	1	LCD segments corresponding to COM1 and COM3 are on and LCD segments corresponding to COM2 is off.
0	1	1	LCD segments corresponding to COM2 and COM3 are on and LCD segments corresponding to COM1 is off.
1	1	1	All LCD segments corresponding to COM1 to COM3 are on.

Explanation of the LED Control by General-purpose Output Ports

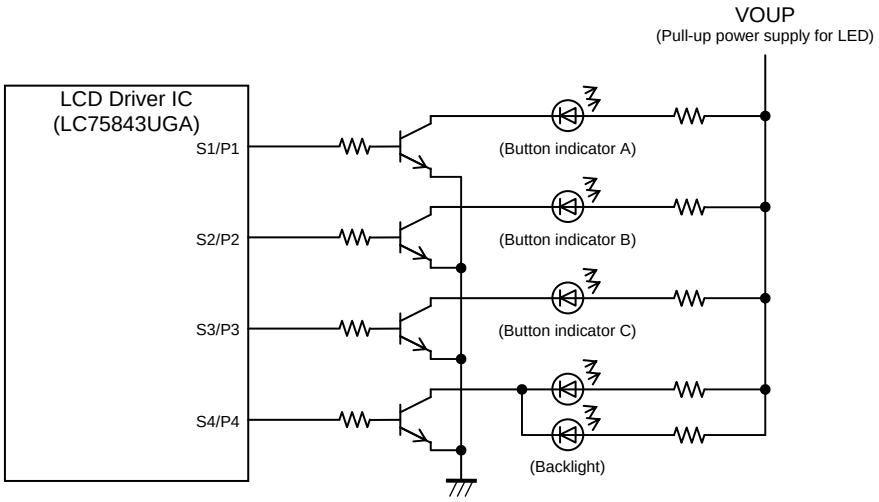


Figure 8. Peripheral circuits configuration example of the general-purpose output ports

(1) LED Control Waveform

The LC75843UGA has up to four general-purpose output ports. In addition, the PWM output function has up to 3ch and can perform brightness adjustment of the LED individually for each channel. The brightness of the LED has a method to adjust a forward current of LED flowing at the time of ON, or there is pulse width modulation (PWM) control to adjust the apparent brightness by repeating ON and OFF at high speed. The LED looks bright if the ON time per unit time by PWM control is long. In addition, it looks dark if the ON time per unit time by PWM control is short. When LED is always turn on (Brightness is 100%), the consumption electric current is maximum. When LED is ON, the LED uses electricity, and when LED is OFF, the LED does not use electricity. Thus, it can set the low power consumption by PWM control. When used the general-purpose output port, the following figure shows the LED control waveform.

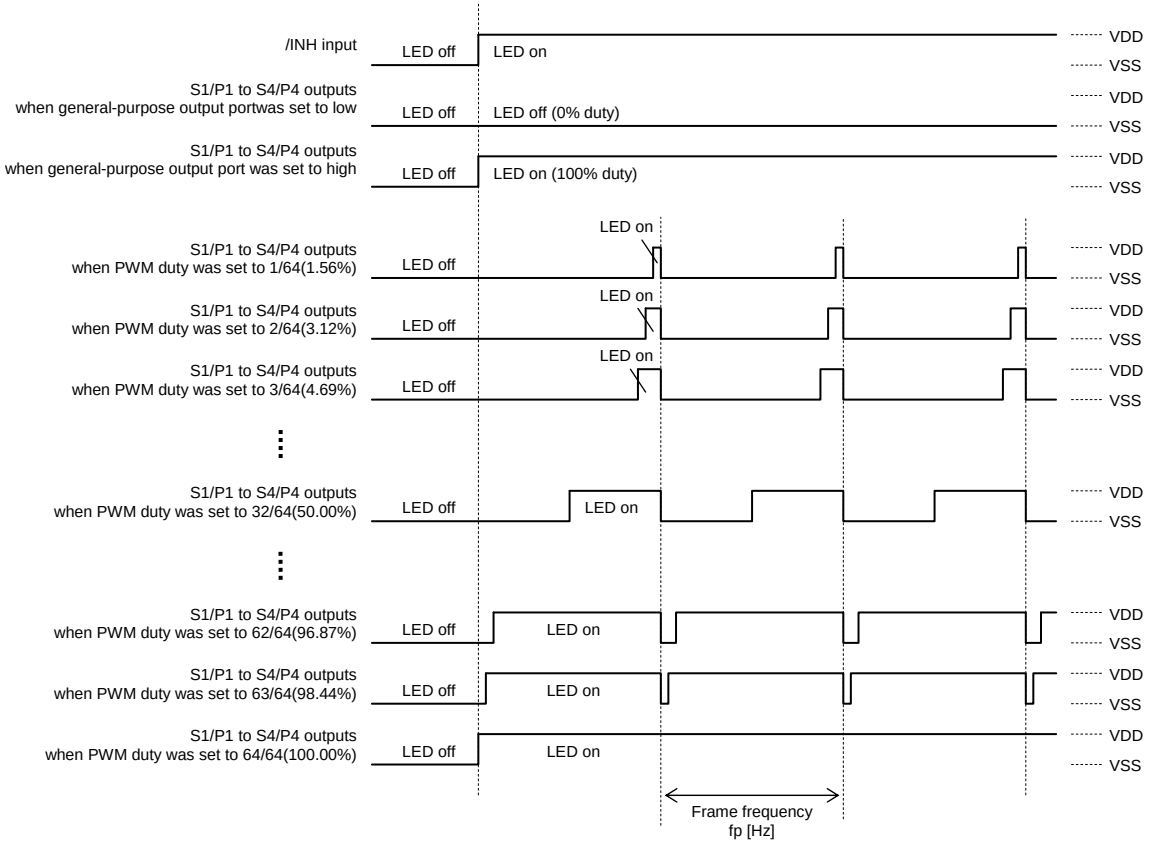


Figure 9. General-purpose port output waveform

(2) S1/P1 to S4/P4 Output Pins Function Setting (P0 to P2)

The registers from P0 to P2 can set the “Output pins from S1/P1 to S4/P4 of the segment output port” or “Output pins from S1/P1 to S4/P4 of the general-purpose output port”. The LCD system configuration example controls LED by general-purpose output port of the S1/P1 to S4/P4 output pins. Therefore, this system sets P0=1, P1=0 and P2=0.

P0	P1	P2	Output pin state			
			S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	**0**	**0**	**P1**	**P2**	**P3**	**P4**
1	0	1	S1	S2	S3	S4
1	1	0	S1	S2	S3	S4
1	1	1	S1	S2	S3	S4

S1 to S4 : Segment output ports
P1 to P4 : General-purpose output ports

(3) General-purpose Ports (P1 to P4) Function Setting (PS10,PS11,PS20,PS21,PS30,PS31,PS40 and PS41)

The registers from PS10 and PS11 can set the “General-purpose output function”, “Clock output function”, or “PWM output function” of the general-purpose output port (P1). In addition, PS20, PS21, PS30, PS31, PS40 and PS41 registers can set the “General-purpose output function” or “PWM output function” of the general-purpose output ports (P2 to P4). The general-purpose output function outputs general-purpose output ports (P1 to P4) of high level or low level by “Display data setting registers (D1 to D12)”. The clock output function outputs internal oscillator clock (fosc) or external clock input (fck) of the 1/2 frequency division or 1/8 frequency division. This function can set only general-purpose output port (P1). Therefore, when stop the clock, the “Display data setting register (D1)” by general-purpose output function sets the “0”, and general-purpose output port (P1) outputs low level. The PWM output function has up to 3ch and can perform brightness adjustment of the LED individually for each channel. However, PWM duty setting register (W10 to W15, W20 to W25, and W30 to W35) does not have a setting function of 0%-duty. Therefore when you want to turn off the LED, the “Display data setting registers (D1 to D12)” by general-purpose output function set the “0”, and general-purpose output ports (P1 to P4) output low level.

PS10	PS11	General-purpose output port (P1) function
0	0	General-purpose output function : High level or low level output
1	0	Clock output function : Outputs a clock of the fosc/2 frequency
0	1	Clock output function : Outputs a clock of fosc/8 frequency
1	1	PWM output function (ch1) : Controlled by PWM duty setting register from W10 to W15

PS20	PS21	General-purpose output port (P2) function
0	0	General-purpose output function : High level or low level output
1	0	PWM output function (ch1) : Controlled by PWM duty setting register from W10 to W15
0	1	PWM output function (ch2) : Controlled by PWM duty setting register from W20 to W25
1	1	PWM output function (ch3) : Controlled by PWM duty setting register from W30 to W35

PS30	PS31	General-purpose output port (P3) function
0	0	General-purpose output function : High level or low level output
1	0	PWM output function (ch1) : Controlled by PWM duty setting register from W10 to W15
0	1	PWM output function (ch2) : Controlled by PWM duty setting register from W20 to W25
1	1	PWM output function (ch3) : Controlled by PWM duty setting register from W30 to W35

PS40	PS41	General-purpose output port (P4) function
0	0	General-purpose output function : High level or low level output
1	0	PWM output function (ch1) : Controlled by PWM duty setting register from W10 to W15
0	1	PWM output function (ch2) : Controlled by PWM duty setting register from W20 to W25
1	1	PWM output function (ch3) : Controlled by PWM duty setting register from W30 to W35

The LCD system configuration example uses general-purpose output port function from S1/P1 to S4/P4. The following table shows the relation between the “Display data setting registers (D1 to D12)” and general-purpose output ports (P1 to P4) of high level or low level.

Display data	Controlled output pin	Notes
D1	S1/P1	When PS10=0, PS11=0 and D1=0, S1/P1 is outputted at the low level. When PS10=0, PS11=0 and D1=1, S1/P1 is outputted at the high level. When “PS10, PS11” are not “0, 0”, D1 is invalid.
D4	S2/P2	When PS20=0, PS21=0 and D4=0, S2/P2 is outputted at the low level. When PS20=0, PS21=0 and D4=1, S2/P2 is outputted at the high level. When “PS20, PS21” are not “0, 0”, D4 is invalid.
D7	S3/P3	When PS30=0, PS31=0 and D7=0, S3/P3 is outputted at the low level. When PS30=0, PS31=0 and D7=1, S3/P3 is outputted at the high level. When “PS30, PS31” are not “0, 0”, D7 is invalid.
D10	S4/P4	When PS40=0, PS41=0 and D10=0, S4/P4 is outputted at the low level. When PS40=0, PS41=0 and D10=1, S4/P4 is outputted at the high level. When “PS40, PS41” are not “0, 0”, D10 is invalid.

When control the LED in the system configuration example of the Figure 8, a register setting example is shown below.

(Case 1) When all LED were set to OFF.

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
OFF			OFF			OFF			OFF		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
0	0	0	0	0	0	0	0	0	0	0	0

(Case 2) When backlight-LED was set to ON (Brightness is 50%).

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
OFF			OFF			OFF			**ON (W30 to W35=1,1,1,1,1,0)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
0	0	0	0	0	0	0	0	0	**1**	**1**	0

(Case 3) When backlight-LED was set to ON (Brightness is 50%) and button indicator A-LED was set to ON (Brightness is 50%).

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON (W10 to W15=1,1,1,1,1,0)			OFF			OFF			**ON (W30 to W35=1,1,1,1,1,0)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
1	**1**	0	0	0	0	0	0	0	**1**	**1**	0

(Case 4) When backlight-LED was set to ON (Brightness is 50%) and button indicator B-LED was set to ON (Brightness is 50%).

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
OFF			**ON (W10 to W15=1,1,1,1,1,0)**			OFF			**ON (W30 to W35=1,1,1,1,1,0)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
0	0	0	**1**	**0**	0	0	0	0	**1**	**1**	0

(Case 5) When backlight-LED was set to ON (Brightness is 50%) and button indicator A/B/C-LED were set to ON (Brightness is 50%).

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON (W10 to W15=1,1,1,1,1,0)			**ON (W10 to W15=1,1,1,1,1,0)**			**ON (W20 to W25=1,1,1,1,1,0)**			**ON (W30 to W35=1,1,1,1,1,0)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
1	**1**	0	**1**	**0**	0	**0**	**1**	0	**1**	**1**	0

(Case 6) When button indicator C-LED was changed from 50% to 79.69%.

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON (W10 to W15=1,1,1,1,1,0)			**ON (W10 to W15=1,1,1,1,1,0)**			**ON (W20 to W25=0,1,0,0,1,1)**			**ON (W30 to W35=1,1,1,1,1,0)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
1	**1**	0	**1**	**0**	0	**0**	**1**	0	**1**	**1**	0

(Case 7) When backlight-LED was set to OFF.

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON (W10 to W15=1,1,1,1,1,0)			**ON (W10 to W15=1,1,1,1,1,0)**			**ON (W20 to W25=0,1,0,0,1,1)**			OFF		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
1	**1**	0	**1**	**0**	0	**0**	**1**	0	0	0	0

(Case 8) When all LED were set to ON (Brightness is 100%).

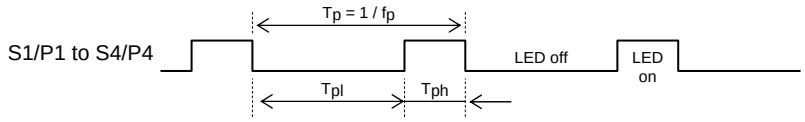
General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON (W10 to W15=1,1,1,1,1,1)			**ON (W10 to W15=1,1,1,1,1,1)**			**ON (W20 to W25=1,1,1,1,1,1)**			**ON (W30 to W35=1,1,1,1,1,1)**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
1	**1**	0	**1**	**0**	0	**0**	**1**	0	**1**	**1**	0

or

General-purpose output port (P1) control			General-purpose output port (P2) control			General-purpose output port (P3) control			General-purpose output port (P4) control		
ON			**ON**			**ON**			**ON**		
PS10	PS11	D1	PS20	PS21	D4	PS30	PS31	D7	PS40	PS41	D10
0	0	**1**	0	0	**1**	0	0	**1**	0	0	**1**

(4) PWM Duty Setting (W10 to W15, W20 to W25, W30 to W35)

The registers from W10 to W15, from W20 to W25, and from W30 to W35 can set the pulse width of the PWM output. The PWM duty setting has up to 3ch and can perform brightness adjustment of the LED individually for each channel. However, the PWM duty setting register (W10 to W15, W20 to W25, and W30 to W35) does not have a setting function of the 0%-duty. Therefore when you want to turn off the LED, the “Display data setting registers (D1 to D12)” by general-purpose output function set the “0”, and general-purpose output ports (P1 to P4) output low level.



PWM duty = (T_{ph} / (T_{pl}+T_{ph}))

Wx0	Wx1	Wx2	Wx3	Wx4	Wx5	PWM output pulse width (PWM duty)
0	0	0	0	0	0	1/64 (1.56%)
1	0	0	0	0	0	2/64 (3.12%)
0	1	0	0	0	0	3/64 (4.69%)
1	1	0	0	0	0	4/64 (6.25%)
0	0	1	0	0	0	5/64 (7.81%)
1	0	1	0	0	0	6/64 (9.38%)
0	1	1	0	0	0	7/64 (10.94%)
1	1	1	0	0	0	8/64 (12.50%)
0	0	0	1	0	0	9/64 (14.06%)
1	0	0	1	0	0	10/64 (15.62%)
0	1	0	1	0	0	11/64 (17.19%)
1	1	0	1	0	0	12/64 (18.75%)
0	0	1	1	0	0	13/64 (20.31%)
1	0	1	1	0	0	14/64 (21.87%)
0	1	1	1	0	0	15/64 (23.44%)
1	1	1	1	0	0	16/64 (25.00%)
0	0	0	0	1	0	17/64 (26.56%)
1	0	0	0	1	0	18/64 (28.12%)
0	1	0	0	1	0	19/64 (29.69%)
1	1	0	0	1	0	20/64 (31.25%)
0	0	1	0	1	0	21/64 (32.81%)
1	0	1	0	1	0	22/64 (34.37%)
0	1	1	0	1	0	23/64 (35.94%)
1	1	1	0	1	0	24/64 (37.50%)
0	0	0	1	1	0	25/64 (39.06%)
1	0	0	1	1	0	26/64 (40.62%)
0	1	0	1	1	0	27/64 (42.19%)
1	1	0	1	1	0	28/64 (43.75%)
0	0	1	1	1	0	29/64 (45.31%)
1	0	1	1	1	0	30/64 (46.87%)
0	1	1	1	1	0	31/64 (48.44%)
1	1	1	1	1	0	32/64 (50.00%)

Wx0	Wx1	Wx2	Wx3	Wx4	Wx5	PWM output pulse width (PWM duty)
0	0	0	0	0	1	33/64 (51.56%)
1	0	0	0	0	1	34/64 (53.12%)
0	1	0	0	0	1	35/64 (54.69%)
1	1	0	0	0	1	36/64 (56.25%)
0	0	1	0	0	1	37/64 (57.81%)
1	0	1	0	0	1	38/64 (59.37%)
0	1	1	0	0	1	39/64 (60.94%)
1	1	1	0	0	1	40/64 (62.50%)
0	0	0	1	0	1	41/64 (64.06%)
1	0	0	1	0	1	42/64 (65.62%)
0	1	0	1	0	1	43/64 (67.19%)
1	1	0	1	0	1	44/64 (68.75%)
0	0	1	1	0	1	45/64 (70.31%)
1	0	1	1	0	1	46/64 (71.87%)
0	1	1	1	0	1	47/64 (73.44%)
1	1	1	1	0	1	48/64 (75.00%)
0	0	0	0	1	1	49/64 (76.56%)
1	0	0	0	1	1	50/64 (78.12%)
0	1	0	0	1	1	51/64 (79.69%)
1	1	0	0	1	1	52/64 (81.25%)
0	0	1	0	1	1	53/64 (82.81%)
1	0	1	0	1	1	54/64 (84.37%)
0	1	1	0	1	1	55/64 (85.94%)
1	1	1	0	1	1	56/64 (87.50%)
0	0	0	1	1	1	57/64 (89.06%)
1	0	0	1	1	1	58/64 (90.62%)
0	1	0	1	1	1	59/64 (92.19%)
1	1	0	1	1	1	60/64 (93.75%)
0	0	1	1	1	1	61/64 (95.31%)
1	0	1	1	1	1	62/64 (96.87%)
0	1	1	1	1	1	63/64 (98.44%)
1	1	1	1	1	1	64/64 (100.00%)

x : 1 to 3

Explanation of the Instruction Data

(1) Fundamental Clock Operating Mode Setting (OC, EXF)

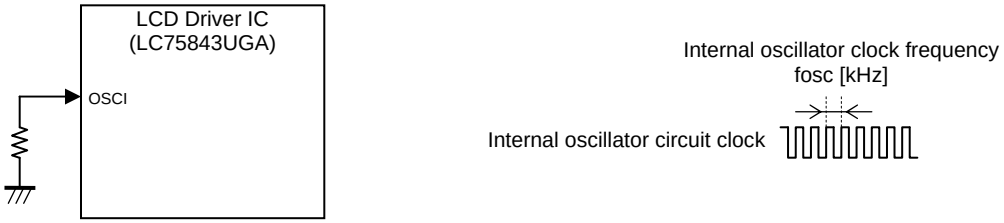


Figure 10. Peripheral circuits configuration example of the external clock input pin

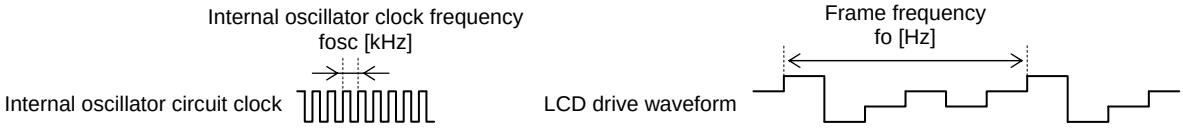
The OC register can set the “Internal oscillator operating mode” or “External clock input operating mode”. Furthermore, when OC register sets the “External clock input operating mode (OC=1)”, the EXF register can set the division ratio. The EXF register can set the division ratio a clock to input from OSCI pin becomes 300 [kHz](Typ.) and 38 [kHz](Typ.). However, when set the “External clock 38kHz input mode (OC=1 and EXF=1)”, please be careful because PWM output function is invalidity. The LCD system configuration example sets OC=0 and EXF=0 to use the “Internal oscillator operating mode”.

OC	EXF	Fundamental clock operating mode	OSCI input pin state
0	**0/1**	**Internal oscillator operating mode**	**Connect to GND**
1	0	External clock 300kHz input mode	Inputs a clock of 300 [kHz](Typ.)
1	1	External clock 38kHz input mode	Inputs a clock of 38 [kHz](Typ.)

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

(2) LCD Drive Waveform Frame Frequency Setting (FC0 to FC3)

The registers from FC0 to FC3 can set the frame frequency (fo) of the common and segment output waveform. The frame frequency (frame ratio) setting of the LCD drive waveform is different by “Fundamental clock operating mode setting register (OC)” and “External clock operating frequency setting register (EXF)”.



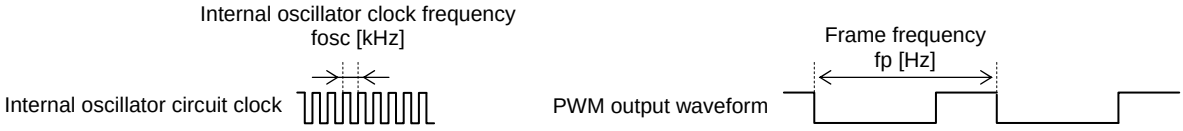
The LCD system configuration example sets OC=0 to use the “Internal oscillator operating mode”. When sets OC=0, the following table shows the frame frequency of the LCD drive waveform.

FC0	FC1	FC2	FC3	Internal oscillator operating mode (OC=0)	
				LCD drive waveform frame ratio	LCD drive waveform frame frequency fo [Hz] (Internal oscillator clock frequency is fosc=300 [kHz](typ.))
0	0	0	0	fosc / 6144	48.83
0	0	0	1	fosc / 5376	55.80
0	0	1	0	fosc / 4608	65.10
0	0	1	1	fosc / 3840	78.12
0	1	0	0	fosc / 3456	86.80
0	1	0	1	fosc / 3072	97.66
0	1	1	0	fosc / 2688	111.61
0	1	1	1	fosc / 2304	130.21
1	0	0	0	fosc / 2112	142.04
1	0	0	1	fosc / 1920	156.25
1	0	1	0	fosc / 1728	173.61
1	0	1	1	fosc / 1536	195.31
1	1	0	0	fosc / 1344	223.21
1	1	0	1	fosc / 1152	260.42
1	1	1	0	fosc / 960	312.50
1	1	1	1	fosc / 768	390.62

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

(3) PWM Output Waveform Frame Frequency Setting (PF0 to PF3)

The registers from PF0 to PF3 can set the PWM output frame frequency (fp) of the general-purpose output port. When set the “External clock input operating mode setting (OC = 1)” and “External clock 38kHz input mode setting (EXF=1)”, these registers are invalid.



The LCD system configuration example is “Internal oscillator operating mode” operated. Therefore, this system sets OC=0. When sets OC=0, the following table shows the frame frequency (fp) of the PWM output waveform.

PF0	PF1	PF2	PF3	Internal oscillator operating mode (OC=0)	
				PWM output waveform frame ratio	PWM output waveform frame frequency fp [Hz] (Internal oscillator clock frequency is fosc=300 [kHz](typ.))
0	0	0	0	fosc / 1536	195.31
1	0	0	0	fosc / 1408	213.07
0	1	0	0	fosc / 1280	234.37
1	1	0	0	fosc / 1152	260.42
0	0	1	0	fosc / 1024	292.97
1	0	1	0	fosc / 896	334.82
0	1	1	0	fosc / 768	390.62
1	1	1	0	fosc / 640	468.75
0	0	0	1	fosc / 512	585.94
1	0	0	1	fosc / 384	781.25
0	1	0	1	fosc / 256	1171.87
1	1	0	1	fosc / 896	334.82
0	0	1	1	fosc / 896	334.82
1	0	1	1	fosc / 896	334.82
0	1	1	1	fosc / 896	334.82
1	1	1	1	fosc / 896	334.82

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

(4) All Segments Turn Off Mode Setting (SC)

The SC register can set the “Normal mode” or “All segments turn off mode”. The LC75843UGA can display forced turn off by the /INH pin. When sets /INH pin=Low (VSS), segment outputs (S5 to S25, and S28), common outputs (COM1, COM2/S27 and COM3/S26) and general-purpose port outputs (S1/P1 to S4/P4) are outputted at the all VSS level. In addition, it can display OFF (turn off the segments) by controllable SC register from the software of the LCD controller. When sets SC=1, segment outputs (S5 to S25, and S28) are outputted at the all off waveform.

/INH pin	SC register	Output pin state		
		Segment outputs (S5 to S25, and S28)	Common output (COM1, COM2/S27 and COM3/S26)	General-purpose port outputs (S1/P1 to S4/P4)
Low (VSS)	0/1	All segment outputs are VSS level	All common outputs are VSS level	All general-purpose port outputs are VSS level
High (VDD)	0	Segments can output ON waveform	Common outputs are scan drive waveform	General-purpose outputs or PWM waveform
	1	All segment outputs are OFF waveform	Common outputs are scan drive waveform	General-purpose outputs or PWM waveform

The LCD system configuration example is LCD panel of the 1/3-duty drive used. Therefore, when set “1/3-duty drive mode (DT0=1 and DT1=0)”, the following figure shows the LCD drive waveform.

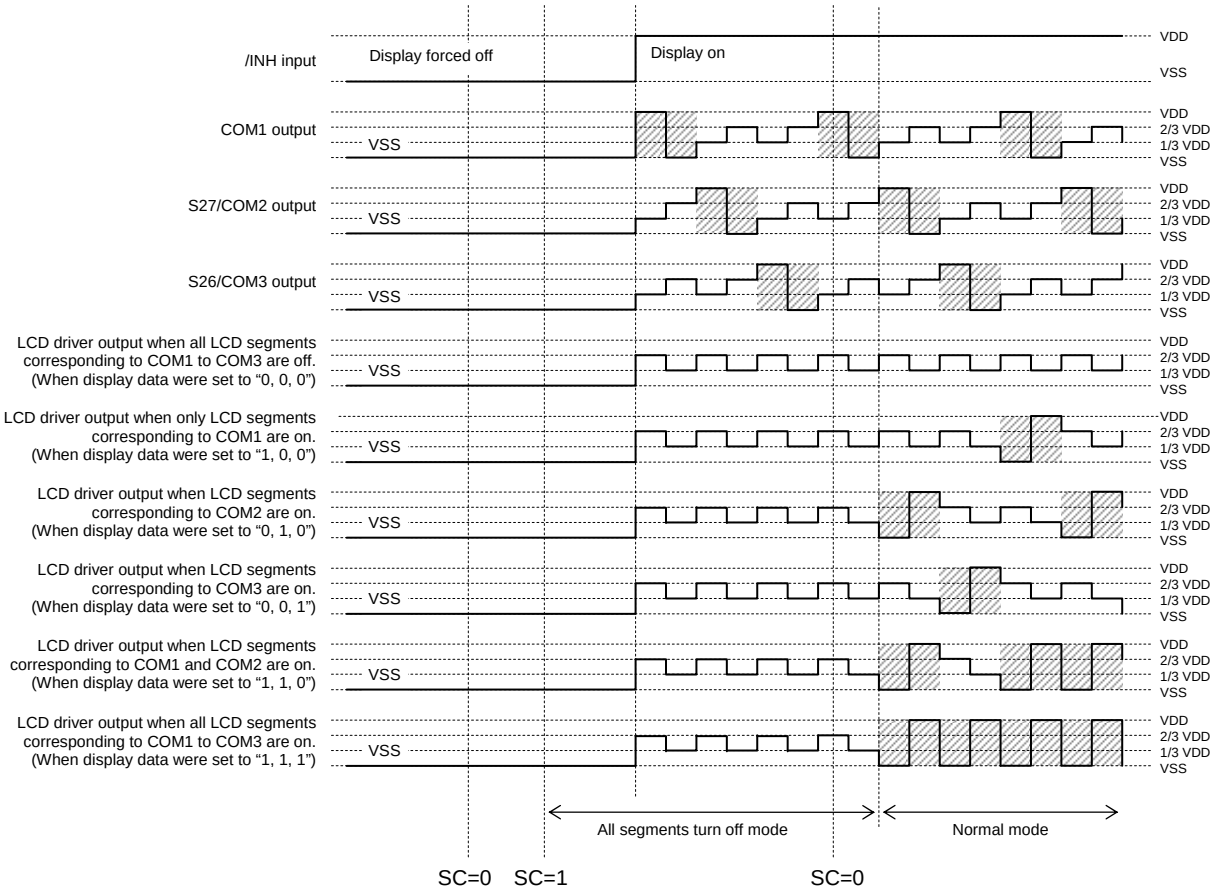


Figure 11. LCD driver output waveform when SC is set

(5) Power Saving Mode Setting (BU)

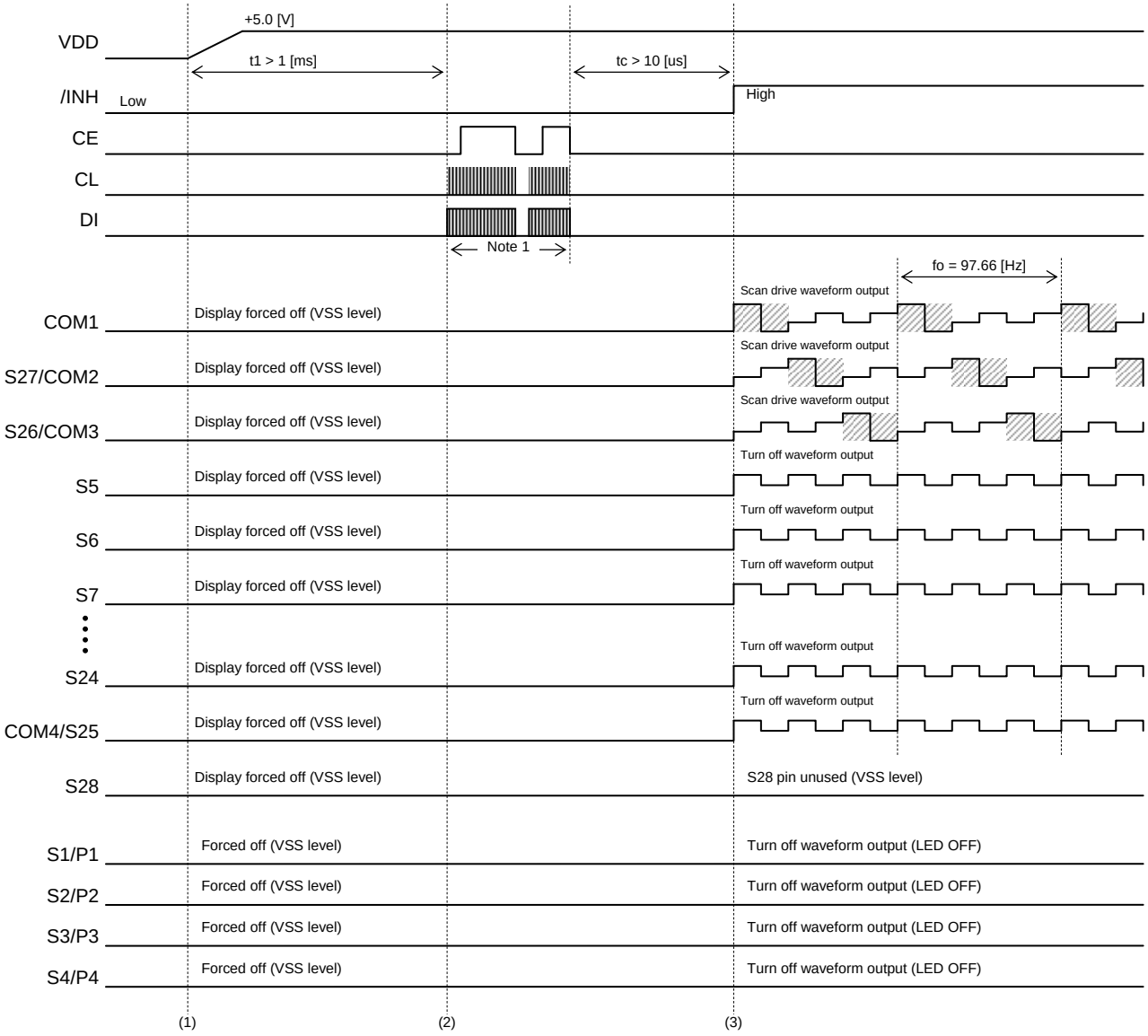
The BU register can set the “Normal mode” or “Power saving mode”. The LC75843UGA built-in the “Power saving mode” as a low power consumption mode. When set the “Power saving mode”, the internal oscillator circuit is stopped, and external clock input is inhibited and common / segment output pins are outputted at the VSS level. However, the output pins from S1/P1 to S4/P4 can output of high level or low level as a general-purpose output function by “Display data setting registers (D1 to D12)”. (PWM output function is invalid)

BU	Low power consumption mode	Internal operating conditions
0	Normal mode	Normal mode
1	Power saving mode	• When output pins from S1/P1 to S4/P4 set the general-purpose output port, the output pins from S1/P1 to S4/P4 can use only a general-purpose output function of high level or low level. • Segment output pins (S5 to S25, and S28) are VSS level. • Common output pins (COM1, COM2/S27 and COM3/S26) are VSS level. • The internal oscillator circuit is stopped. • External clock input is inhibited. • The reception of serial control data is possible. (Registers are updated)

Software Control Example of the LCD Controller

(1) Timing Chart From Power-on State to LCD Display ON

First, the following figure shows the timing waveform from power-on state to initial setting and LCD display ON in the LCD system configuration example.



< Operation sequence >

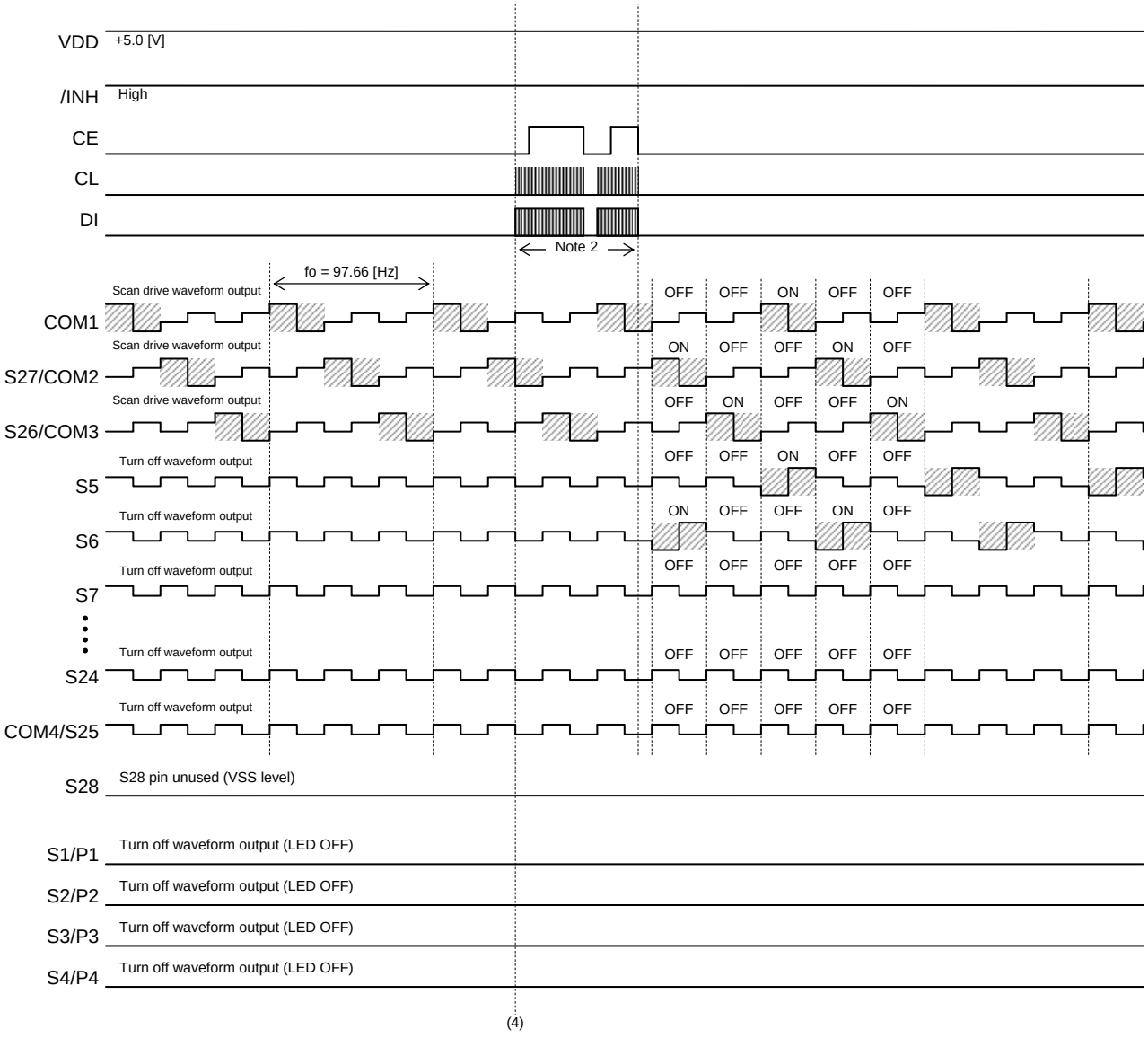
(1) Power-on.
(2) The initial setting command is transferred after passage of “Serial data input wait time (t1 > 1 [ms])”.
(3) The display forced off is cancelled by setting the /INH pin to High(VDD) after passage of “Command execute wait time (tc > 10 [us])”.

< Transfer instruction data >

Note 1 : CCB address = (44)h, D1 to D12= all “0” data, D13 to D78= all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=0 and PS11=0 (S1/P1=Low level general-purpose output),
PS20=0 and PS21=0 (S2/P2=Low level general-purpose output),
PS30=0 and PS31=0 (S3/P3=Low level general-purpose output),
PS40=0 and PS41=0 (S4/P4=Low level general-purpose output),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(2) Timing Chart of the LCD Display Contents Change

Next, the following figure shows the timing waveform of the LCD display contents change. For example, when S5 segment corresponding to COM1 is ON and S6 segment corresponding to COM2 is ON, the following figures shows the segment to change.



< Operation sequence >

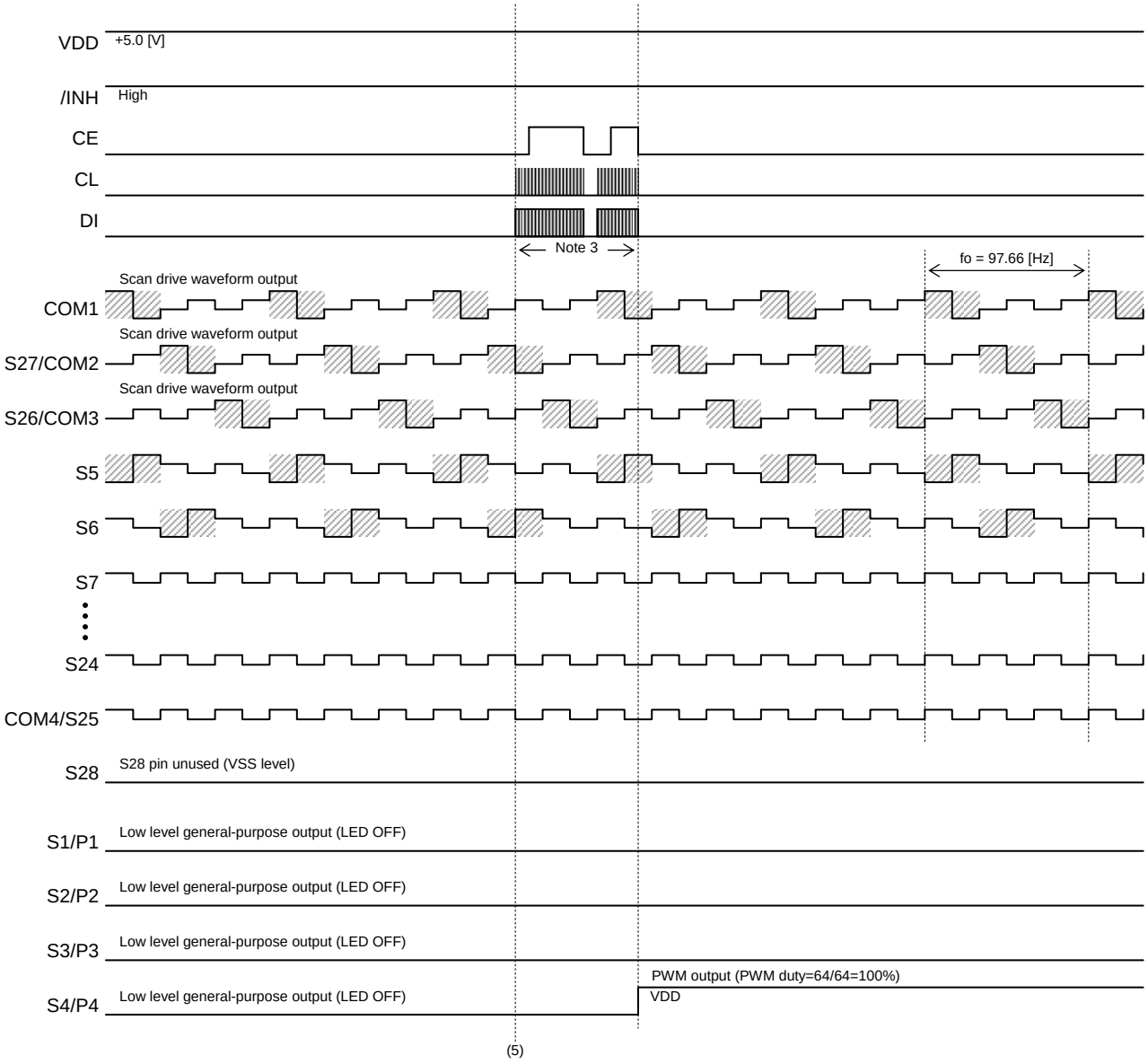
(4) The command of the LCD display change is transferred.

< Transfer instruction data >

Note 2 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=0 and PS11=0 (S1/P1=Low level general-purpose output),
PS20=0 and PS21=0 (S2/P2=Low level general-purpose output),
PS30=0 and PS31=0 (S3/P3=Low level general-purpose output),
PS40=0 and PS41=0 (S4/P4=Low level general-purpose output),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(3) Timing Chart of the Setting to Turn on the LED of Backlight

Next, the following figure shows the timing waveform of turn on the LED of backlight (Brightness is 100%) connecting to S4/P4 output pin.



< Operation sequence >

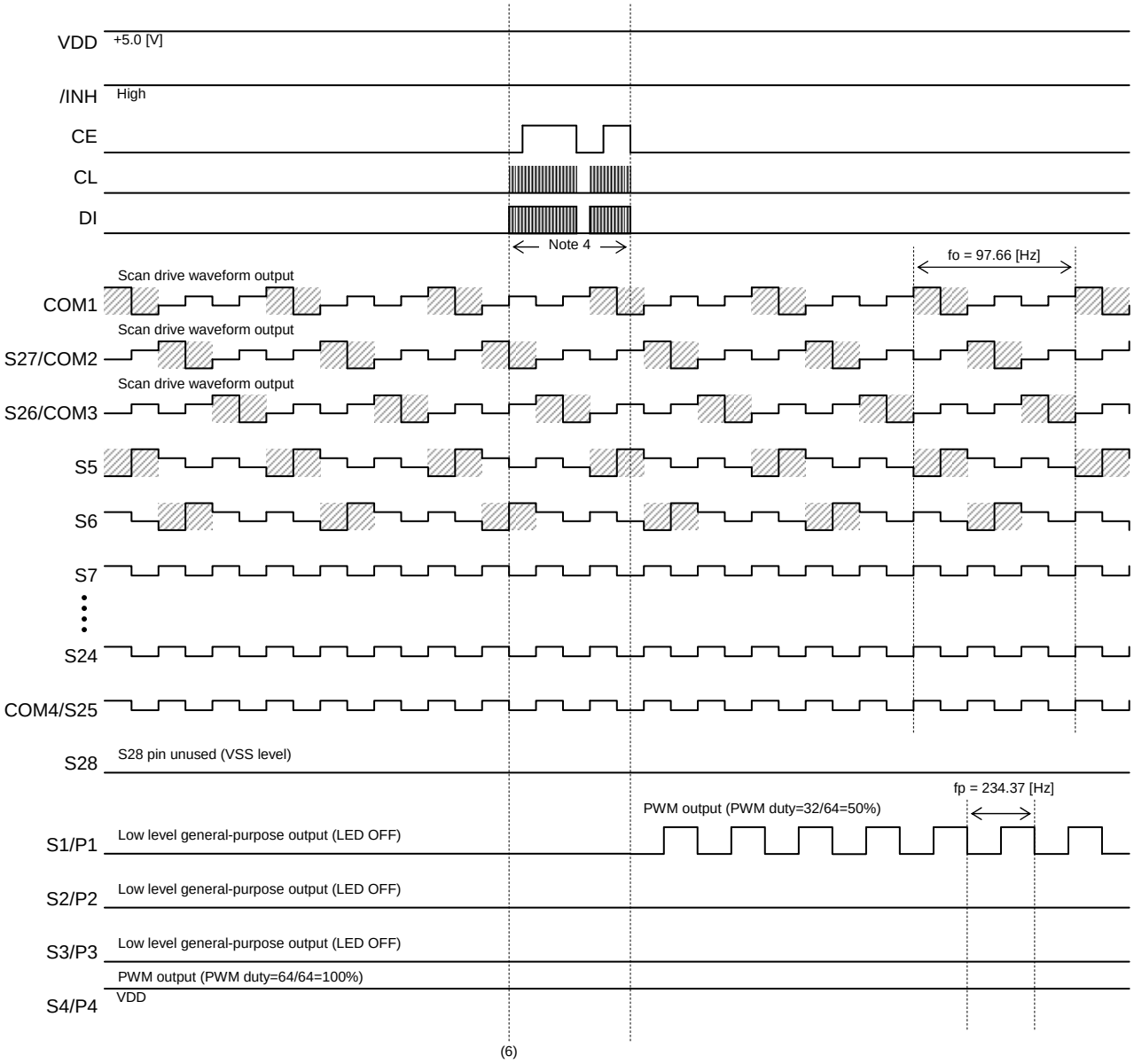
(5) The command of the LED control is transferred.

< Transfer instruction data >

Note 3 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=0 and PS11=0 (S1/P1=Low level general-purpose output),
PS20=0 and PS21=0 (S2/P2=Low level general-purpose output),
PS30=0 and PS31=0 (S3/P3=Low level general-purpose output),
PS40=1 and PS41=1 (S4/P4=PWM output function (ch3) setting),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(4) Timing Chart of the Setting to Turn on the LED of Button Indicator A

Next, the following figure shows the timing waveform of turn on the LED of button indicator A (Brightness is 50%) connecting to S1/P1 output pin.



< Operation sequence >

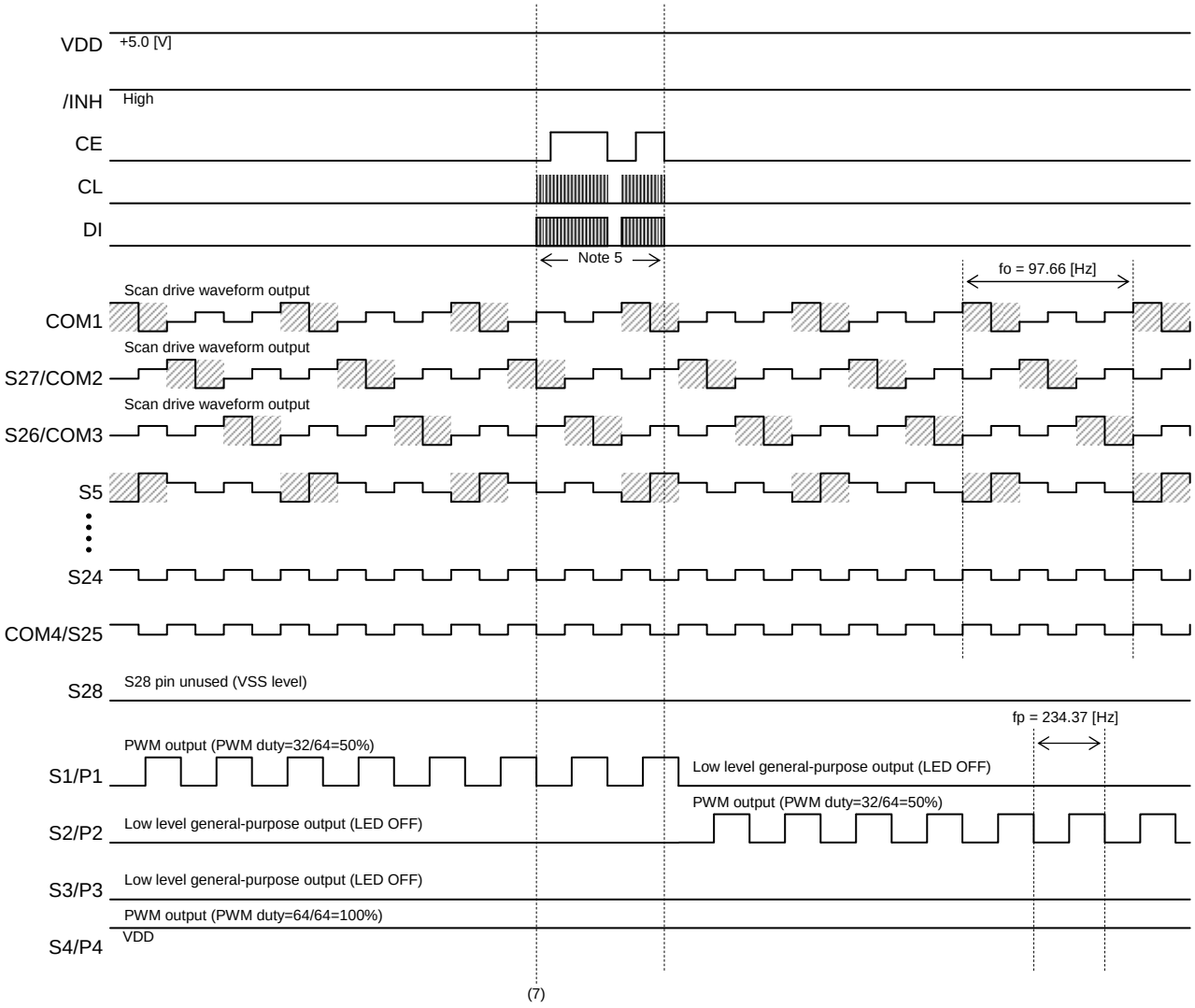
(6) The command of the LED control is transferred.

< Transfer instruction data >

Note 4 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=1 and PS11=1 (S1/P1=PWM output function (ch1) setting),
PS20=0 and PS21=0 (S2/P2=Low level general-purpose output),
PS30=0 and PS31=0 (S3/P3=Low level general-purpose output),
PS40=1 and PS41=1 (S4/P4=PWM output function (ch3) setting),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(5) Timing Chart of the Setting to Turn on the LED of Button Indicator B

Next, the following figure shows the timing waveform of turn off the LED of button indicator A connecting to S1/P1 output pin, and turn on the LED of button indicator B (Brightness is 50%) connecting to S2/P2 output pin.



< Operation sequence >

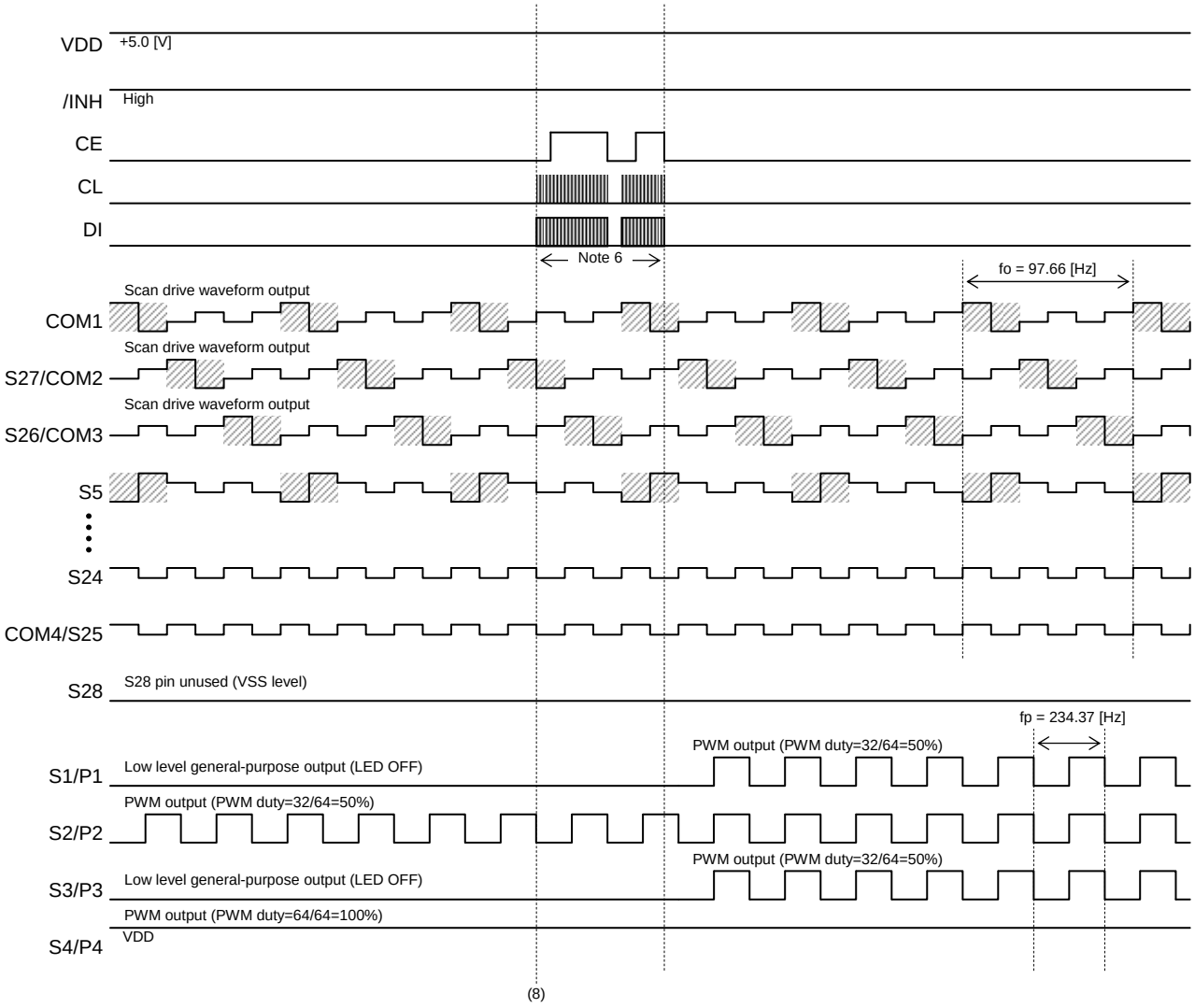
(7) The command of the LED control is transferred.

< Transfer instruction data >

Note 5 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=0 and PS11=0 (S1/P1=Low level general-purpose output),
PS20=1 and PS21=0 (S2/P2=PWM output function (ch1) setting),
PS30=0 and PS31=0 (S3/P3=Low level general-purpose output),
PS40=1 and PS41=1 (S4/P4=PWM output function (ch3) setting),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(6) Timing Chart of the Setting to Turn on the LED of Button Indicator A to C

Next, the following figure shows the timing waveform of turn on the LED of button indicator A to C connecting to S1/P1 to S3/P3 output pin.



< Operation sequence >

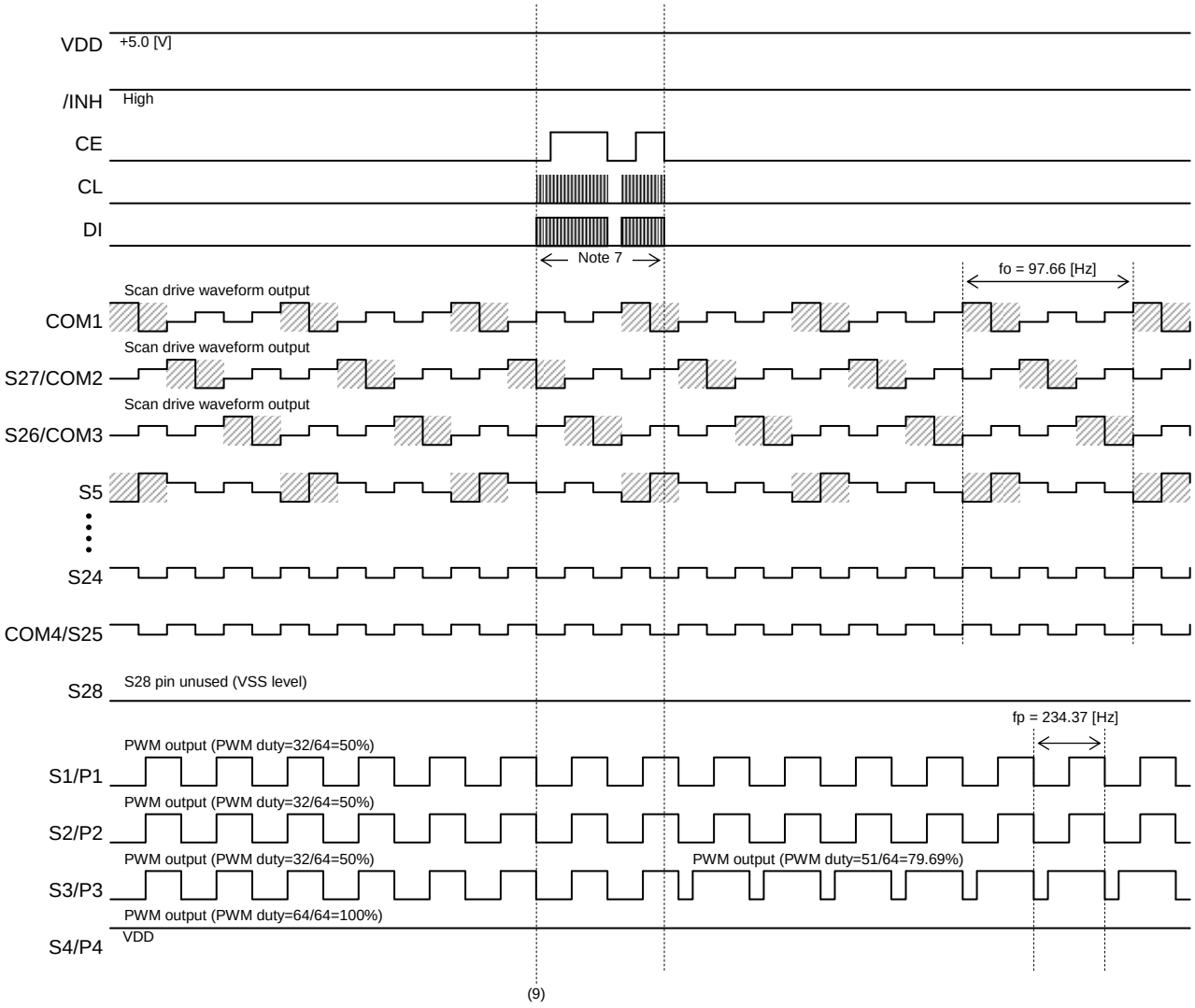
(8) The command of the LED control is transferred.

< Transfer instruction data >

Note 6 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=1,1,1,1,1,0 (Brightness is 50%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=1 and PS11=1 (S1/P1=PWM output function (ch1) setting),
PS20=1 and PS21=0 (S2/P2=PWM output function (ch1) setting),
PS30=0 and PS31=1 (S3/P3=PWM output function (ch2) setting),
PS40=1 and PS41=1 (S4/P4=PWM output function (ch3) setting),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(7) Timing Chart of the Setting to Change the Brightness of the LED

Next, the following figure shows the timing waveform of the LED brightness change (Brightness is 79.69%) of button indicator C connecting to S3/P3 output pin.



< Operation sequence >

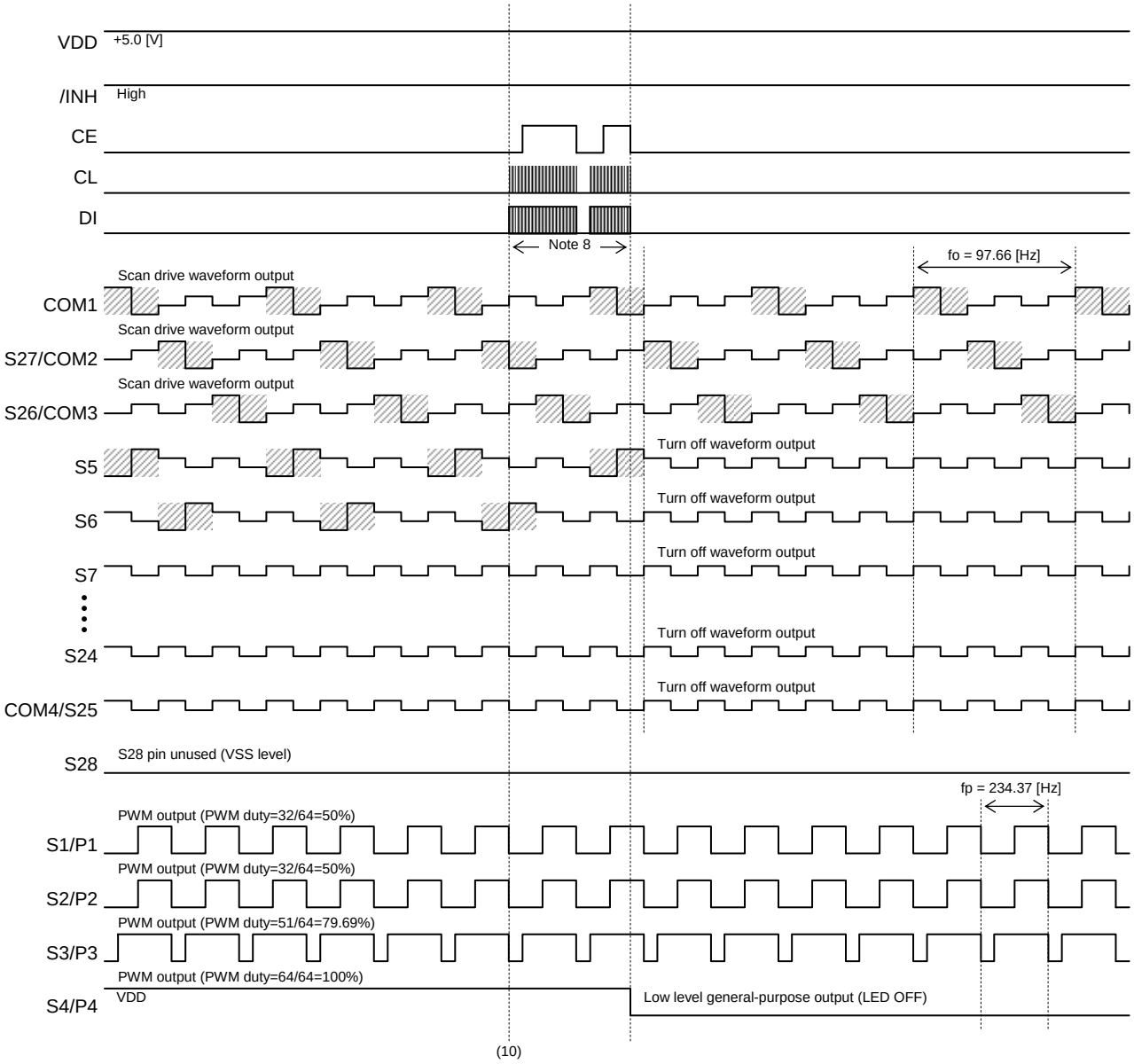
(9) The command of the LED control is transferred.

< Transfer instruction data >

Note 7 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=0,1,0,0,1,1 (Brightness is 79.69%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=1 and PS11=1 (S1/P1=PWM output function (ch1) setting),
PS20=1 and PS21=0 (S2/P2=PWM output function (ch1) setting),
PS30=0 and PS31=1 (S3/P3=PWM output function (ch2) setting),
PS40=1 and PS41=1 (S4/P4=PWM output function (ch3) setting),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=0 (“All segment turn off mode” was cancelled), BU=0 (“Power saving mode” was cancelled).

(8) Timing Chart of the Setting to Turn off the Segments and Turn off the LED of Backlight

Next, the following figure shows the timing waveform of the display OFF (turn off the all segments) and turn off the LED of backlight.



< Operation sequence >

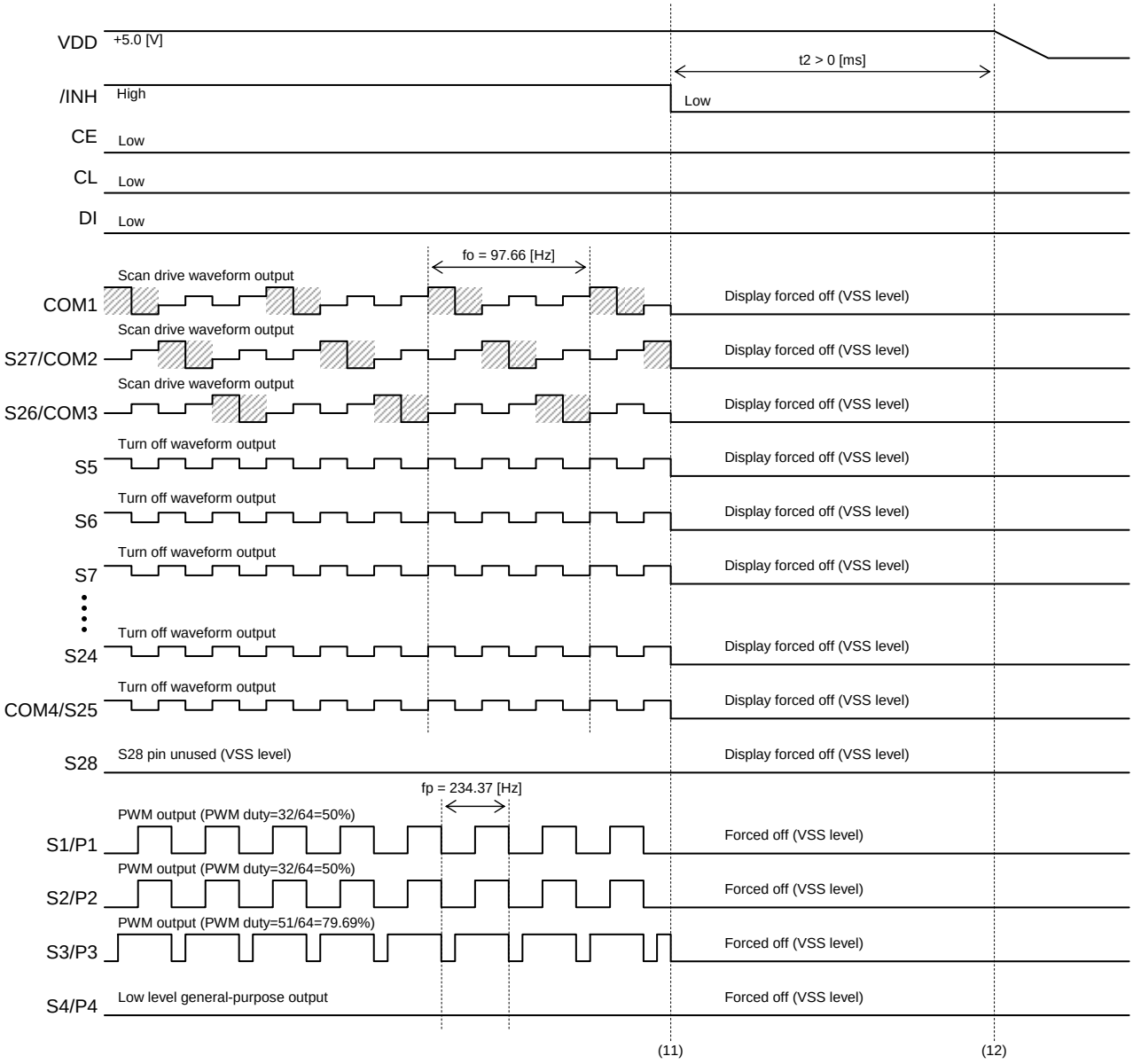
(10) The command of the turn off the segments and turn off the LED of backlight setting is transferred.

< Transfer instruction data >

Note 8 : CCB address = (44)h, D1 to D12=all “0” data,
D13=1, D14=0, D15=0, D16=0, D17=1, D18=0, D19 to D78=all “0” data,
DT0=1 and DT1=0 (1/3-duty),
W10 to W15=1,1,1,1,1,0 (Brightness is 50%),
W20 to W25=0,1,0,0,1,1 (Brightness is 79.69%),
W30 to W35=1,1,1,1,1,1 (Brightness is 100%),
PF0=0, PF1=1, PF2=0 and PF3=0 (fp=234.37 [Hz]),
PS10=1 and PS11=1 (S1/P1=PWM output function (ch1) setting),
PS20=1 and PS21=0 (S2/P2=PWM output function (ch1) setting),
PS30=0 and PS31=1 (S3/P3=PWM output function (ch2) setting),
PS40=0 and PS41=0 (S4/P4=Low level general-purpose output),
P0=1, P1=0 and P2=0 (S1/P1 to S4/P4 are set by general-purpose output port (P1 to P4)),
FC0=0, FC1=1, FC2=0 and FC3=1 (fo=97.66 [Hz]),
DN=0 (S28 pin unused), EXF=0 and OC=0 (Internal oscillator operating mode),
SC=1 (Set the “All segment turn off mode”),
BU=0 (“Power saving mode” was cancelled).

(9) Timing Chart from LCD Display OFF to Power-off State

Finally, the following figure shows the timing waveform to set by power-off state from LCD display OFF.



< Operation sequence >

(11) The display forced off is set by setting the /INH pin to Low (VSS).

(12) Power-off.

Application Circuit

(1) In the Case of the LCD System Configuration Using the LCD Panel of 66 Segments

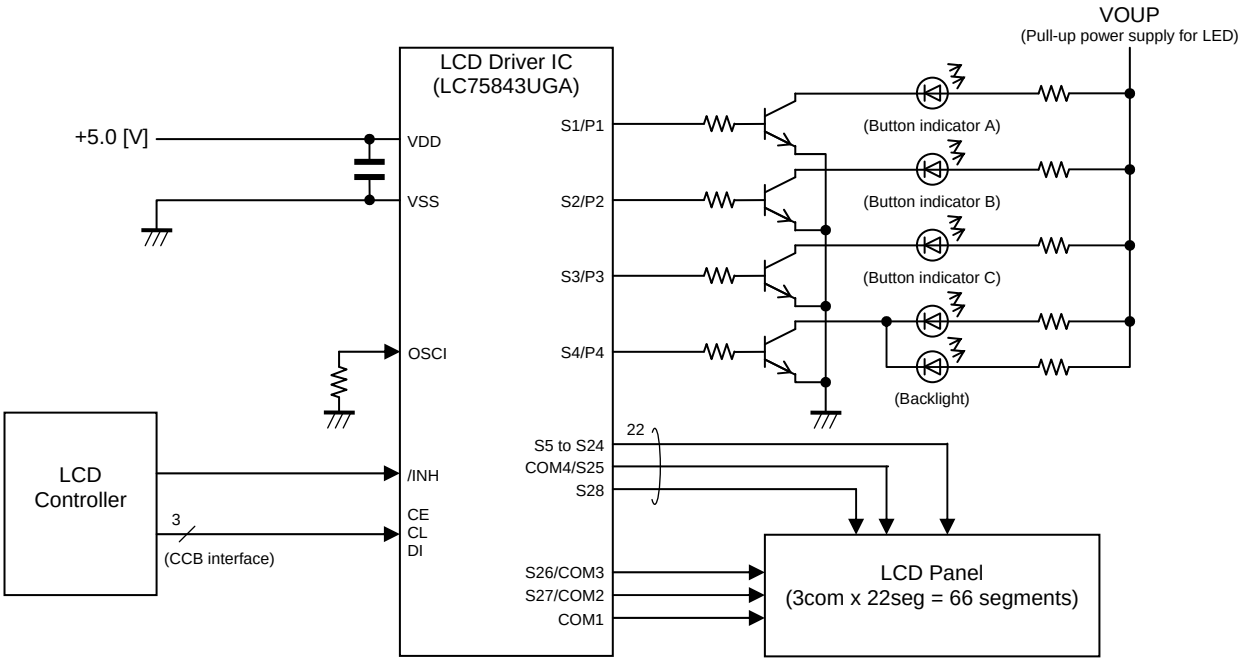


Figure 12. LCD system configuration using the LCD panel of 66 segments

The LC75843UGA is able to drive up to 66 segments the LCD panel of the 1/3-duty when the output pins from S1/P1 to S4/P4 used general-purpose output ports (P1 to P4).

The following explains a setting method example of serial control data in this case.

This system sets DT0=1 and DT1=0 to use an LCD panel of the 1/3-duty drive.

DT0	DT1	LCD drive type	Output pins state			
			COM1	COM2/S27	COM3/S26	COM4/S25
0	0	1/4-duty and 1/3-bias drive type	COM1	COM2	COM3	COM4
1	**0**	**1/3-duty and 1/3-bias drive type**	**COM1**	**COM2**	**COM3**	**S25**
0	1	1/2-duty and 1/2-bias drive type	COM1	COM2	S26	S25
1	1	Static (1/1-duty) drive type	COM1	S27	S26	S25

This system sets DN=1 to use S28 output terminal as the segment output.

DN	S28 output pin state
0	VSS level output
1	**S28 segment output**

This system sets LCD display data from D13 to D78 to use LCD segments from S5 to S25, and S28. In addition, the pins from S1/P1 to S4/P4 use general-purpose output port function. Therefore, sets the general-purpose output ports (P1 to P4) of high level output or low level output by D1 to D12. When sets the “1/3-duty drive mode”, the following table shows the relation between the Display data setting registers (D13 to D78) and the segment outputs and the common outputs.

Output pin	COM1	COM2/S27	COM3/S26
S5	**D13**	**D14**	**D15**
S6	**D16**	**D17**	**D18**
S7	**D19**	**D20**	**D21**
S8	**D22**	**D23**	**D24**
S9	**D25**	**D26**	**D27**
S10	**D28**	**D29**	**D30**
S11	**D31**	**D32**	**D33**
S12	**D34**	**D35**	**D36**
S13	**D37**	**D38**	**D39**
S14	**D40**	**D41**	**D42**
S15	**D43**	**D44**	**D45**
S16	**D46**	**D47**	**D48**
S17	**D49**	**D50**	**D51**
S18	**D52**	**D53**	**D54**
S19	**D55**	**D56**	**D57**
S20	**D58**	**D59**	**D60**
S21	**D61**	**D62**	**D63**
S22	**D64**	**D65**	**D66**
S23	**D67**	**D68**	**D69**
S24	**D70**	**D71**	**D72**
COM4/S25	**D73**	**D74**	**D75**
S28	**D76**	**D77**	**D78**

This system sets output pins from S1/P1 to S4/P4 to a general-purpose output port and controls LED. Therefore, this system sets P0=1, P1=0 and P2=0.

P0	P1	P2	Output pin state			
			S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	**0**	**0**	**P1**	**P2**	**P3**	**P4**
1	0	1	S1	S2	S3	S4
1	1	0	S1	S2	S3	S4
1	1	1	S1	S2	S3	S4

S1 to S4 : Segment output ports
P1 to P4 : General-purpose output ports

The registers of the PS10 and PS11 can set the “General-purpose output function”, “Clock output function”, or “PWM output function” of the general-purpose output port (P1). In addition, the registers of the PS20, PS21, PS30, PS31, PS40 and PS41 can set the “General-purpose output function” or “PWM output function” of the general-purpose output ports (P2, P3 and P4). The general-purpose output function outputs general-purpose output ports (P1 to P4) of high level or low level by “Display data setting registers (D1, D4, D7 and D10)”. The PWM output function can set the pulse width of the PWM output by “PWM duty setting register (W10 to W15, W20 to W25 and W30 to W35)”. The PWM duty setting has up to 3ch and can perform brightness adjustment of the LED individually for each channel.

The setting method about the registers except the above is the same as “Explanation of the LCD drive control”, “Explanation of the LED Control by General-purpose Output Ports” and “Explanation of the Instruction Data”.

(2) In the Case of the LCD System Configuration Using the LCD Panel of 69 Segments

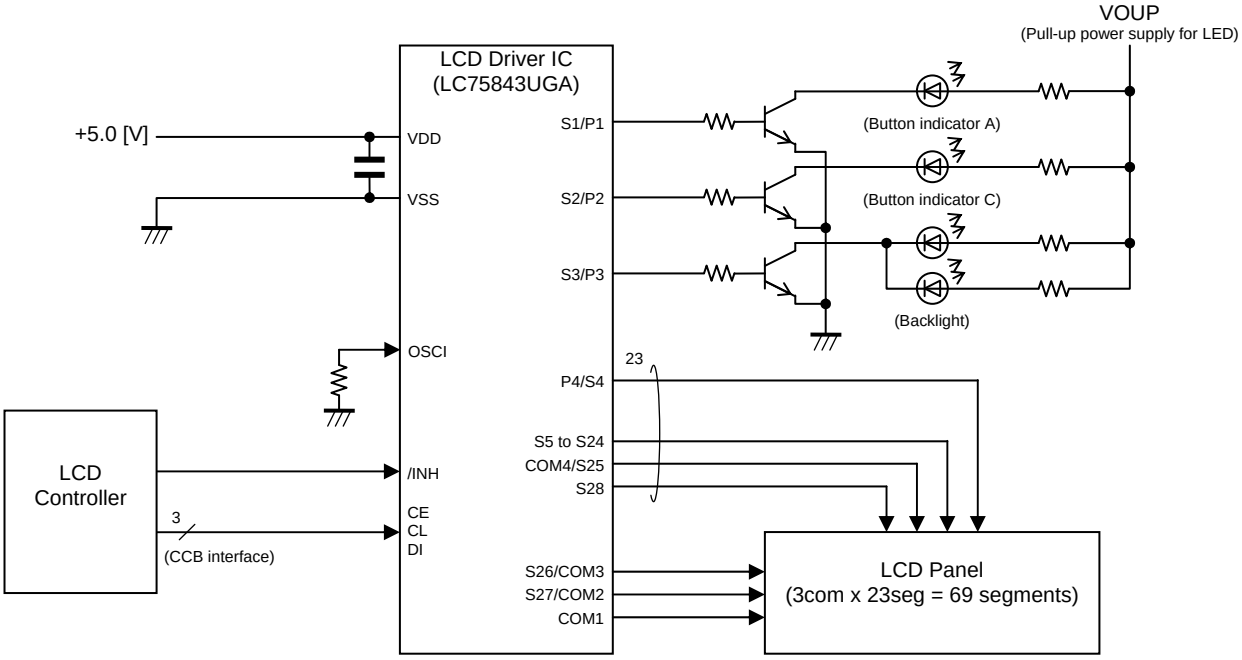


Figure 13. LCD system configuration using the LCD panel of 69 segments

The output pins from S1/P1 to S4/P4 of the LC75843UGA can set the “Segment output port” or “General-purpose output port”. This IC is able to drive up to 69 segments the LCD panel of the 1/3-duty when the output pins from S1/P1 to S3/P3 used general-purpose output ports (P1 to P3) and the S4/P4 output pin used segment output port (S4). The following explains a setting method example of serial control data in this case.

This system sets DT0=1 and DT1=0 to use an LCD panel of the 1/3-duty drive.

DT0	DT1	LCD drive type	Output pins state			
			COM1	COM2/S27	COM3/S26	COM4/S25
0	0	1/4-duty and 1/3-bias drive type	COM1	COM2	COM3	COM4
1	**0**	**1/3-duty and 1/3-bias drive type**	**COM1**	**COM2**	**COM3**	**S25**
0	1	1/2-duty and 1/2-bias drive type	COM1	COM2	S26	S25
1	1	Static (1/1-duty) drive type	COM1	S27	S26	S25

This system sets DN=1 to use S28 output terminal as the segment output.

DN	S28 output pin state
0	VSS level output
1	**S28 segment output**

This system sets LCD display data from D10 to D78 to use LCD segments from S4 to S25, and S28. In addition, the pins from S1/P1 to S3/P3 use general-purpose output port function. Therefore, sets the general-purpose output ports (P1 to P3) of high level output or low level output by D1 to D9. When sets the “1/3-duty drive mode”, the following table shows the relation between the Display data setting registers (D10 to D78) and the segment outputs and the common outputs.

Output pin	COM1	COM2/S27	COM3/S26
S4/P4	**D10**	**D11**	**D12**
S5	**D13**	**D14**	**D15**
S6	**D16**	**D17**	**D18**
S7	**D19**	**D20**	**D21**
S8	**D22**	**D23**	**D24**
S9	**D25**	**D26**	**D27**
S10	**D28**	**D29**	**D30**
S11	**D31**	**D32**	**D33**
S12	**D34**	**D35**	**D36**
S13	**D37**	**D38**	**D39**
S14	**D40**	**D41**	**D42**
S15	**D43**	**D44**	**D45**
S16	**D46**	**D47**	**D48**
S17	**D49**	**D50**	**D51**
S18	**D52**	**D53**	**D54**
S19	**D55**	**D56**	**D57**
S20	**D58**	**D59**	**D60**
S21	**D61**	**D62**	**D63**
S22	**D64**	**D65**	**D66**
S23	**D67**	**D68**	**D69**
S24	**D70**	**D71**	**D72**
COM4/S25	**D73**	**D74**	**D75**
S28	**D76**	**D77**	**D78**

When the S1/P1 to S3/P3 output pins used general-purpose output ports (P1 to P3) and when the S4/P4 output pin used segment output port (S4), this system sets P0=0, P1=1 and P2=1.

P0	P1	P2	Output pin state			
			S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	**1**	**1**	**P1**	**P2**	**P3**	**S4**
1	0	0	P1	P2	P3	P4
1	0	1	S1	S2	S3	S4
1	1	0	S1	S2	S3	S4
1	1	1	S1	S2	S3	S4

S1 to S4 : Segment output ports
P1 to P4 : General-purpose output ports

The registers of the PS10 and PS11 can set the “General-purpose output function”, “Clock output function”, or “PWM output function” of the general-purpose output port (P1). In addition, the registers of the PS20, PS21, PS30 and PS31 can set the “General-purpose output function” or “PWM output function” of the general-purpose output ports (P2 and P3). The general-purpose output function outputs general-purpose output ports (P1 to P3) of high level or low level by “Display data setting registers (D1, D4 and D7)”.

This system does not use the registers of the PS40 and PS41. Therefore, those set all “0”.

The setting method about the registers except the above is the same as “Explanation of the LCD drive control”, “Explanation of the LED Control by General-purpose Output Ports” and “Explanation of the Instruction Data”.

(3) In the Case of the LCD System Configuration Using the LCD Panel of 78 Segments

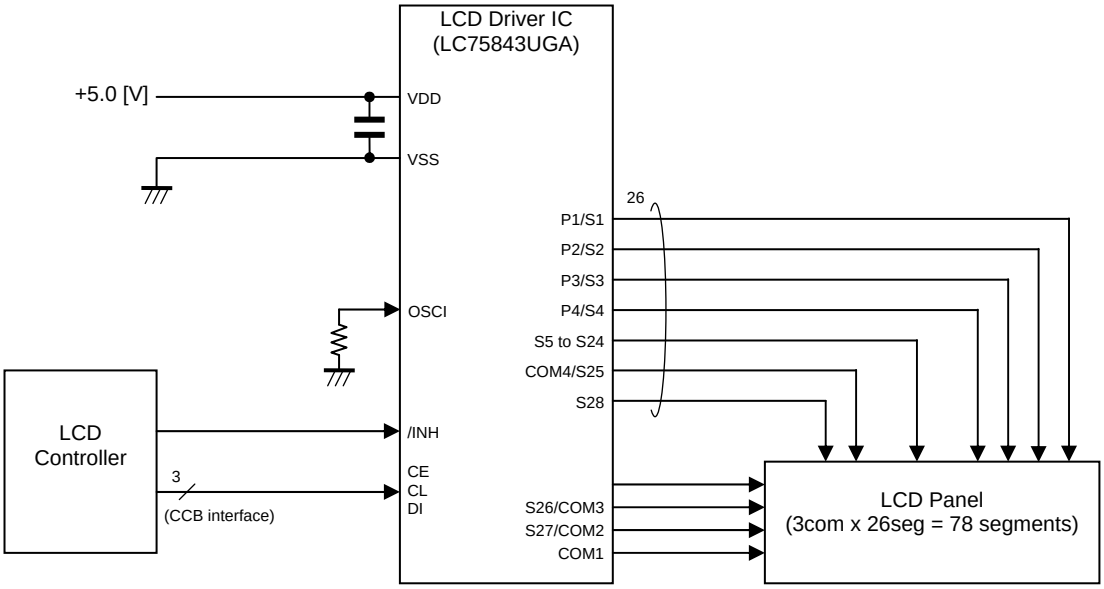


Figure 14. LCD system configuration using the LCD panel of 78 segments

The LC75843UGA is able to drive up to 78 segments the LCD panel of the 1/3-duty when the output pins from S1/P1 to S4/P4 used segment output ports (S1 to S4).
The following explains a setting method example of serial control data in this case.

This system sets DT0=1 and DT1=0 to use an LCD panel of the 1/3-duty drive.

DT0	DT1	LCD drive type	Output pins state			
			COM1	COM2/S27	COM3/S26	COM4/S25
0	0	1/4-duty and 1/3-bias drive type	COM1	COM2	COM3	COM4
1	**0**	**1/3-duty and 1/3-bias drive type**	**COM1**	**COM2**	**COM3**	**S25**
0	1	1/2-duty and 1/2-bias drive type	COM1	COM2	S26	S25
1	1	Static (1/1-duty) drive type	COM1	S27	S26	S25

This system sets DN=1 to use S28 output terminal as the segment output.

DN	S28 output pin state
0	VSS level output
1	**S28 segment output**

This system sets LCD display data from D1 to D78 to use LCD segments from S1 to S25, and S28. When sets the “1/3-duty drive mode”, the following table shows the relation between the Display data setting registers (D1 to D78) and the segment outputs and the common outputs.

Output pin	COM1	COM2/S27	COM3/S26
S1/P1	**D1**	**D2**	**D3**
S2/P2	**D4**	**D5**	**D6**
S3/P3	**D7**	**D8**	**D9**
S4/P4	**D10**	**D11**	**D12**
S5	**D13**	**D14**	**D15**
S6	**D16**	**D17**	**D18**
S7	**D19**	**D20**	**D21**
S8	**D22**	**D23**	**D24**
S9	**D25**	**D26**	**D27**
S10	**D28**	**D29**	**D30**
S11	**D31**	**D32**	**D33**
S12	**D34**	**D35**	**D36**
S13	**D37**	**D38**	**D39**
S14	**D40**	**D41**	**D42**
S15	**D43**	**D44**	**D45**
S16	**D46**	**D47**	**D48**
S17	**D49**	**D50**	**D51**
S18	**D52**	**D53**	**D54**
S19	**D55**	**D56**	**D57**
S20	**D58**	**D59**	**D60**
S21	**D61**	**D62**	**D63**
S22	**D64**	**D65**	**D66**
S23	**D67**	**D68**	**D69**
S24	**D70**	**D71**	**D72**
COM4/S25	**D73**	**D74**	**D75**
S28	**D76**	**D77**	**D78**

This system sets output pins from S1/P1 to S4/P4 to a segment output port and drives LCD segment. Therefore this system sets P0=0, P1=0 and P2=0.

P0	P1	P2	Output pin state			
			S1/P1	S2/P2	S3/P3	S4/P4
0	**0**	**0**	**S1**	**S2**	**S3**	**S4**
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4
1	0	1	S1	S2	S3	S4
1	1	0	S1	S2	S3	S4
1	1	1	S1	S2	S3	S4

S1 to S4 : Segment output ports
P1 to P4 : General-purpose output ports

This system does not use the registers of the PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, W10 to W15, W20 to W25, W30 to W35, and PF0 to PF3. Therefore, those set all “0”.

The setting method about the registers except the above is the same as “Explanation of the LCD drive control”, “Explanation of the LED Control by General-purpose Output Ports” and “Explanation of the Instruction Data”.

(4) In the Case of the LCD System Configuration to Input an External Clock (300kHz)

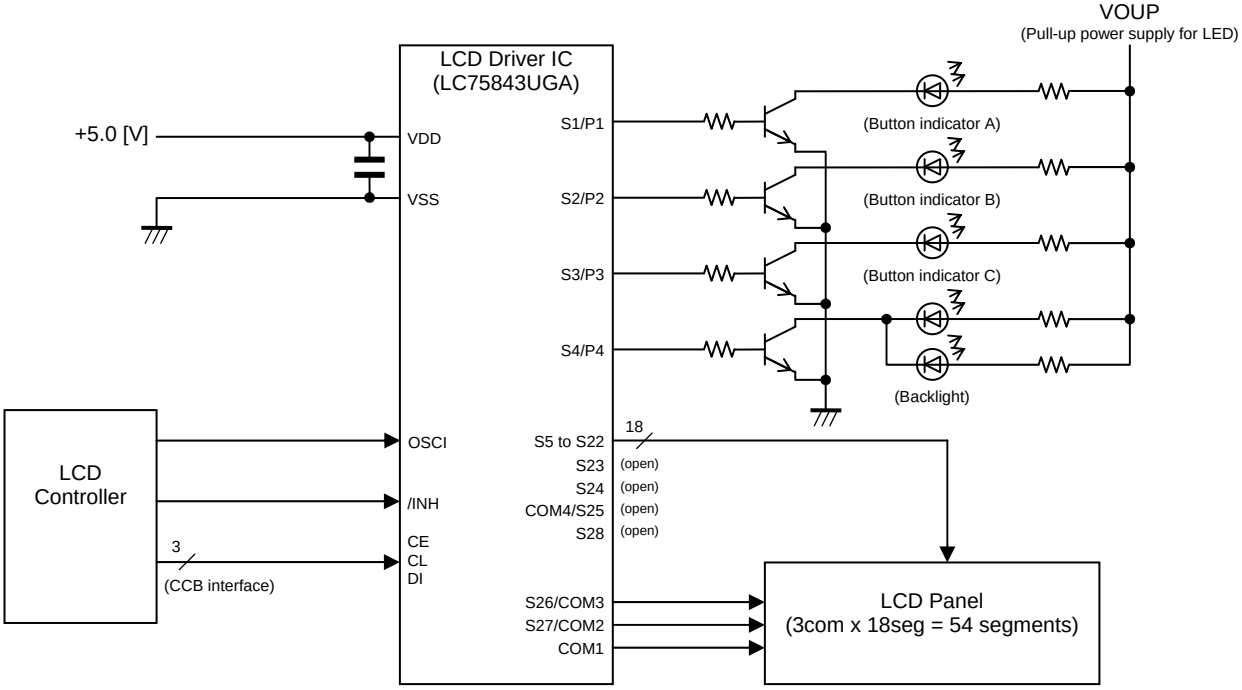


Figure 15. LCD system configuration to input an external clock (300kHz)

The LC75843UGA is able to set the “Internal oscillator operating mode” or “External clock input operating mode”. Furthermore, this IC can set the division ratio a clock to input from OSCI pin becomes 300 [kHz](Typ.) or 38 [kHz](Typ.). However, when set the “External clock 38kHz input mode (OC=1 and EXF=1)”, please be careful because PWM output function is invalidity.

The reason why a customer selects the LCD system configuration using the “External clock input operating mode” is because the characteristic of the internal oscillator clock frequency (fosc) is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore the customer may worry about the flicker of the liquid crystal display occurring by interference with other frequency. Furthermore, there may be a customer hoping to lower clock frequency more because of the low power consumption and EMI (Electro Magnetic Interference) measures, etc.

First of all, the following table shows the pin explanation of the external clock input pin (OSCI) and the specifications of the allowable operating ranges.

Pin name	Pin function
OSCI	External clock input pin. When “Internal oscillator operating mode (OC=0)”, make sure to connect OSCI to GND. When “External clock input mode (OC=1)”, OSCI is used to input the external clock.

Allowable operating ranges at Ta= -40°C to +105°C, VSS=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	VDD	4.5		6.3	V
Input High Level Voltage	V_{IH2}	OSCI	0.4 V_{DD}		6.3	V
Input Low Level Voltage	V_{IL2}	OSCI	0		0.2 V_{DD}	V
External Clock input Frequency	f_{ck}	OSCI, External clock input operating mode	10	300	600	kHz
External Clock Duty Ratio	D_{ck}	OSCI, External clock input operating mode	30	50	70	%

These specifications show an example, and, we have a case to change these specifications without a notice for improvement. Therefore, it is not guaranteed for design as the mass production equipment. When designing equipment, refer to the “Delivery specification for the LC75843UGA”.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

The following explains a setting method example of serial control data in this case.

This system sets OC=1 and EXF=0 to use the “External clock 300kHz input mode”

OC	EXF	Fundamental clock operating mode	OSCI input pin state
0	0/1	Internal oscillator operating mode	Connect to GND
1	**0**	**External clock 300kHz input mode**	**Inputs a clock of 300 [kHz](Typ.)**
1	1	External clock 38kHz input mode	Inputs a clock of 38 [kHz](Typ.)

The registers from FC0 to FC3 can set the frame frequency (fo) of the common and segment output waveform. When sets OC=1 and EXF=0, the following table shows the frame frequency of the LCD drive waveform.

FC0	FC1	FC2	FC3	External clock 300kHz input operating mode (OC=1, EXF=0)	
				LCD drive waveform frame ratio	LCD drive waveform frame frequency fo [Hz] (External clock input frequency is fck=300 [kHz](typ.))
0	0	0	0	fck / 6144	48.83
0	0	0	1	fck / 5376	55.80
0	0	1	0	fck / 4608	65.10
0	0	1	1	fck / 3840	78.12
0	1	0	0	fck / 3456	86.80
0	1	0	1	fck / 3072	97.66
0	1	1	0	fck / 2688	111.61
0	1	1	1	fck / 2304	130.21
1	0	0	0	fck / 2112	142.04
1	0	0	1	fck / 1920	156.25
1	0	1	0	fck / 1728	173.61
1	0	1	1	fck / 1536	195.31
1	1	0	0	fck / 1344	223.21
1	1	0	1	fck / 1152	260.42
1	1	1	0	fck / 960	312.50
1	1	1	1	fck / 768	390.62

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

The registers from PF0 to PF3 can set the PWM output frame frequency (fp) of the general-purpose output port. When sets OC=1 and EXF=0, the following table shows the frame frequency of the PWM output waveform.

PF0	PF1	PF2	PF3	External clock 300kHz input operating mode (OC=1, EXF=0)	
				PWM output waveform frame ratio	PWM output waveform frame frequency fp [Hz] (External clock input frequency is fck=300 [kHz](typ.))
0	0	0	0	fck / 1536	195.31
1	0	0	0	fck / 1408	213.07
0	1	0	0	fck / 1280	234.37
1	1	0	0	fck / 1152	260.42
0	0	1	0	fck / 1024	292.97
1	0	1	0	fck / 896	334.82
0	1	1	0	fck / 768	390.62
1	1	1	0	fck / 640	468.75
0	0	0	1	fck / 512	585.94
1	0	0	1	fck / 384	781.25
0	1	0	1	fck / 256	1171.87
1	1	0	1	fck / 896	334.82
0	0	1	1	fck / 896	334.82
1	0	1	1	fck / 896	334.82
0	1	1	1	fck / 896	334.82
1	1	1	1	fck / 896	334.82

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

The setting method about the registers except the above is the same as “Explanation of the LCD drive control”, “Explanation of the LED Control by General-purpose Output Ports” and “Explanation of the Instruction Data”.

(5) In the Case of the LCD System Configuration to Input an External Clock (38kHz)

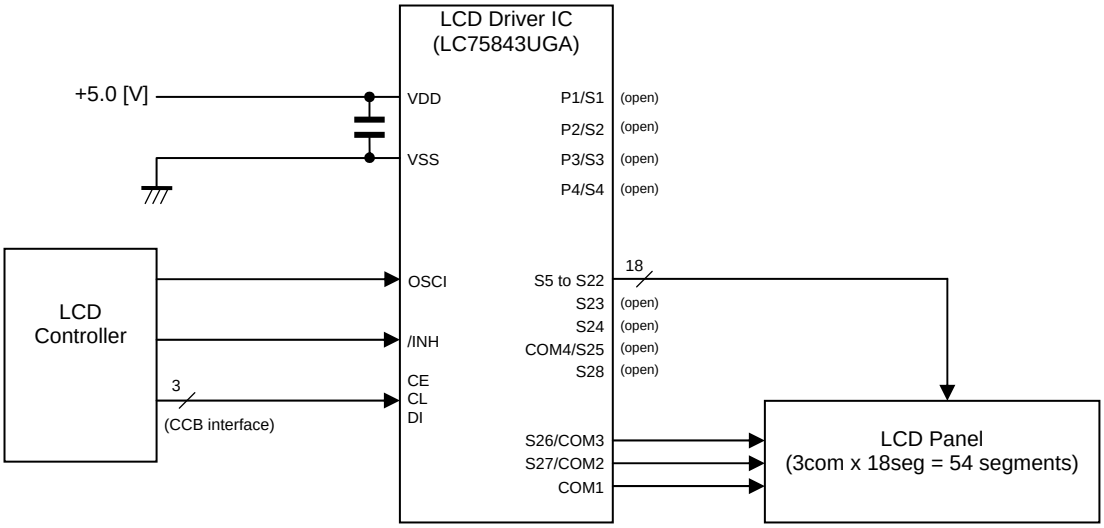


Figure 16. LCD system configuration to input an external clock (38kHz)

The LC75843UGA is able to set the “Internal oscillator operating mode” or “External clock input operating mode”. Furthermore, this IC can set the division ratio a clock to input from OSCI pin becomes 300 [kHz](Typ.) or 38 [kHz](Typ.). However, when set the “External clock 38kHz input mode (OC=1 and EXF=1)”, please be careful because PWM output function is invalidity.

The following explains a setting method example of serial control data in this case.

This system sets OC=1 and EXF=1 to use the “External clock 38kHz input mode”

OC	EXF	Fundamental clock operating mode	OSCI input pin state
0	0/1	Internal oscillator operating mode	Connect to GND
1	0	External clock 300kHz input mode	Inputs a clock of 300 [kHz](Typ.)
1	**1**	**External clock 38kHz input mode**	**Inputs a clock of 38 [kHz](Typ.)**

The registers from FC0 to FC3 can set the frame frequency (fo) of the common and segment output waveform. When sets OC=1 and EXF=1, the following table shows the frame frequency of the LCD drive waveform.

FC0	FC1	FC2	FC3	External clock 38kHz input operating mode (OC=1, EXF=1)	
				LCD drive waveform frame ratio	LCD drive waveform frame frequency fo [Hz] (External clock input frequency is fck=38 [kHz](typ.))
0	0	0	0	fck / 768	49.48
0	0	0	1	fck / 672	56.55
0	0	1	0	fck / 576	65.97
0	0	1	1	fck / 480	79.16
0	1	0	0	fck / 432	87.96
0	1	0	1	fck / 384	98.96
0	1	1	0	fck / 336	113.09
0	1	1	1	fck / 288	131.94
1	0	0	0	fck / 264	143.94
1	0	0	1	fck / 240	158.33
1	0	1	0	fck / 216	175.92
1	0	1	1	fck / 192	197.92
1	1	0	0	fck / 168	226.19
1	1	0	1	fck / 144	263.89
1	1	1	0	fck / 120	316.67
1	1	1	1	fck / 96	395.83

The explanation mentioned above is used only to explain internal operation and how to IC, and the characteristic of the products is uneven by a production variation and the terms of use of the IC (Power supply voltage, temperature, etc.). Therefore, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

This system sets output pins from S1/P1 to S4/P4 to a segment output port and drives LCD segment. Therefore this system sets P0=0, P1=0 and P2=0.

P0	P1	P2	Output pin state			
			S1/P1	S2/P2	S3/P3	S4/P4
0	**0**	**0**	**S1**	**S2**	**S3**	**S4**
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4
1	0	1	S1	S2	S3	S4
1	1	0	S1	S2	S3	S4
1	1	1	S1	S2	S3	S4

S1 to S4 : Segment output ports
P1 to P4 : General-purpose output ports

This system does not use the registers of the PS10, PS11, PS20, PS21, PS30, PS31, PS40, PS41, W10 to W15, W20 to W25, W30 to W35, and PF0 to PF3. Therefore, those set all “0”.

The setting method about the registers except the above is the same as “Explanation of the LCD drive control”, “Explanation of the LED Control by General-purpose Output Ports” and “Explanation of the Instruction Data”.

When LED control is necessary for the LCD system configuration example of the “External clock 38kHz input mode”, the output pins from S1/P1 to S4/P4 are set the general-purpose output ports (P1 to P4), and if it is only setting of ON (Brightness is 100%) or OFF of the LED, it can be set. Then, this system controls LED by general-purpose output port of the output pins from S1/P1 to S4/P4, therefore, this system sets P0=1, P1=0 and P2=0. In addition, the general-purpose output port (P4) uses the general-purpose output function, therefore, this system sets PS40=0 and PS41=0. Finally, the general-purpose output port (P4) outputs high level (LED turns on with 100% of brightness) or low level (turn off the LED) by the “Display data setting register (D10)”.

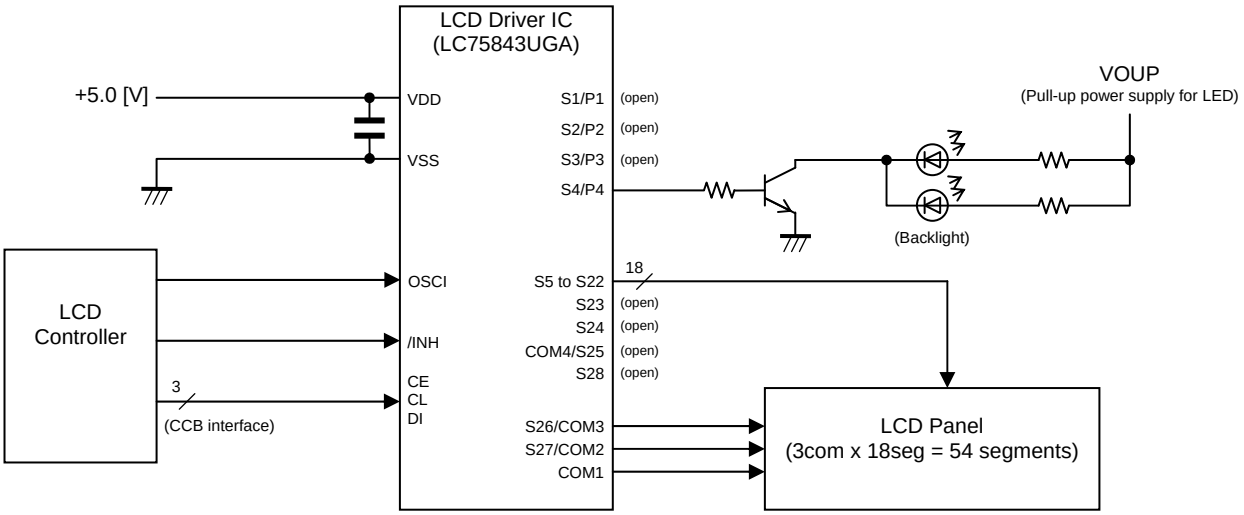


Figure 17. LED control by the LCD system configuration to input an external clock (38kHz)

(6) In the Case of the LCD System Configuration Using two LCD Panels.

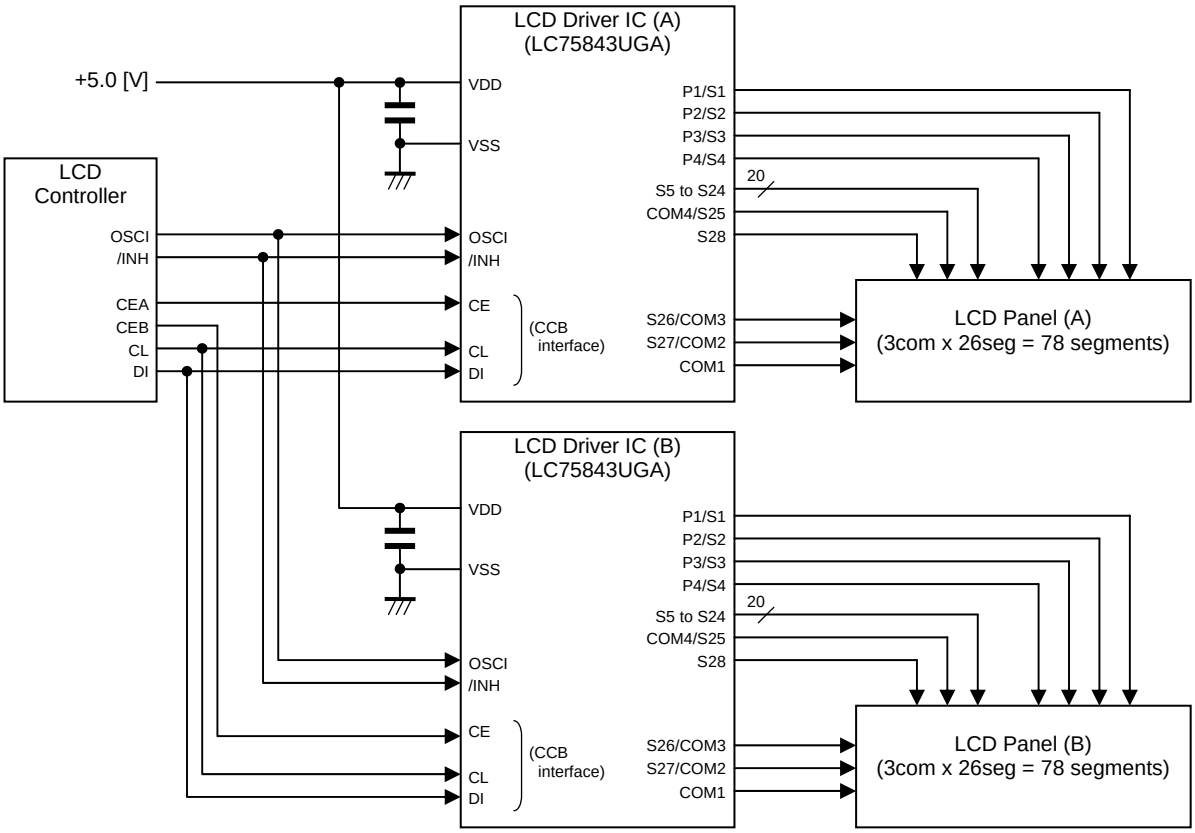


Figure 18. LCD system configuration using two LCD panels

In the case of the system configuration using two LCD panels, the CL and DI signal of the CCB interface are input from an LCD controller into both LC75843UGA and are controlled at the same time, and the CE signal of the CCB interface is input from an LCD controller into LC75843UGA separately and is controlled separately.

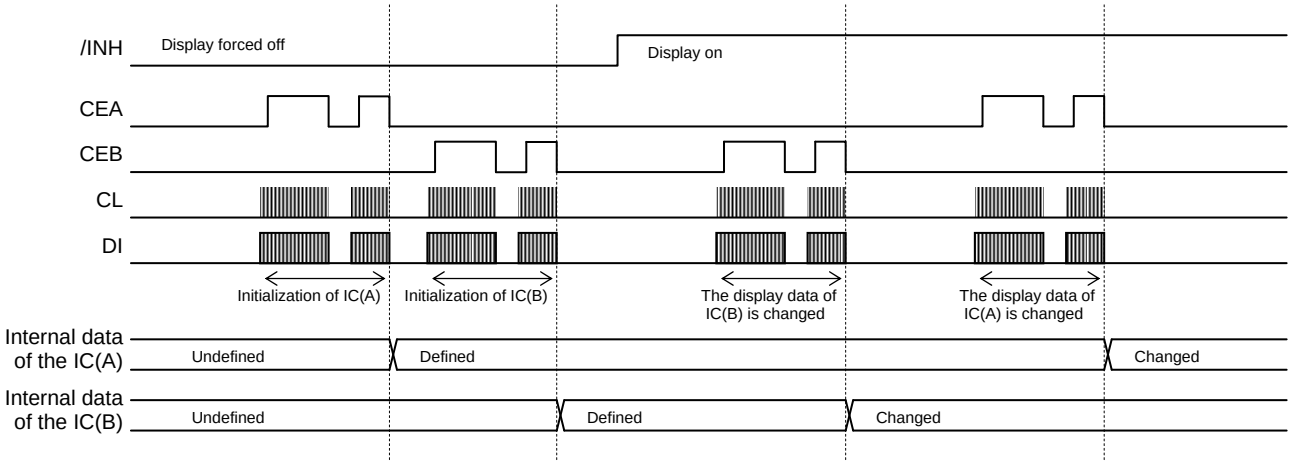


Figure 19. Control example of the LCD system configuration using two LCD panels

When serial control data is transferred for LCD driver IC(A), the “Chip enable A (CEA)” signal is set to control signal, and the “chip enable B (CEB)” signal is held to low level. When serial control data is transferred for LCD driver IC(B), the “Chip enable A (CEA)” signal is held to low level, and the “Chip enable B (CEB)” signal is set to control signal.

Even if a control signal is input into CL and DI, the internal data of the LCD driver IC are not changed if CE signal is heldd to low level.