LV5636VH

DC/DC Boost converter for BS/CS antennas
Application Note Ver.2.0

ON Semiconductor®
http://onsemi.com

1. Overview

LV5636VH integrates 1ch DC/DC boost converter and 1ch LDO. It is suitable as the power supply for BS/CS antennas of LCD/PDP TV and BD recorders that require automatic recovery without IC destruction and malfunction when the output is short-circuited.

2. Function

DC/DC boost converter

- Soft-start time: 2.6ms
- Frequency 1MHz operation
- Pulse by pulse over-current limiter
- Short circuit protector (constant timer: 1.6ms)

LDO

- Over-current limiter (Fold back)

ALL

- Under-voltage lockout
- Thermal shut-down protector
- Power good
- Power good delay function
- Built-in output setting resistor
- Output voltage switching function (BS/CS)

3. Block diagram and Application circuit

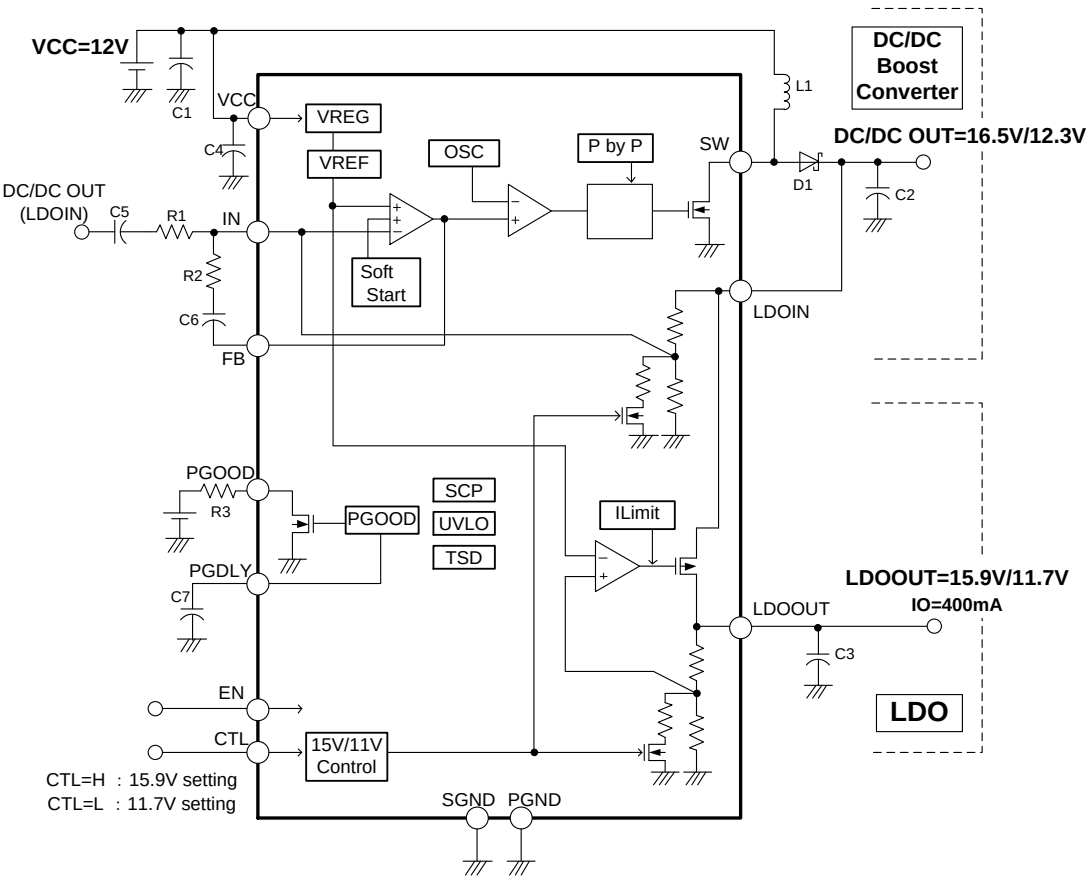


Figure 1: Block diagram and Application circuit

4. Evaluation Board

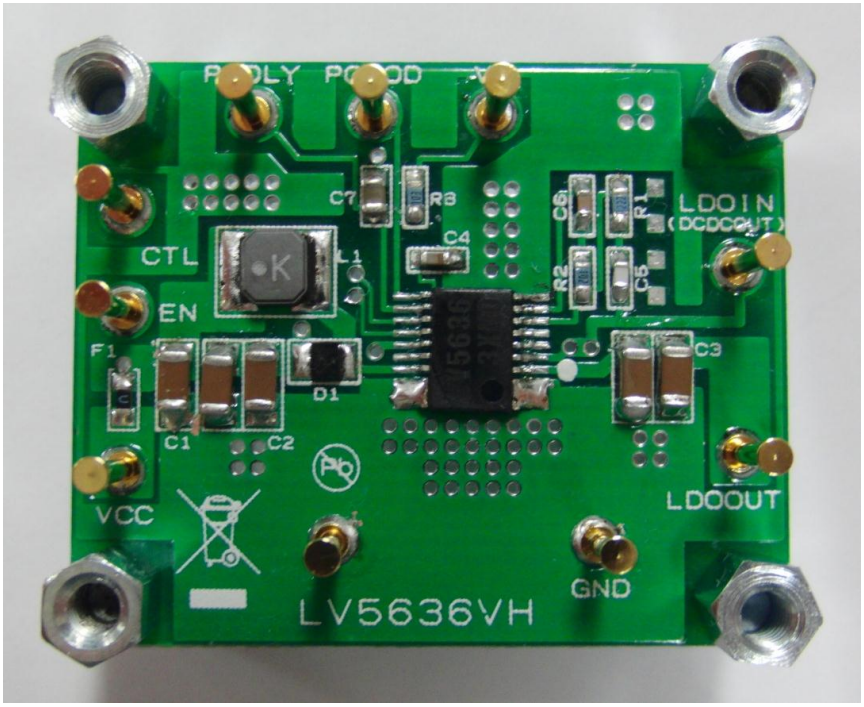


Figure 2: Evaluation Board

4.1 Performance summary

VCC input	12V
LDOOUT output	15.9V / 11.7V
Oscillation Frequency	1MHz
EN input	High(2V): IC ON Low(0V): IC OFF
CTL input	High(2V): LDOOUT=15.9V Low(0V): LDOOUT=11.7V
V1 input	2V
Power Good Delay Time	1.23s (C7=4.7uF)

4.2 Schematic

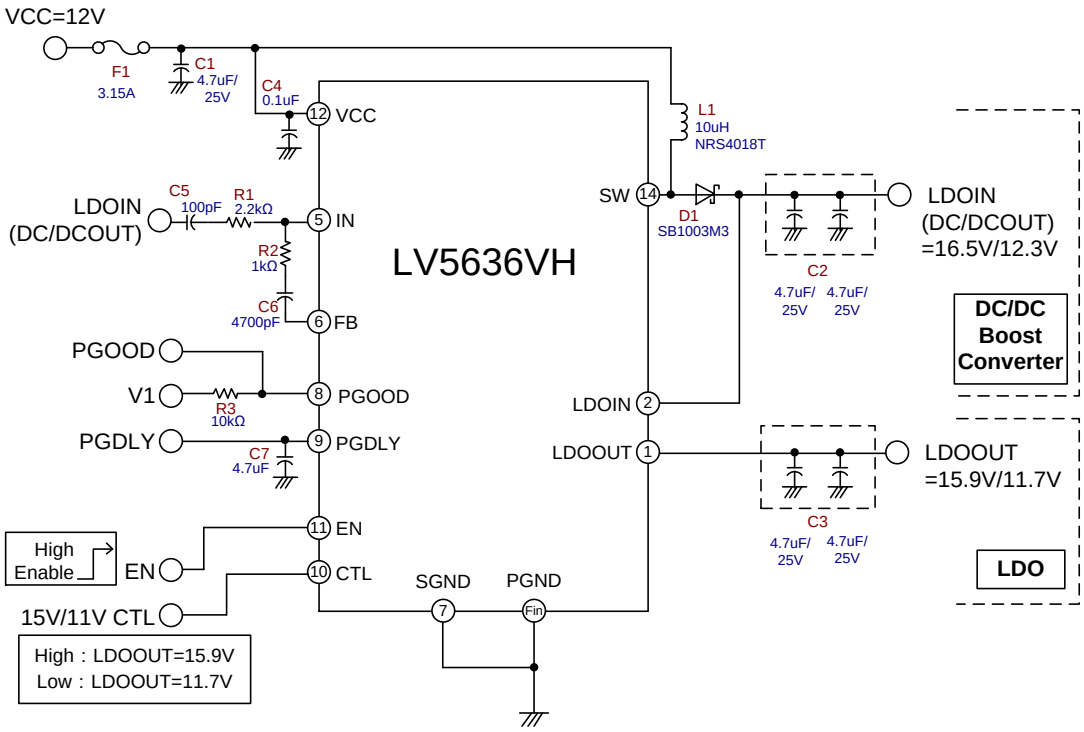


Figure 3: Schematic of Evaluation Board

4.3 Bill of Materials

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
C1	1	Capacitor,Ceramic,B	4.7uF/25V	10%	1206	MURATA	GRM31CB31E475K
C2	2	Capacitor,Ceramic,B	4.7uF/25V	10%	1206	MURATA	GRM31CB31E475K
C3	2	Capacitor,Ceramic,B	4.7uF/25V	10%	1206	MURATA	GRM31CB31E475K
C4	1	Capacitor,Ceramic,B	0.1uF/50V	10%	0603	MURATA	GRM188B31H104K
C5	1	Capacitor,Ceramic,CH	100pF/50V	5%	0603	MURATA	GRM1882C1H101J
C6	1	Capacitor,Ceramic,CH	4700pF/50V	10%	0603	MURATA	GRM188B11H472K
C7	1	Capacitor,Ceramic,B	4.7uF/10V	10%	0805	MURATA	GRM219B31A475K
D1	1	Diode,Schottky	30V/1A	-	MCPH3	ON Semiconductor	SB1003M3
F1	1	Fuse Resistor	3.15A	-	0603	KOA	TF16AT3.15TBK
L1	1	Power Inductor	10uH	20%	4.0x4.0	TAIYO YUDEN	NRS4018T 100MDGJ
R1	1	Chip Resistor	2.2kohm	1%	0603	KOA	RK73H1JTTD223
R2	1	Chip Resistor	1kohm	1%	0603	KOA	RK73H1JTTD103
R3	1	Chip Resistor	10kohm	1%	0603	KOA	RK73H1JTTD104
U1	1	DCDC and LDO Driver	-	-	HSSOP-14	ON Semiconductor	LV5636VH

4.4 Test Procedure

Suggested equipment:

- Current limited DC Power Supply (e.g. ADVANTEST R6243 DC Voltage Current Source/Monitor) ···· 2pcs
- Digital Multimeter (e.g. ADVANTEST R6452 Digital Multimeter) ····· 2pcs
- Multifunction Generator (e.g. NF WF1974) ····· 2pcs
- Electronic Load (e.g. FUJITSU ACCESS LIMITED Electric Load EUL-150αXL) ····· 1pc
- Oscilloscope (e.g. LeCroy WaveRunner) ····· 1pc

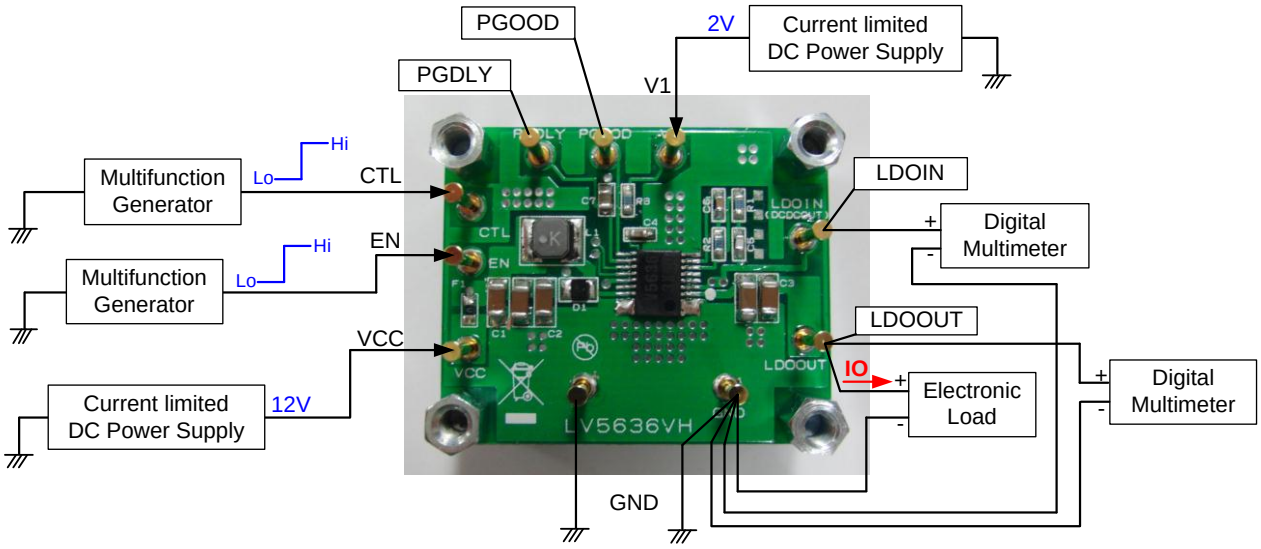


Figure 4: Test setup

Procedure:

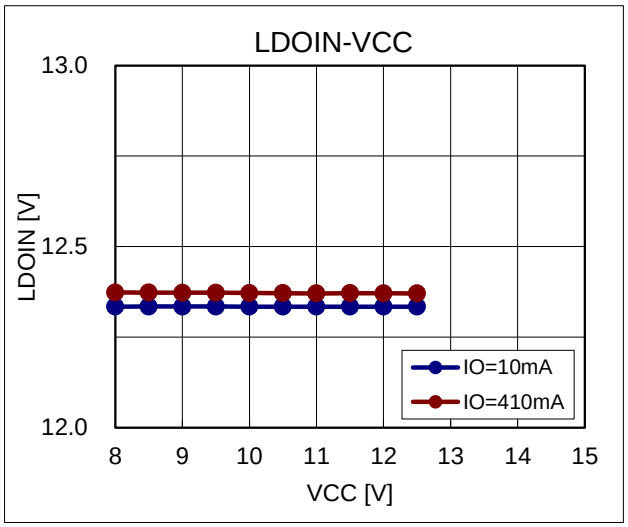
(1) Connect the test setup as shown in Figure 4
(2) Apply 12Vdc to VCC.
(3) Apply 2Vdc to V1.
(4) Apply Low level (0V) or High level (2V) signal to CTL.
(5) Apply Low level (0V) signal to EN.
(6) Check that LDOIN=0[V] and LDOOUT=0[V].
(7) Apply IO(load)=0[A] to LDOOUT.
(8) Apply High level (2V) signal to EN.
(9) If CTL state = Low, Check that LDOIN=12.3[V] and LDOOUT=11.7[V]
If CTL state = High, Check that LDOIN=16.5[V] and LDOOUT=15.9[V]
(10) Set IO to desired level, 0[mA] – 410[mA], and measure LDOOUT voltage and LDOIN voltage.
(11) Change CTL level to High or Low. And Confirm (9) and (10).
(12) Apply Low level signal to EN.
(13) Turn off IO(load).
(14) Turn off VCC, V1, CTL and EN.

4.5 Reference data (Ta=25˚C, VCC=12V, V1=2V)

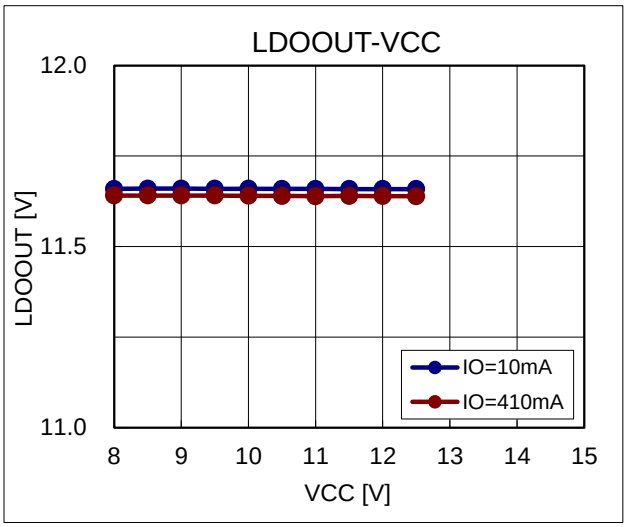
• Line Regulation (Load from LDOOUT)

CTL=Low

LDOIN (DC-DC boost converter output)

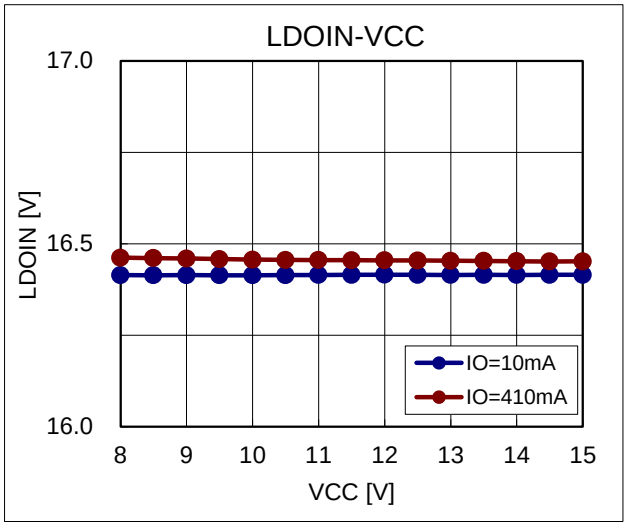


LDOOUT

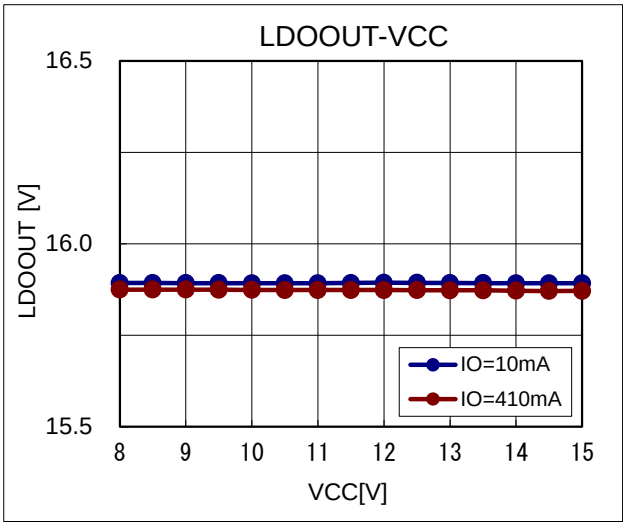


CTL=High

LDOIN (DC-DC boost converter output)



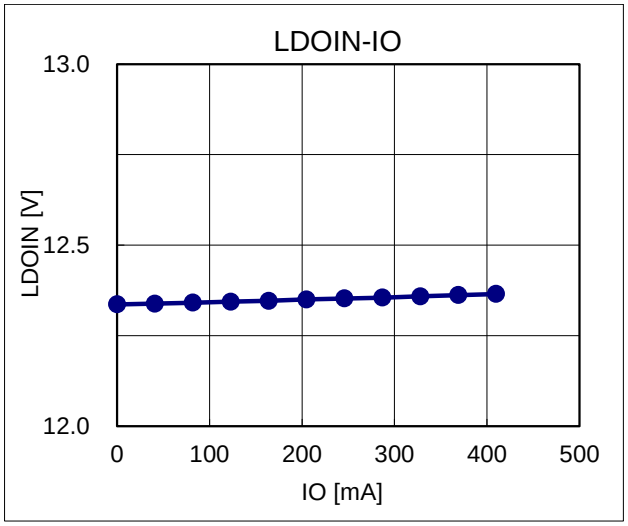
LDOOUT



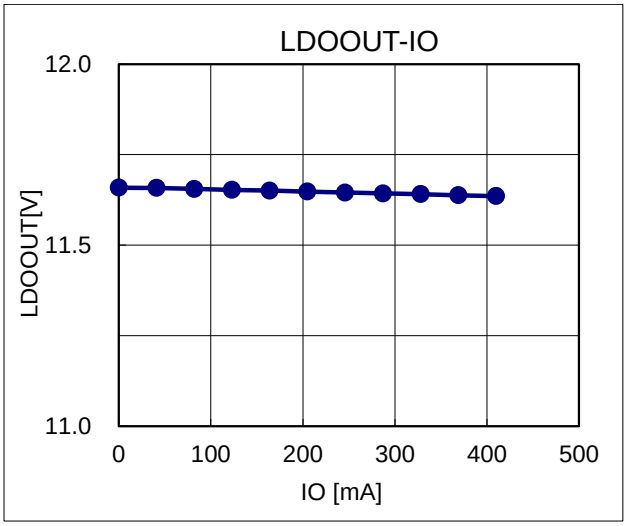
• Load Regulation (Load from LDOOUT)

CTL=Low

LDOIN (DC-DC boost converter output)

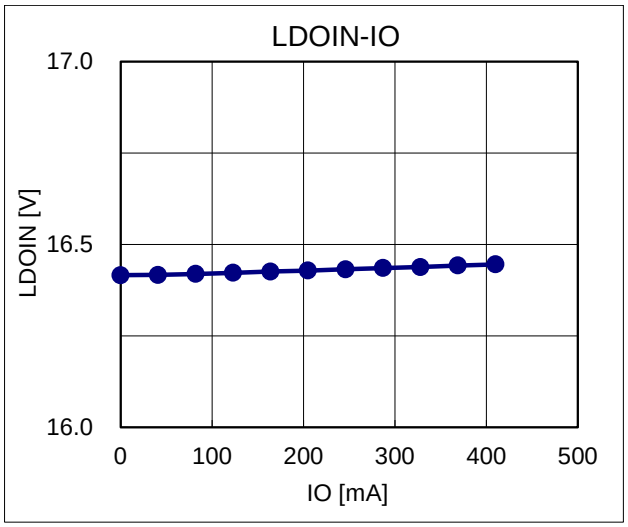


LDOOUT

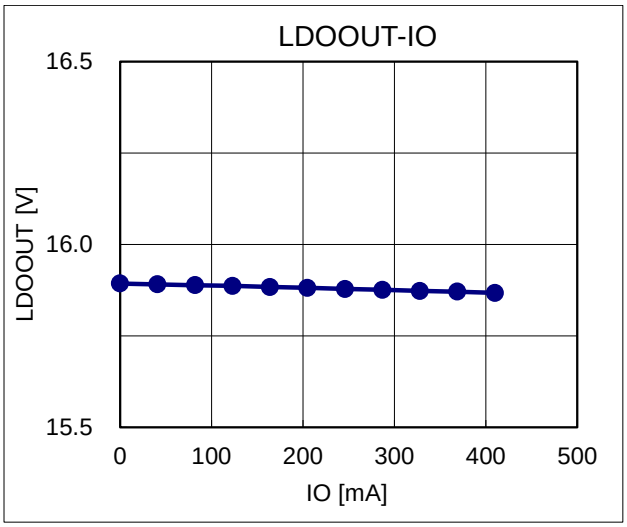


CTL=High

LDOIN (DC-DC boost converter output)



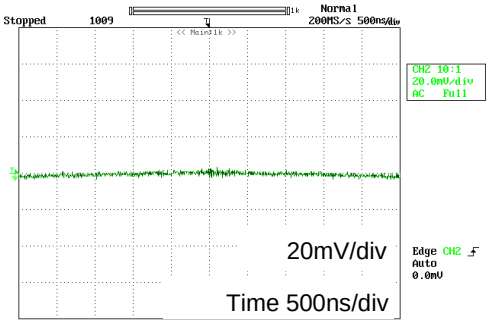
LDOOUT



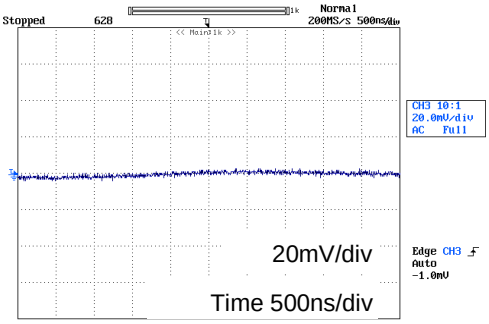
- Output waveform

CTL=Low, IO=0A(LDOOUT load)

LDOIN (DC-DC boost converter output)

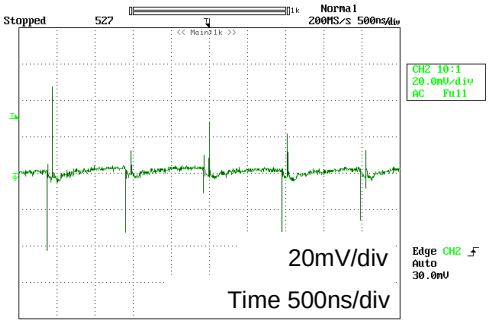


LDOOUT

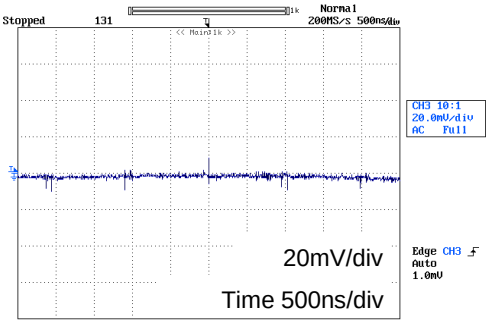


CTL=Low, IO=400mA(LDOOUT load)

LDOIN (DC-DC boost converter output)

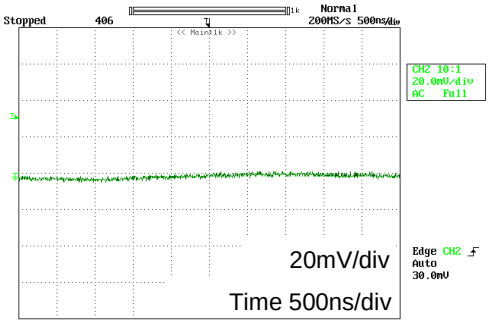


LDOOUT

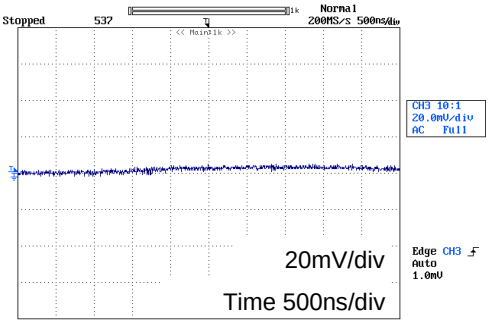


CTL=High, IO=0A(LDOOUT load)

LDOIN (DC-DC boost converter output)

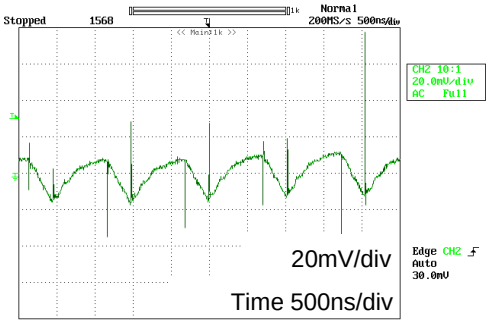


LDOOUT

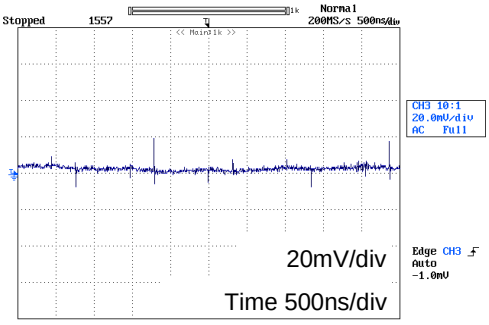


CTL=High, IO=400mA(LDOOUT load)

LDOIN (DC-DC boost converter output)



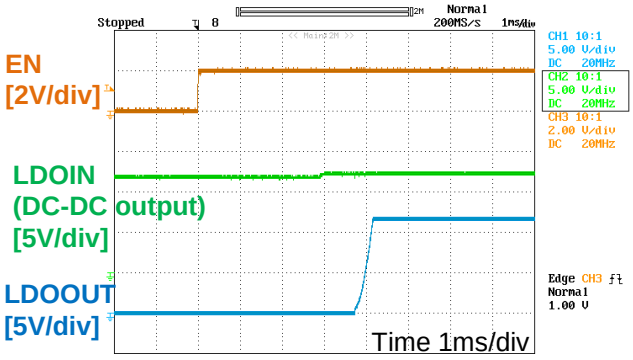
LDOOUT



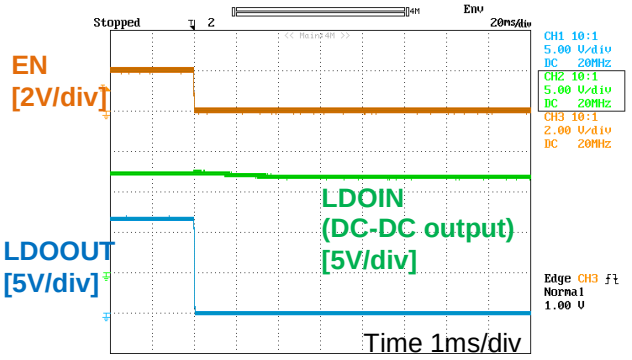
• Start-up and Stop waveform

VCC=12V, CTL=Low, IO=400mA(LDOOUT load)

Start-up

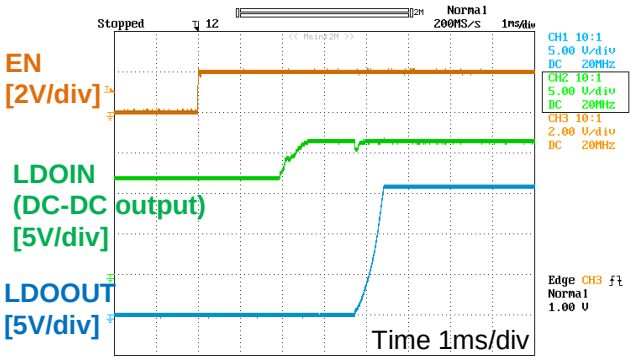


Stop

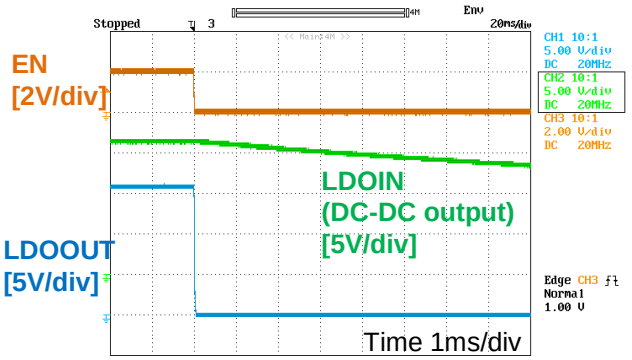


VCC=12V, CTL=High, IO=400mA(LDOOUT load)

Start-up

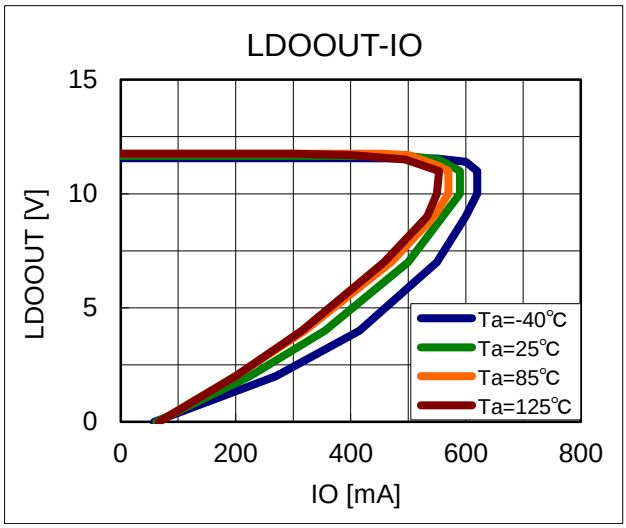


Stop

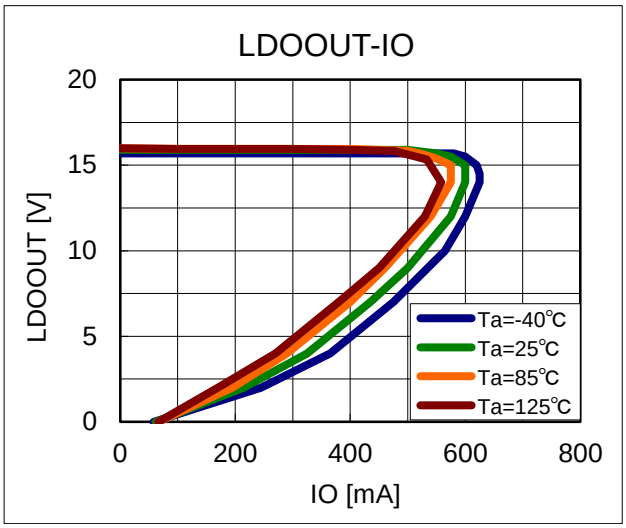


• LDO current limit operation

CTL=Low

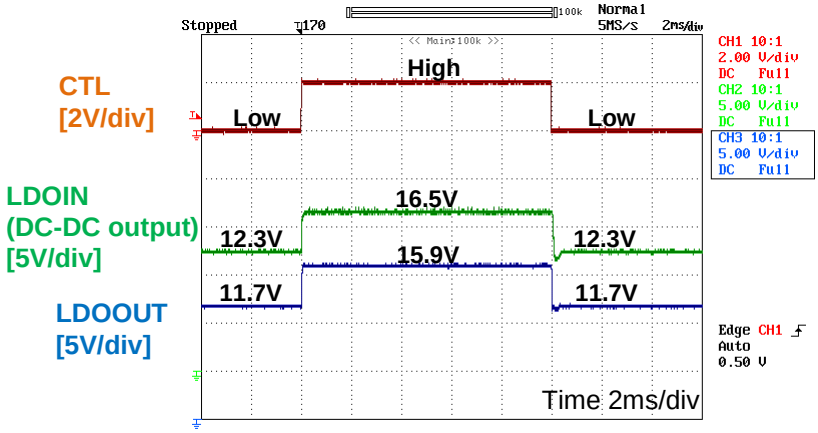


CTL=High



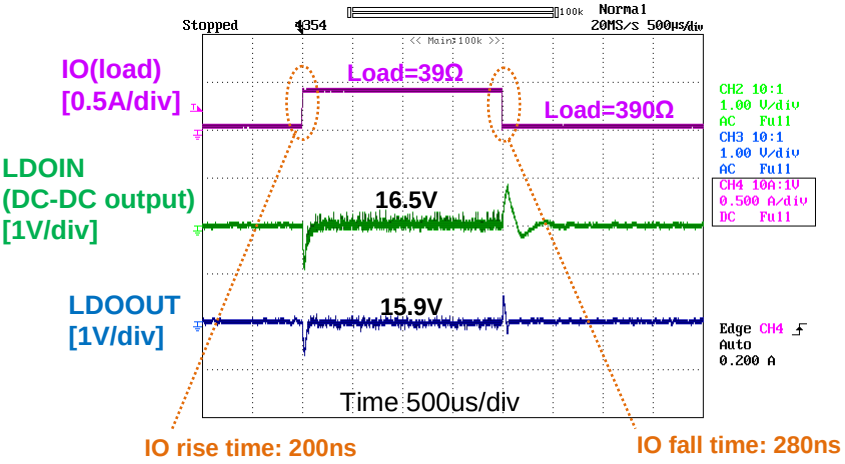
• Output waveform at CTL switching (High/Low)

LDOOUT load =39Ω

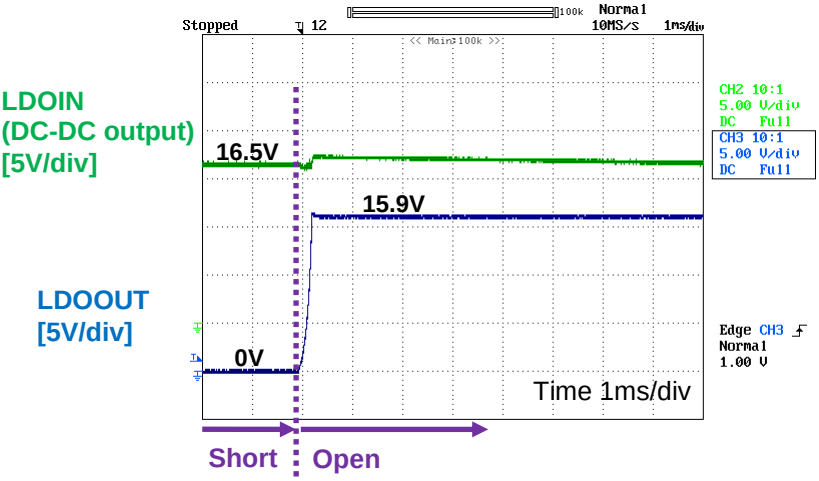


• Load transient response (Load from LDOOUT)

CTL=High, LDOOUT load =39Ω↔390Ω

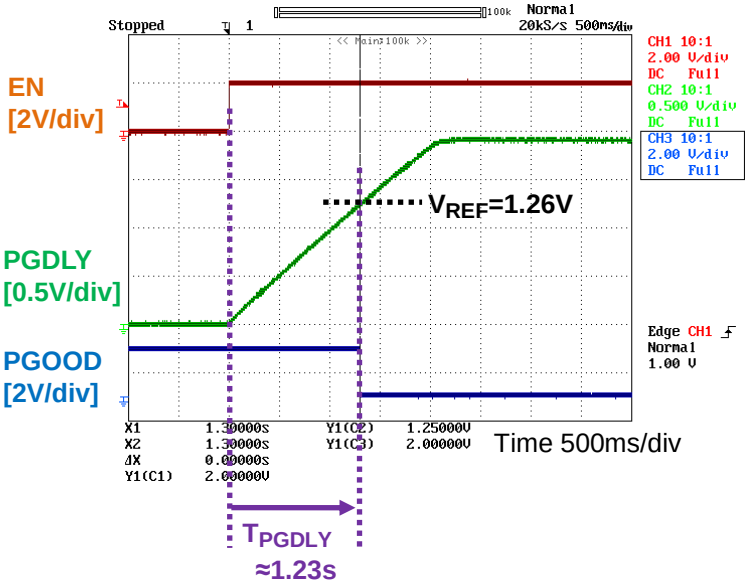


CTL=High, LDOOUT=GND Short → Open



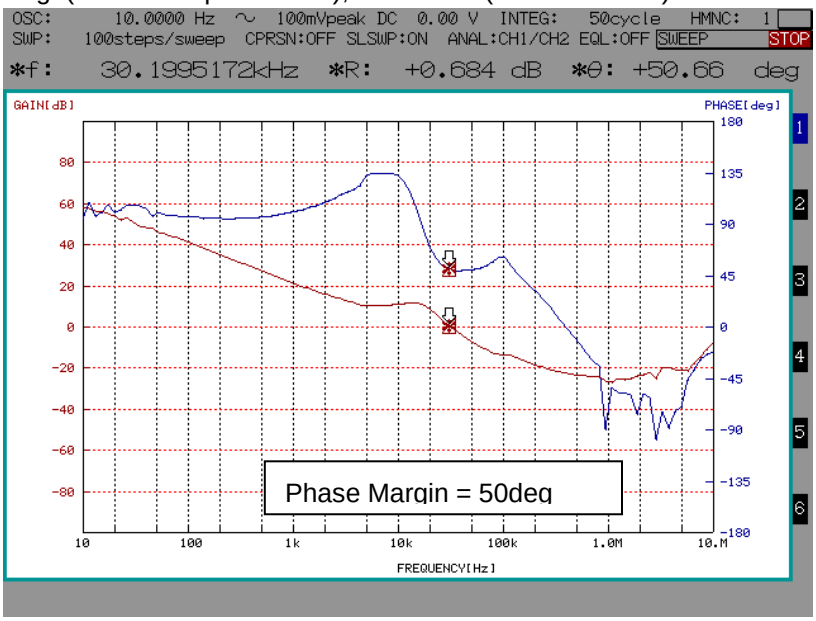
- PGOOD operation waveform

  LDOOUT=GND short, EN: Low→High



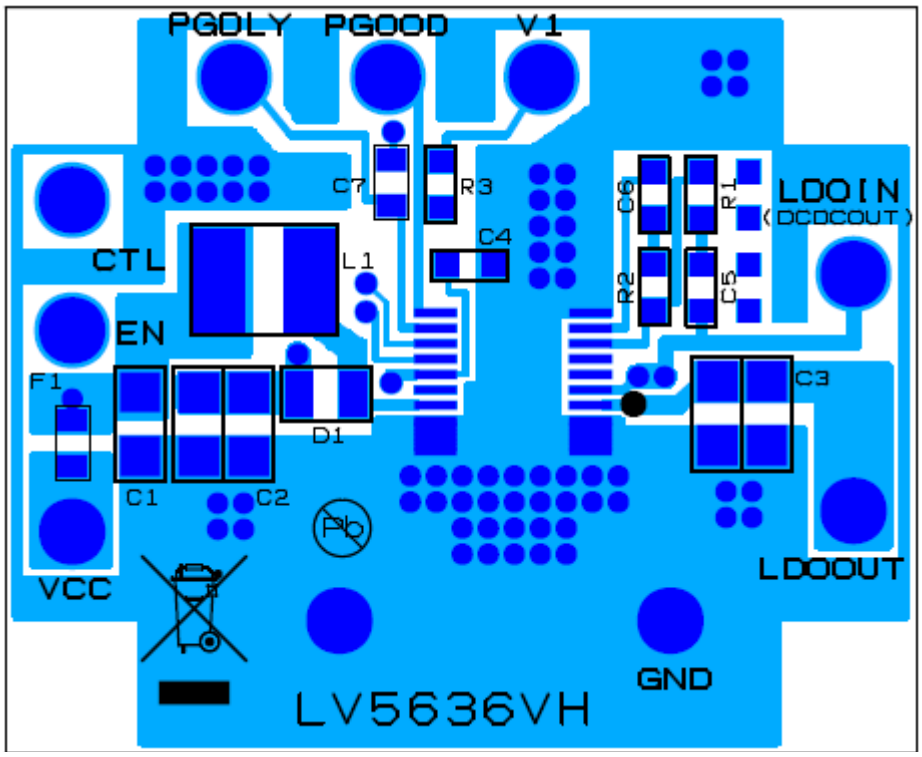
- DC-DC boost converter Gain & Phase frequency response

  CTL=High(DC-DC output =16.5V), IO=400mA(LDOOUT load)

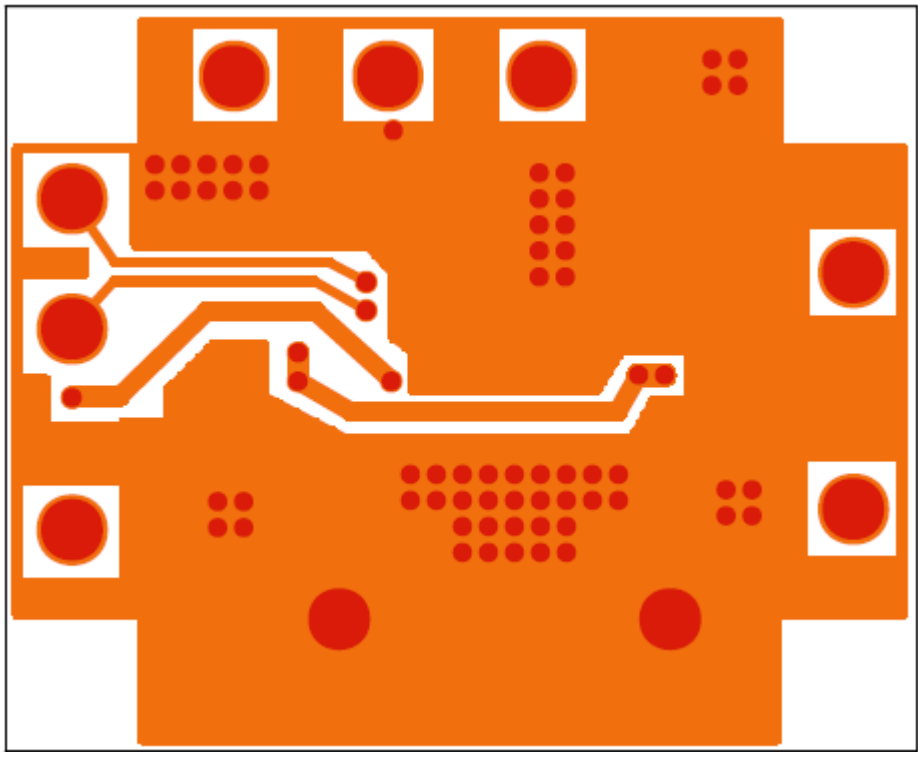


4.6 Board Layout

• Top-Side



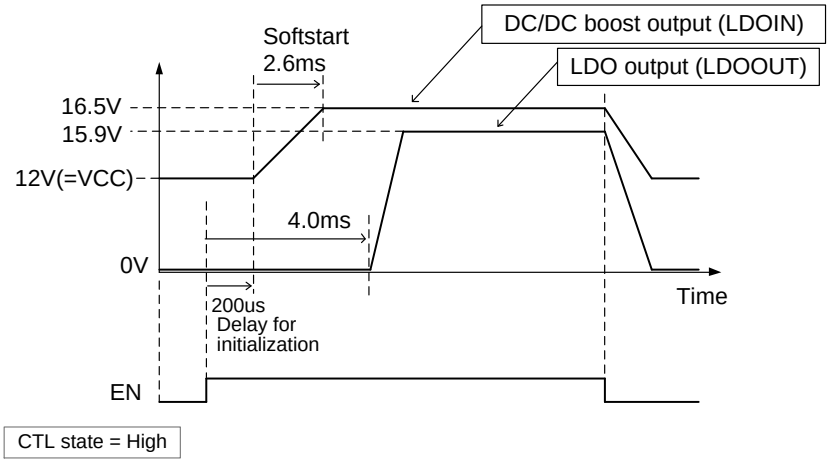
• Bottom-Side



Board size: 63.0mm×38.5mm

5. Detailed description

5.1 Start-up and Stop Diagram



5.2 Power Good Delay

Power good notifies that the output voltage of LDO is within the range of the setting voltage. The output is judged to be “power good” when both outputs are 85% or higher compared to the setting voltages. If the output voltage falls below 85%, PGOOD output becomes H→L(No Good). At “Good” →”No Good”, delay time can be set. To define Power Good delay time (T_{PGDLY}), you need to calculate a value of PGDLY capacitor (C7) using the following formula.

$$T_{PGDLY} = \frac{C7 \times V_{REF}}{I_{PGDLY}}$$

where,

V_{REF} = 1.26 V (typical)

I_{PGDLY} = 4.8 uA (typical)

5.3 Inductor

In DCDC boost converter, the current as shown in the figure on the right-hand side flows through inductor.

DCDC boost converter output voltage (VOUT) is given by the following expression.

$$VOUT = \frac{VIN}{1 - D}$$

where,

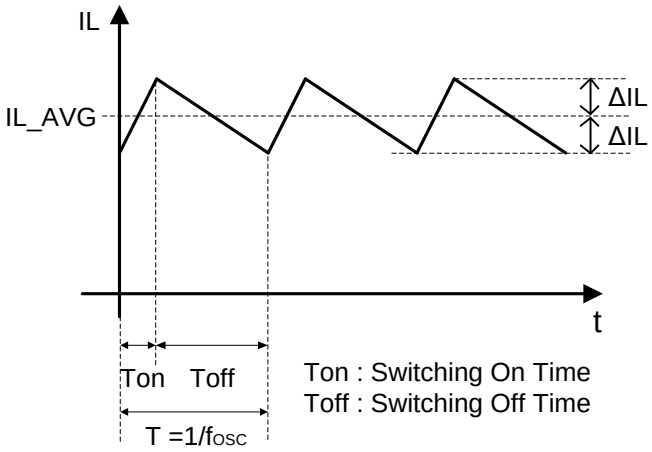
VIN : Input voltage

D : Power MOSFET ON Duty, $D = \frac{Ton}{T}$

Ton : Power MOSFET ON Time

T : Switching period, $T = \frac{1}{f_{OSC}}$

f_{OSC} : Switching frequency = 1 MHz (typical)



Ripple current of the inductor (ΔIL) is given by the following expression.

$$\Delta IL = \frac{VIN \times D}{2 \times L \times f_{OSC}} = \frac{VIN \times Ton}{2 \times L}$$

where,

L : Inductance value of L1

At the maximum output load (IO_{max}), the peak of the inductor current (ILpeak) is given by

$$ILpeak = IL\_AVG_{[max]} + \Delta IL$$

where,

$IL\_AVG_{[max]}$: The average of inductor current at the maximum output load

Select an inductor (L1) which can permit ILpeak.

If ΔIL is higher than the average inductor current, the mode is switched to Discontinuous Mode.

5.3 Input capacitor

RMS ripple current of the input capacitor (C1,C4) is given by

$$Irms(Cin) = \frac{1}{2\sqrt{3}} \times \frac{VIN \times D}{L \times f_{OSC}}$$

Select the input capacitor which can be low ESR and enough capacitance value to supply the stable voltage to VCC pin.

5.4 Output capacitor for DCDC boost converter

RMS ripple current of the output capacitor (C2) for DCDC boost converter is given by

$$Irms(Cout) \approx IO \times \sqrt{\frac{VOUT - VIN}{VIN}}$$

where,

IO : Output load

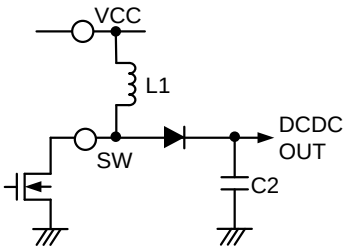
When VIN is minimum and IO is maximum, Irms(Cout) is maximum. Select the output capacitor which can permit the maximum Irms(Cout). Use the capacitor which has enough margin to the maximum rating.

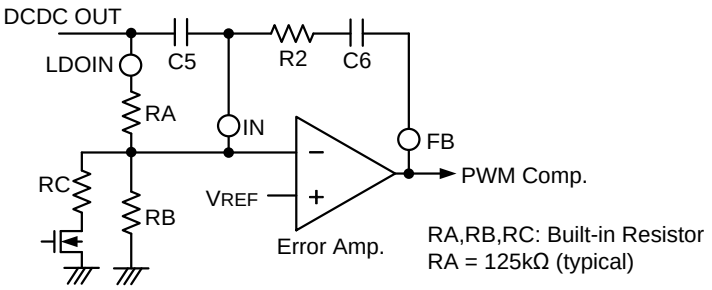
5.5 Rectifier diode for DCDC boost converter

Use the Schottky Diode as rectifier diode for DCDC boost converter. Make sure that the diode meets the following 3 conditions: 1) rated reverse voltage of the diode is higher than output voltage, 2) rated average current is higher than maximum load current and 3) rated surge forward current is higher than peak inductor current.

5.6 Phase compensation for DCDC boost converter

To stabilize DCDC boost converter by phase compensation, you need to cancel double pole (-180deg) caused by LC with 2 zeros (+90deg ×2). Set the frequency of 2 zeros near the LC resonance frequency.





【LC resonance frequency】

$$f_r = \frac{1}{2\pi\times\sqrt{L1\times C2}} \ [Hz]$$

【Zero】

$$f_{z1} = \frac{1}{2\pi\times\sqrt{C5\times RA}} \ [Hz]$$

$$f_{z2} = \frac{1}{2\pi\times\sqrt{C6\times R2}} \ [Hz]$$