LV8760T/LV8761V

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Bi-CMOS LSI

Forward/Reverse H-bridge Driver Application Note

Overview

The LV8760T /LV8761V are an H-bridge driver that can control four operation modes (forward, reverse, brake, and standby) of a motor. The low on-resistance, zero standby current, highly efficient IC is optimal for use in driving brushed DC motors for office equipment.

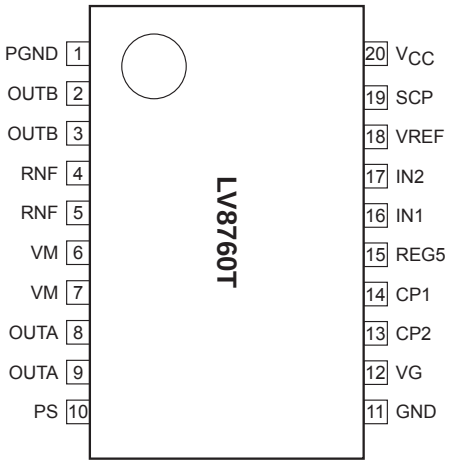
Function

- Forward/reverse H-bridge motor driver: 1 channel
- Built-in current limiter circuit
- Built-in thermal protection circuit
- Built-in short-circuit protection function
- Unusual condition warning output pin (LV8761V only)
- Short-circuit protection circuit selectable from latch-type or auto reset-type (LV8761V only)

Typical Applications

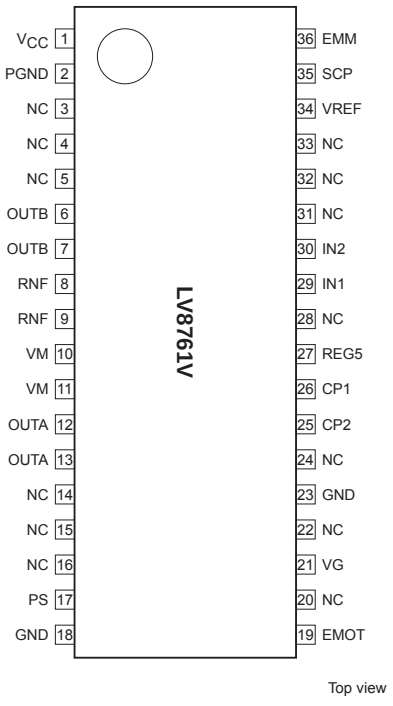
- MFP (Multi Function Printer)
- PPC (Plain Paper Copier)
- LBP (Laser Beam Printer)
- Photo Printer
- Scanner
- Industrial
- Cash Machine
- Entertainment

Pin Assignment



TSSOP20J (225mil)

Packages are not to scale.

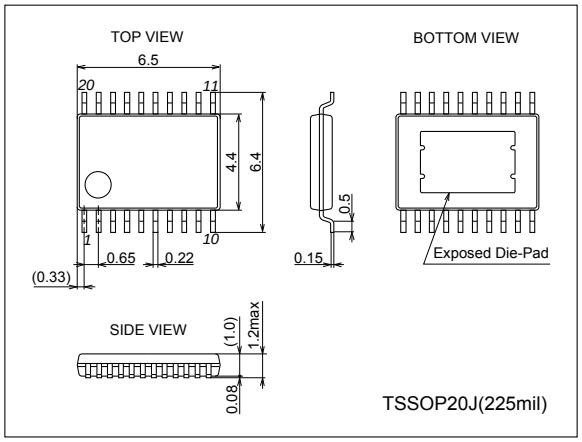


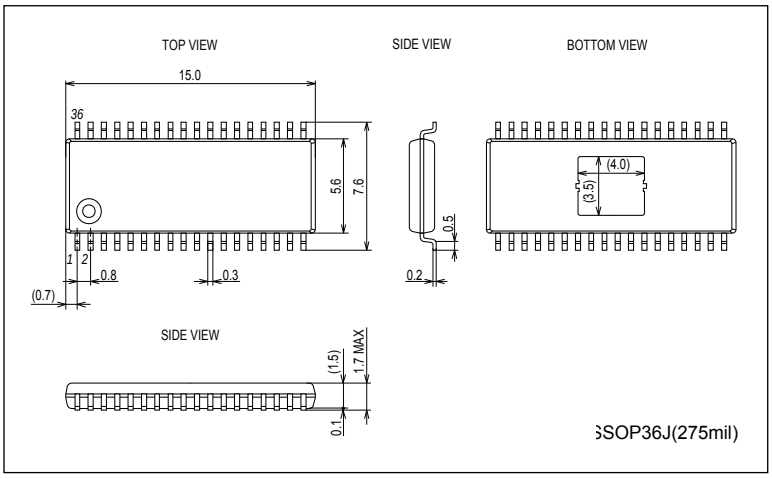
SSOP36J (275mil)

December, 2013

Package Dimensions

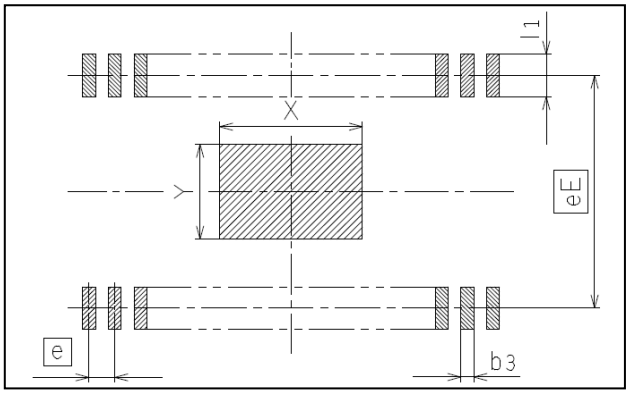
Unit: mm (typ)





Caution: The package dimension is a reference value, which is not a guaranteed value.

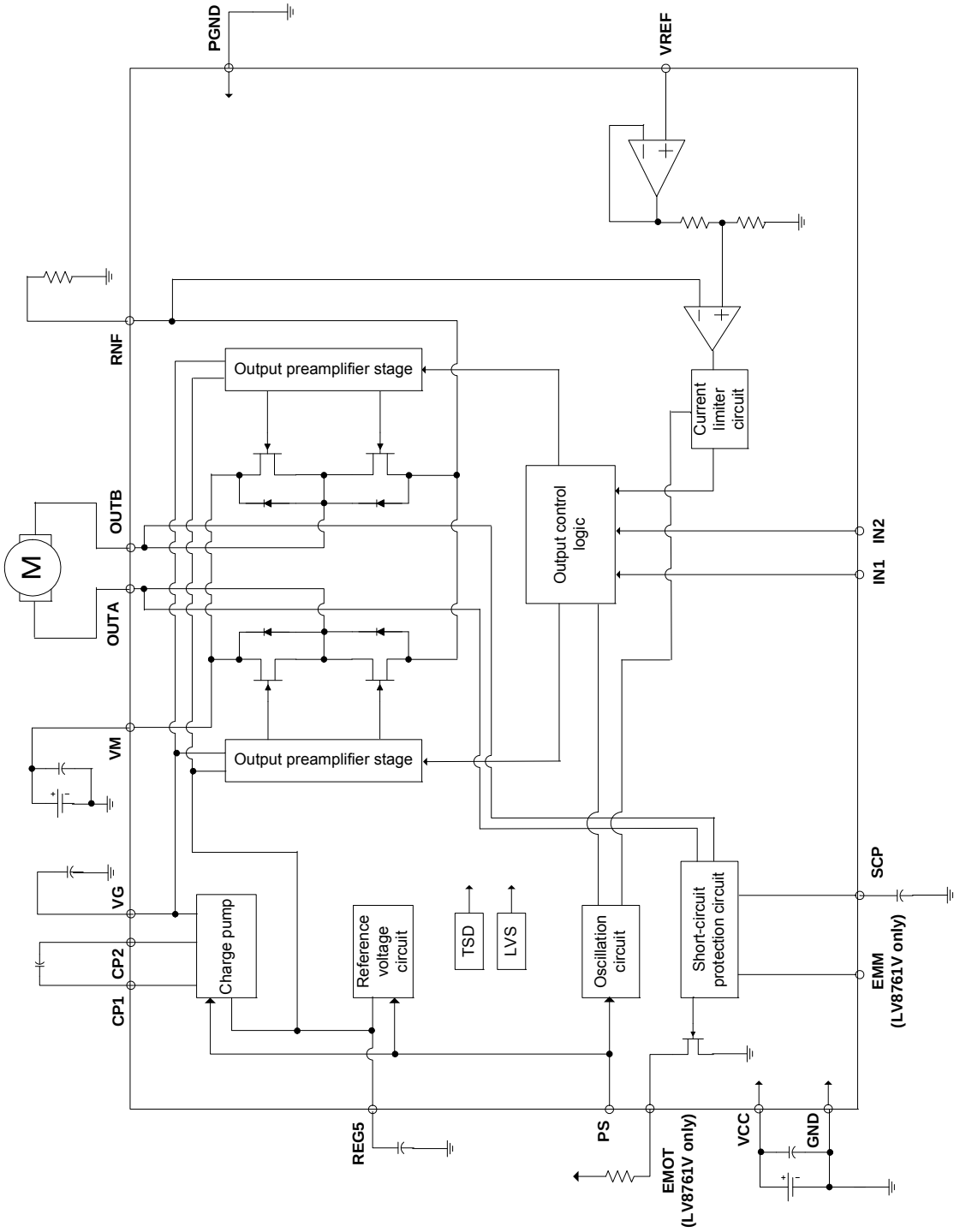
Recommended Soldering Footprint



(Unit:mm)

Reference symbol	TSSOP20J (225mil)	SSOP36J (275mil)
eE	5.80	7.00
e	0.65	0.8
b3	0.32	0.42
l1	1.00	1.00
X	(4.3)	(4.0
Y	(2.8)	(3.5)

Block Diagram



Selection Guide

Part Number	Short-circuit protection	Package
LV8760T	Latch-type	TSSOP20J (225mil) with Exposed Die-Pad
LV8761V	Latch-type/Auto reset-type, Warning output	SSOP36J (275mil) with Exposed Die-Pad

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VM max		38	V
	V_{CC} max		6	V
Output peak current	I_O peak	tw ≤ 20ms, duty 5%	4	A
Output continuous current	I_O max		3	A
Logic input voltage	V_{IN}		-0.3 to V_{CC}+0.3	V
Allowable power dissipation	Pd max	LV8760T *	3.3	W
		LV8761V *	3.15	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*** Specified circuit board: 90mm×90mm×1.6mm, glass epoxy 2-layer board (2S0P), with backside mounting.**

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	VM		9		35	V
	V_{CC}		3		5.5	V
VREF input voltage	VREF		0		V_{CC}-1.8	V
Logic input voltage	V_{IN}		0		V_{CC}	V

Electrical Characteristics at Ta = 25°C, VM = 24V, V_{CC} = 5V, VREF = 1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
General						
Standby mode current drain 1	IMst	PS = "L"			1	μA
Standby mode current drain 2	I_{CC}st	PS = "L"			1	μA
Operating mode current drain 1	IM	PS = "H", IN1 = "H", with no load		1	1.3	mA
Operating mode current drain 2	I_{CC}	PS = "H", IN1 = "H", with no load		3	4	mA
VREG output voltage	VREG	I_O = -1mA	4.75	5	5.25	V
V_{CC} low-voltage cutoff voltage	VthV_{CC}		2.5	2.7	2.9	V
Low-voltage hysteresis voltage	VthHIS		120	150	180	mV
Thermal shutdown temperature	TSD	Design guarantee *	155	170	185	°C
Thermal hysteresis width	ΔTSD	Design guarantee *		40		°C
Output block						
Output on resistance	Ron1	I_O = 3A, sink side		0.2	0.25	Ω
	Ron2	I_O = -3A, source side		0.32	0.40	Ω
Output leakage current	$I_O$leak	V_O = 35V			50	μA
Rising time	tr	10% to 90%		200	500	ns
Falling time	tf	90% to 10%		200	500	ns
Input output delay time	tpLH	IN1 or IN2 to OUTA or OUTB (L → H)		550	700	ns
	tpHL	IN1 or IN2 to OUTA or OUTB (H → L)		550	700	ns
Charge pump block						
Step-up voltage	VGH	VM = 24V	28.0	28.7	29.8	V
Rising time	tONG	VG = 0.1μF		250	500	μs
Oscillation frequency	Fcp		115	140	165	kHz

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Control system input block						
Logic pin input current 1	$I_{IN}L$	V_{IN} = 0.8V adaptive pin : PS	5.6	8	10.4	μA
	$I_{IN}H$	V_{IN} = 5V adaptive pin : PS	56	80	104	μA
Logic pin input current 2	$I_{IN}L$	V_{IN} = 0.8V adaptive pin : IN1, IN2	5.6	8	10.4	μA
	$I_{IN}H$	V_{IN} = 5V adaptive pin : IN1, IN2	35	50	65	μA
Logic pin input H-level voltage	$V_{IN}H$	adaptive pin : PS, IN1, IN2	2.0			V
Logic pin input L-level voltage	$V_{IN}L$	adaptive pin : PS, IN1, IN2			0.8	V
Current limiter block						
VREF input current	IREF		-0.5			μA
Current limit comparator threshold voltage	Vthlim	VREF = 1.5V	0.285	0.3	0.315	V
Short-circuit protection block						
SCP pin charge current	Iscp	SCP = 0V	3.5	5	6.5	μA
Comparator threshold voltage	Vthscp		0.8	1	1.2	V
EMO output saturation voltage (LV8761V only)	Vemo	Io = 500μA		0.3	0.4	V

* Design guarantee value and no measurement is made.

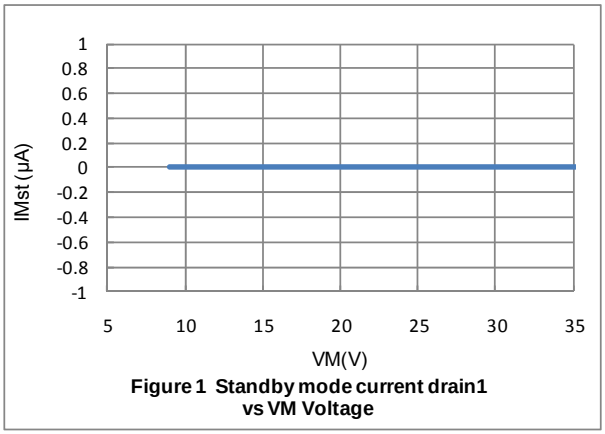


Figure 1 Standby mode current drain1 vs VM Voltage

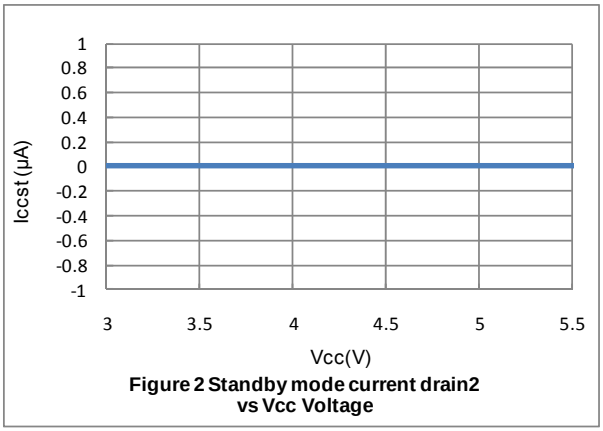


Figure 2 Standby mode current drain2 vs Vcc Voltage

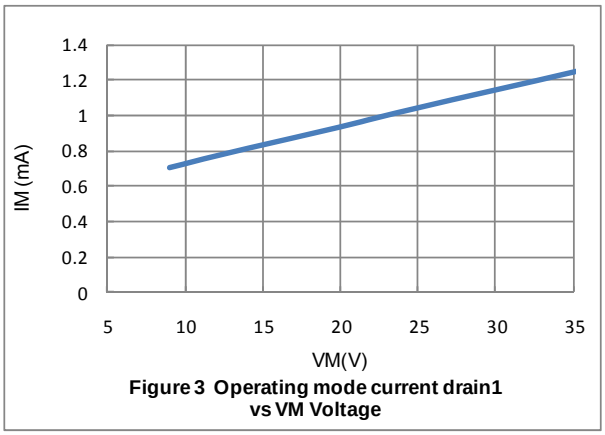


Figure 3 Operating mode current drain1 vs VM Voltage

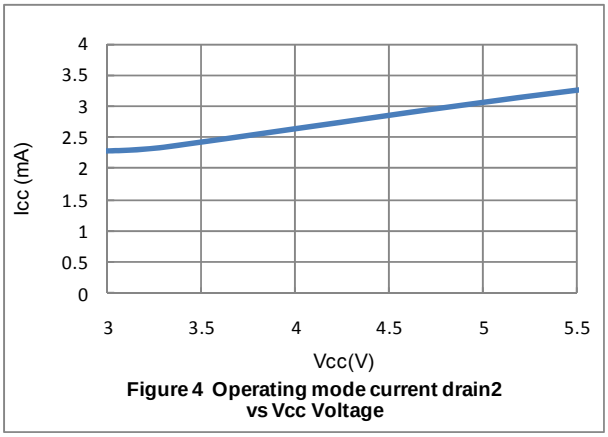


Figure 4 Operating mode current drain2 vs Vcc Voltage

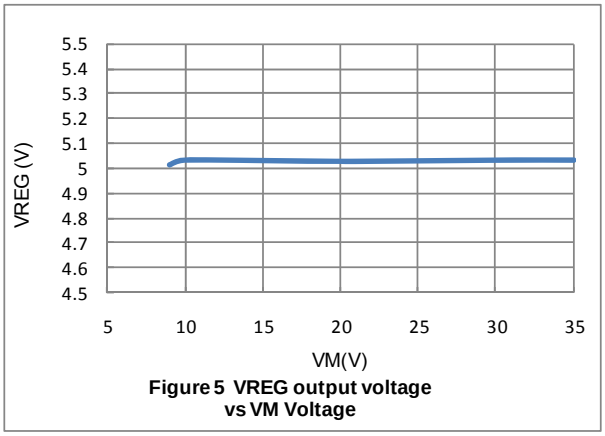


Figure 5 VREG output voltage vs VM Voltage

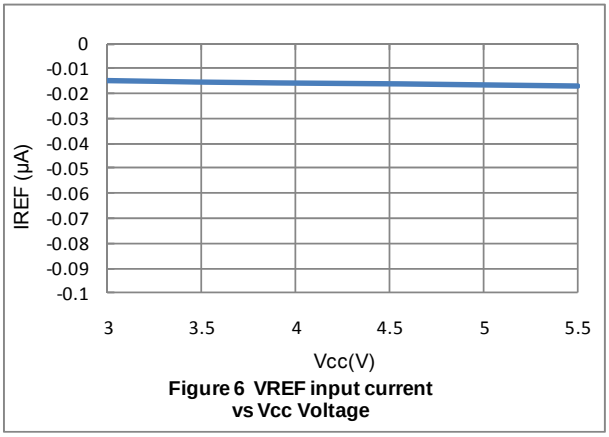


Figure 6 VREF input current vs Vcc Voltage

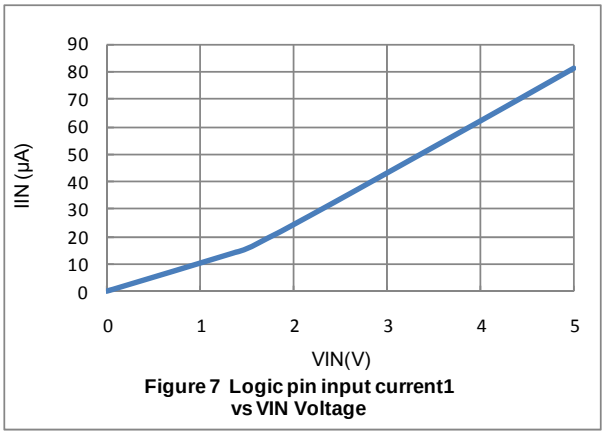


Figure 7 Logic pin input current1 vs VIN Voltage

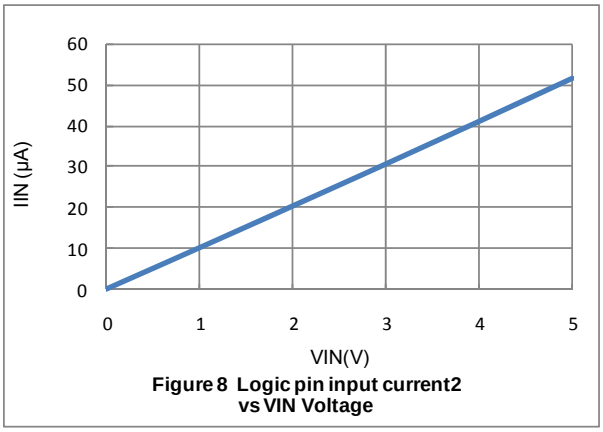


Figure 8 Logic pin input current2 vs VIN Voltage

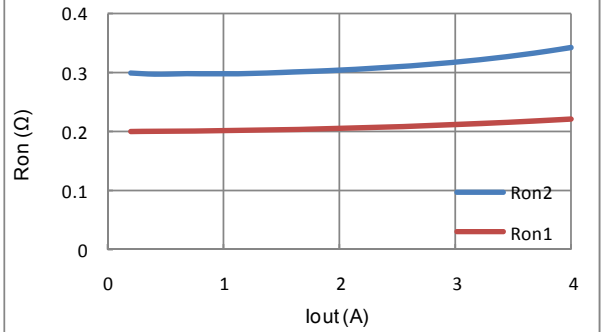


Figure 9 Output on Resistance vs Output Current

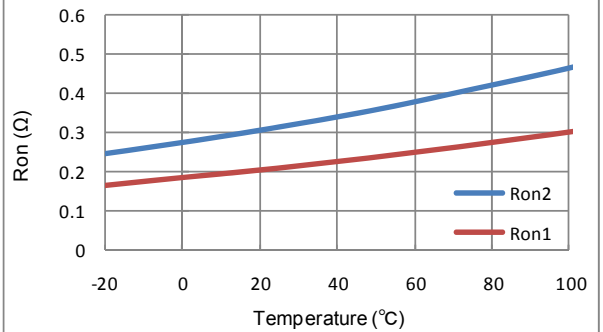


Figure 10 Output on Resistance(Io=3A) vs Temperature

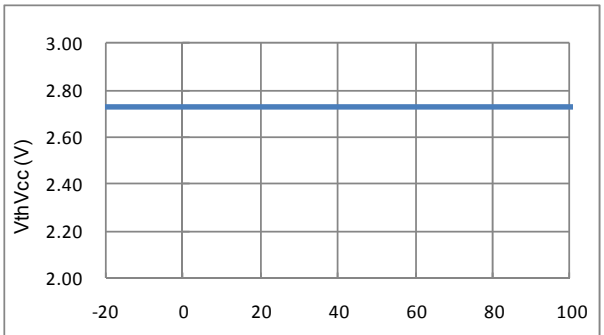


Figure 11 Vcc low-voltage cutoff voltage vs Temperature

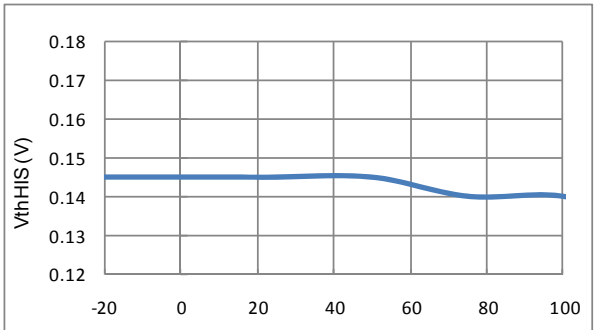


Figure 12 Low-voltage hysteresis voltage vs Temperature

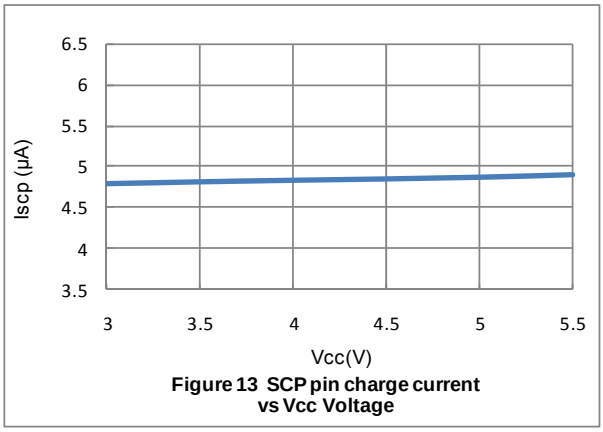


Figure 13 SCP pin charge current vs Vcc Voltage

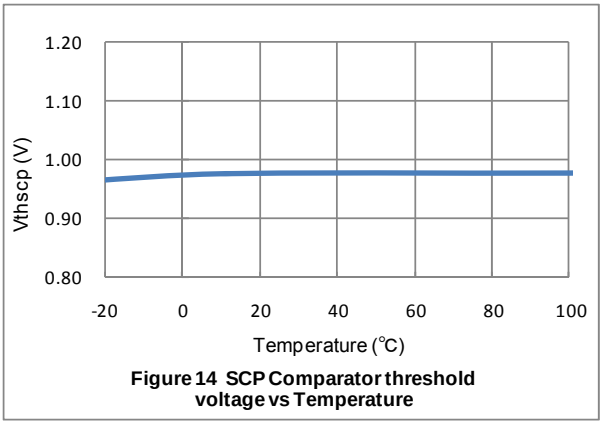


Figure 14 SCP Comparator threshold voltage vs Temperature

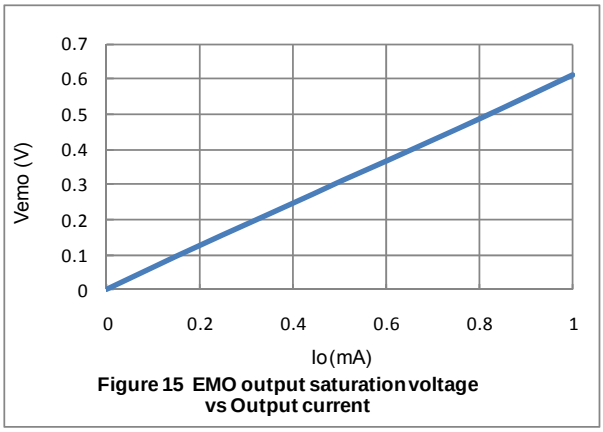
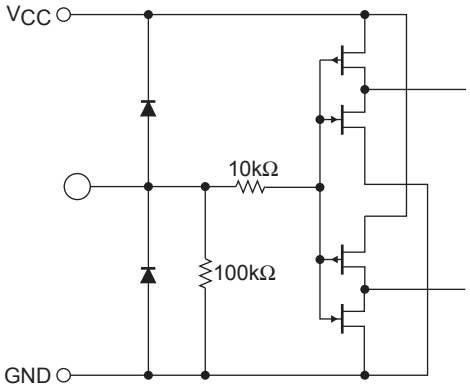
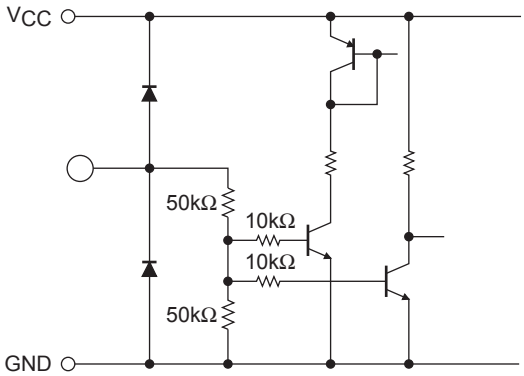
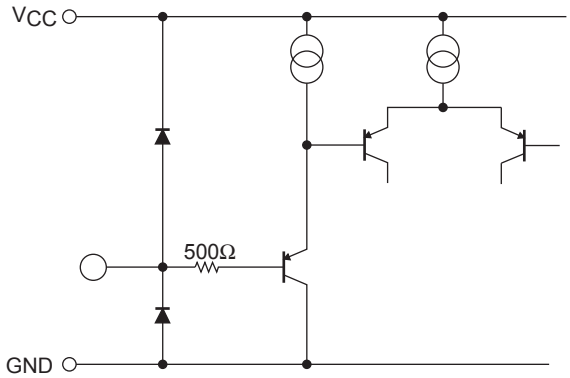
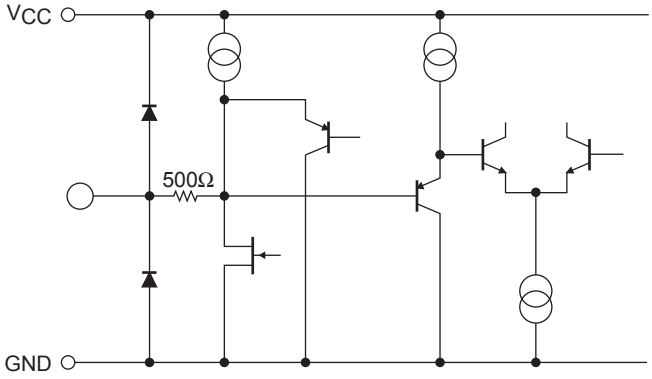


Figure 15 EMO output saturation voltage vs Output current

Pin Functions

Pin No.		Pin Name	Pin Function	Equivalent Circuit
LV8760T	LV8761V			
16 17 —	29 30 36	IN1 IN2 EMM	Output control signal input pin 1. Output control signal input pin 2 Short-circuit protection circuit mode switching pin.	
10	17	PS	Power save signal input pin.	
18	34	VREF	Reference voltage input pin for output current limit setting.	
19	35	SCP	Short-circuit protection circuit, detection time setting capacitor connection pin.	
20	1	VCC	Power supply connection pin for control block.	

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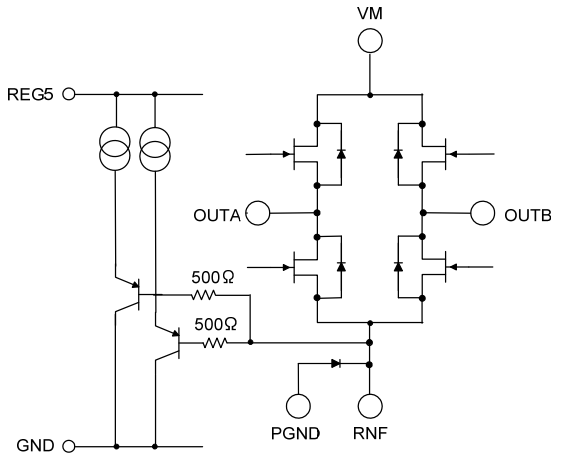
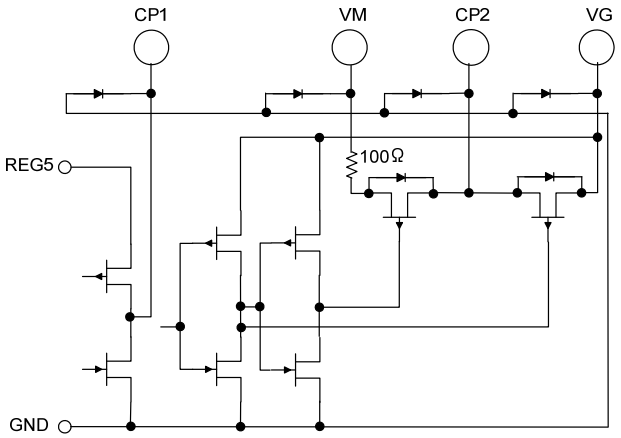
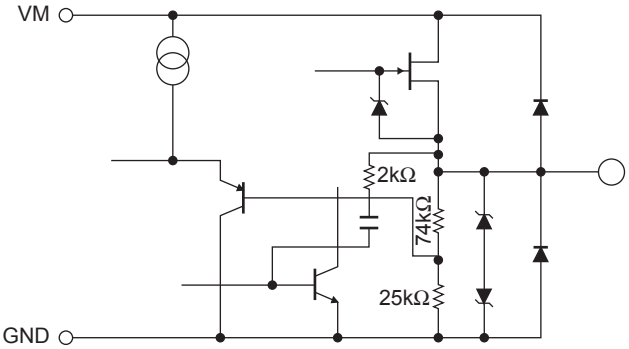
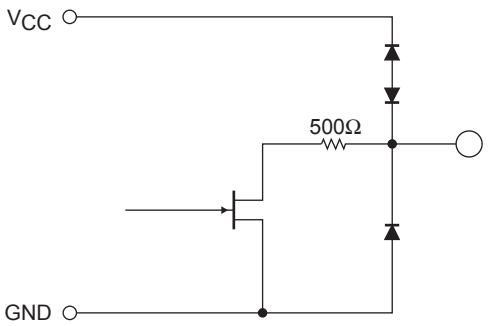
Pin No.		Pin Name	Pin Function	Equivalent Circuit
LV8760T	LV8761V			
6, 7 8, 9 4, 5 2, 3 1	10,11 12,13 8,9 6,7 2	VM OUTA RNF OUTB PGND	Motor power-supply connection pin. OUTA output pin. Current sense resistor connection pin. OUTB output pin. Power ground.	
14 13 12	26 25 21	CP1 CP2 VG	Charge pump capacitor connection pin. Charge pump capacitor connection pin. Charge pump capacitor connection pin.	
15	27	REG5	Internal reference voltage output pin.	
—	19	EMOT	Unusual condition warning output pin.	
11	18,23	GND	Ground.	

DC Motor Driver Operation

1. The recommended order of power supply

It is recommendable that the power supplies are turned on in the following order.

VCC power supply order → VM power supply order → PS pin = High→IN1/IN2 pin control

It becomes the above-mentioned opposite for power supply OFF.

VCC is the controller power supply and VM is the motor power supply. Output FET is controllable safely by powering VCC first to define the state of output FET before powering VM.
If VM is powered first before VCC, output FET cannot be controlled and the operation becomes unstable. However, the above-mentioned order is presented only as a recommendation, and noncompliance is not going to be the cause of over-current or IC destruction.

Also, there are some other cautions to be addressed for the order of power supply.

(1) When VM = 0V and VCC is powered and PS = IN1 (or IN2) = H, even if the control signal is applied to drive output FET, since the output pin is 0V, the short protector circuit detects error state and the output is latched-off. Therefore, make sure to power VCC/VM first and turn on control input (PS, IN1, IN2), then turn on the output.

(2) When the PS pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + REG5 voltage.
The charge pump output (VG) is used to drive gate of the upper FET. If the output is turned on while VG is not sufficiently boosted, the performance of the upper FET decreases, which lowers output voltage. As a result, short protector circuit may operate. Hence, make sure to secure a wait time equivalent to “tONG” or longer after PS turns High.
The output latch-off caused by over current can be cancelled by applying PS signal or re-powering VCC.

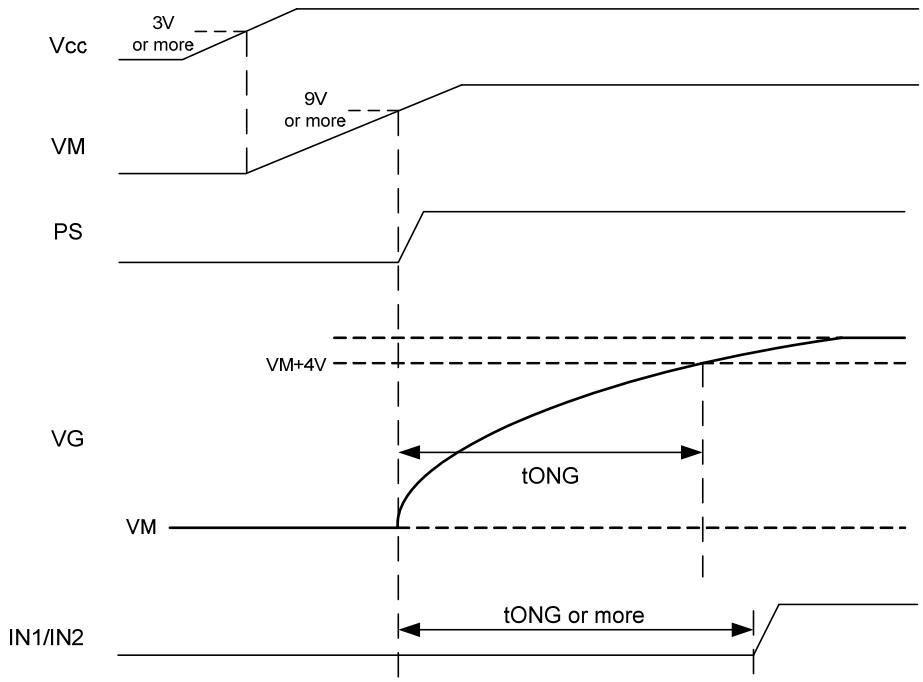


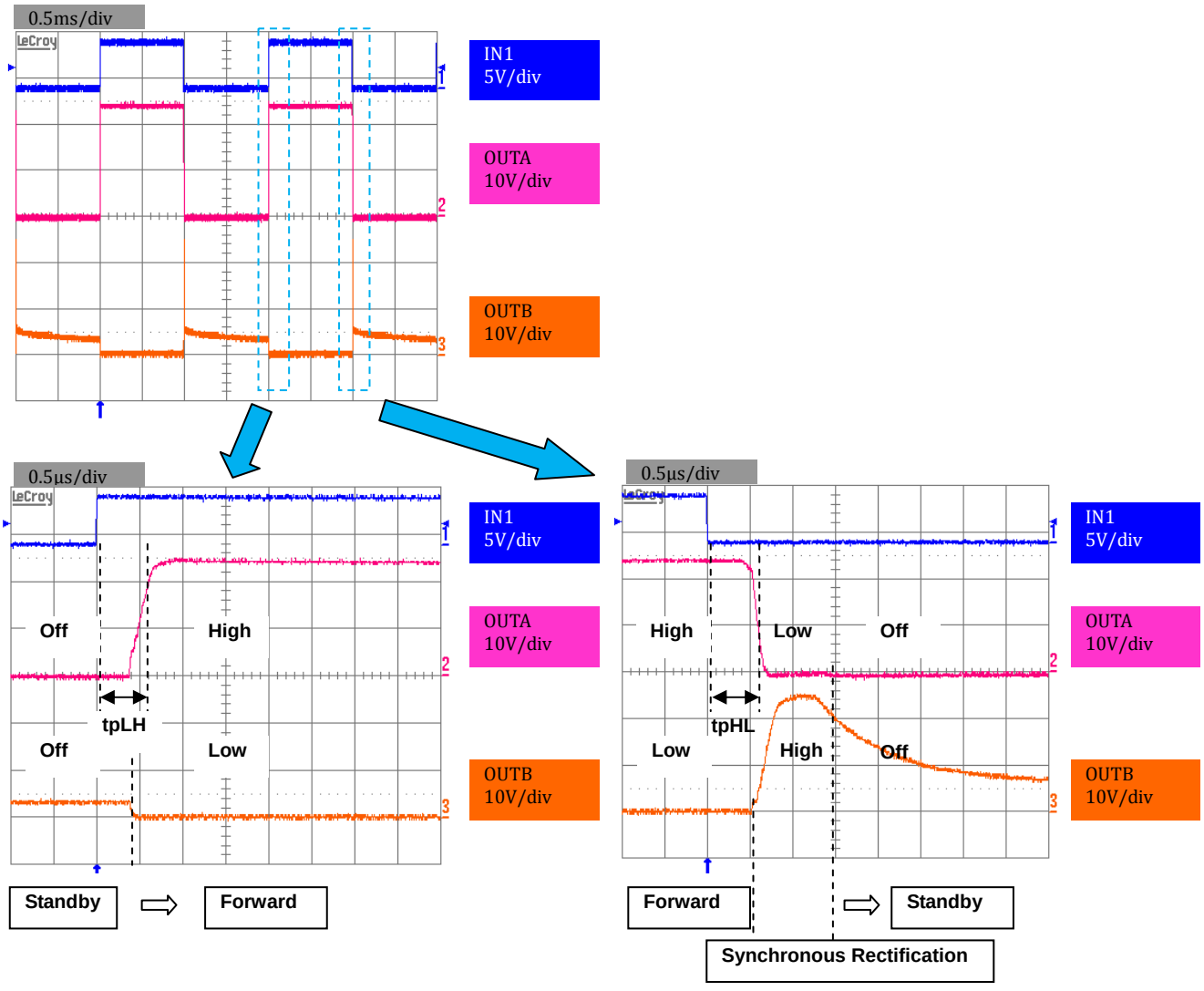
Figure 16. The turning on recommendation order timing chart

2. Output control logic table

Control Input			Output		Mode
PS	IN1	IN2	OUTA	OUTB	
L	*	*	OFF	OFF	Standby
H	L	L	OFF	OFF	Output OFF
H	H	L	H	L	CW (Forward)
H	L	H	L	H	CCW (Reverse)
H	H	H	L	L	Brake

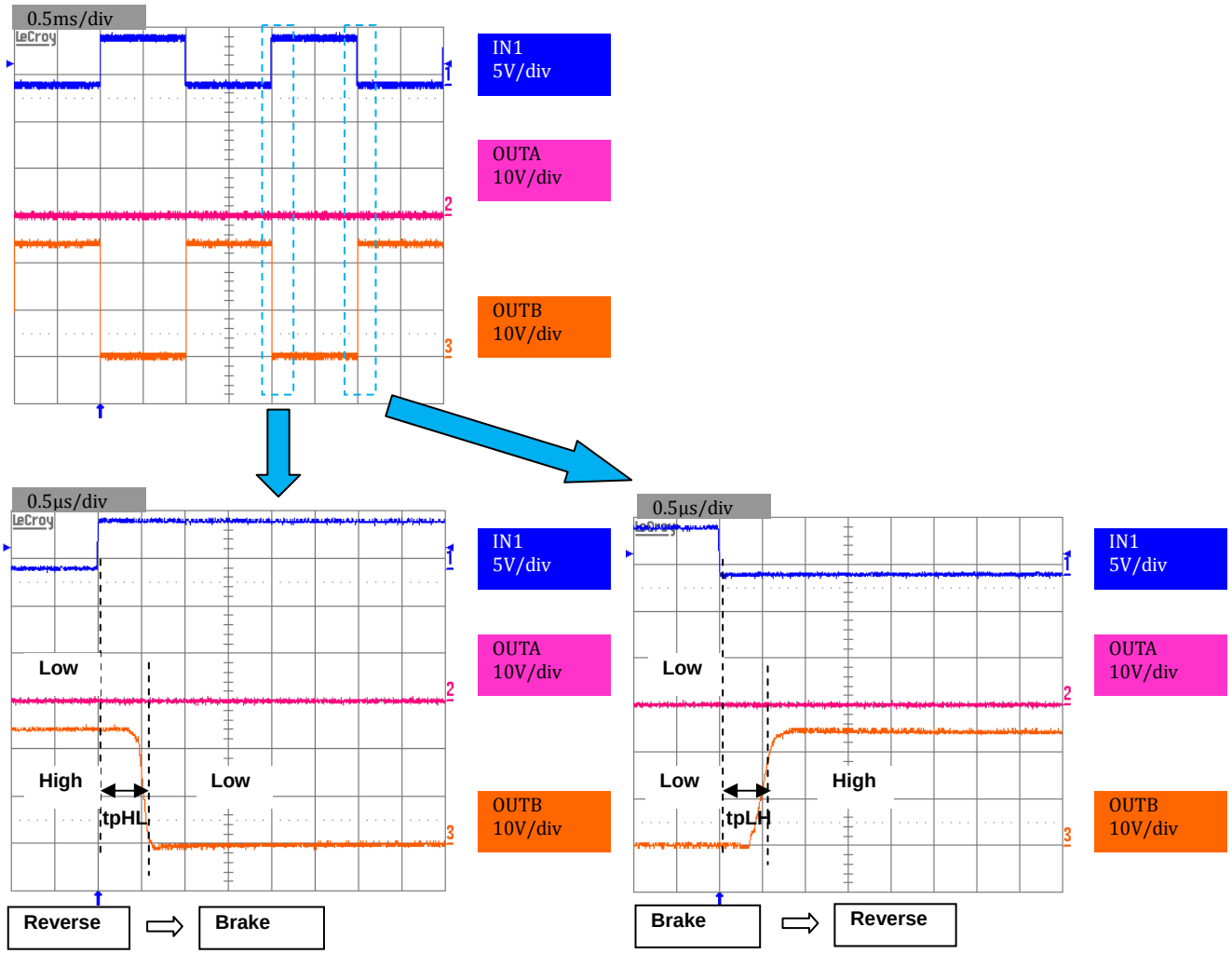
Output waveform example (No load)

Figure 17. Forward ↔ Output off switching
No load, PS=High, IN2=Low
Vcc=5V, VM=24V, VREF=1.5V



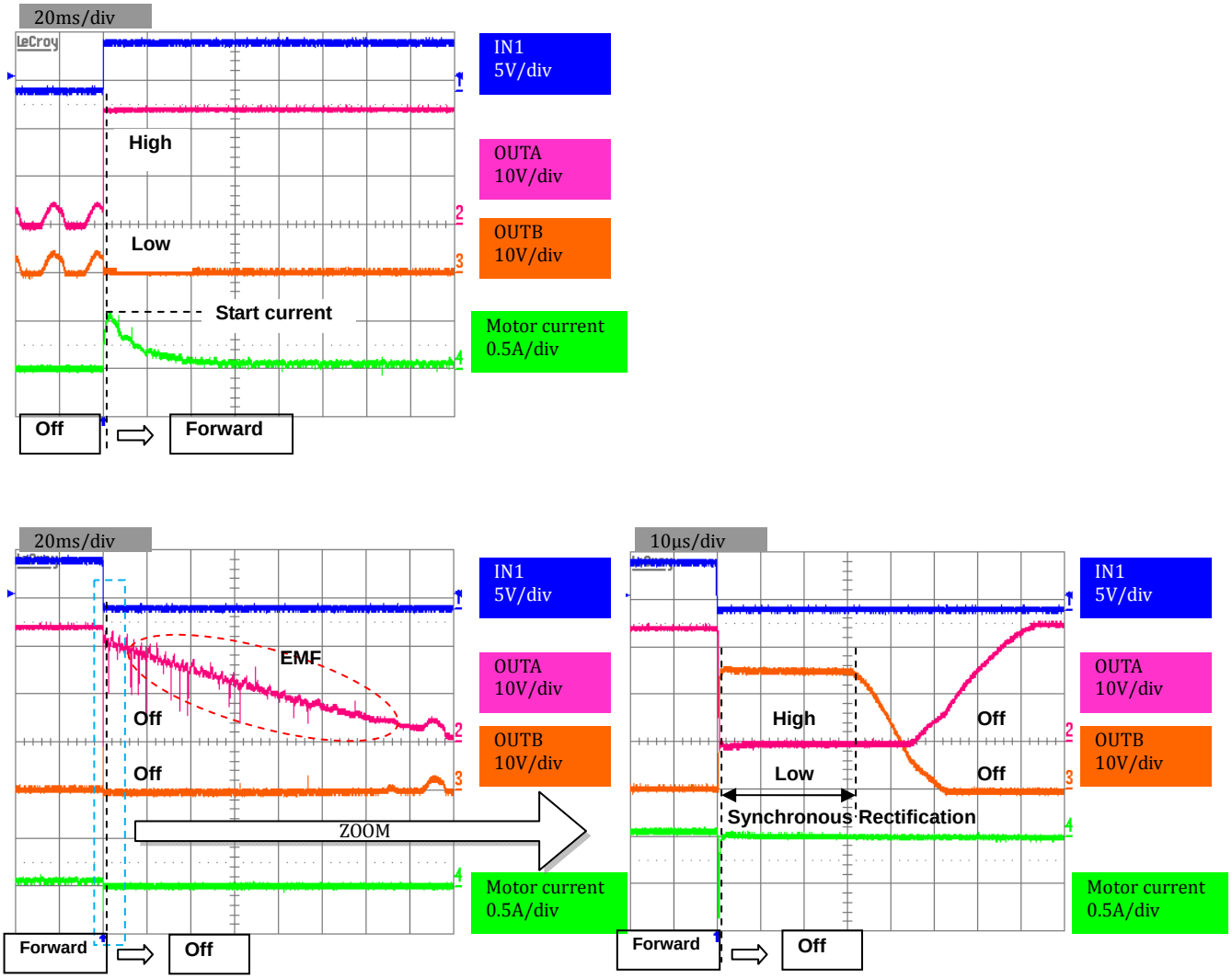
When changing the motor rotation from Forward mode to Standby mode, IC does not turn off at once. The counterpart FET is turned on first, and then the current is attenuated rapidly. (Synchronous Rectification) Afterwards, when the zero current level is detected, the load current is prevented from being reversed by turning off the synchronous rectifier.
Synchronous rectifier control reduces power dissipation during PWM operation.

Figure 18. Reverse ↔ Brake switching
No load, PS=High, IN2=High
Vcc=5V, VM=24V, VREF=1.5V



Output waveform example (DC motor load)

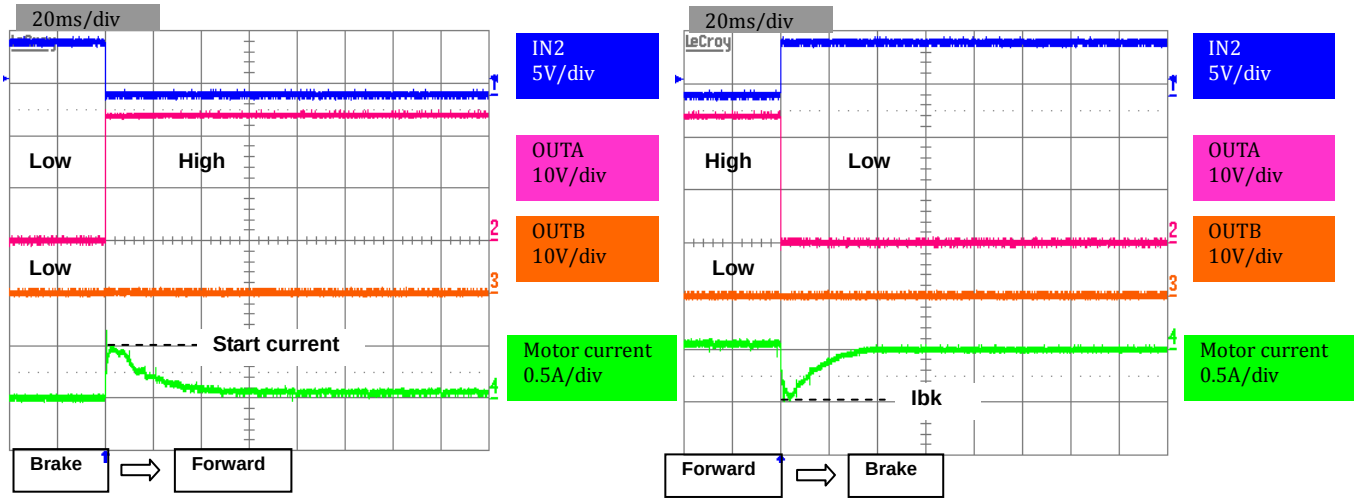
Figure 19. Forward ↔ Output Off switching
DC_motor load, PS=High, IN2=Low
Vcc=VREF=5V, VM=24V, RNF=GND



DC motor starts operation, high current flows. However, as the motor rotation continues, the current is reduced due to the back electromotive force generated in the motor.
Given that the motor supply voltage is Vm, the back electromotive force of the motor is EMF, and the coil resistance is Ra, the motor current is obtained as follows:

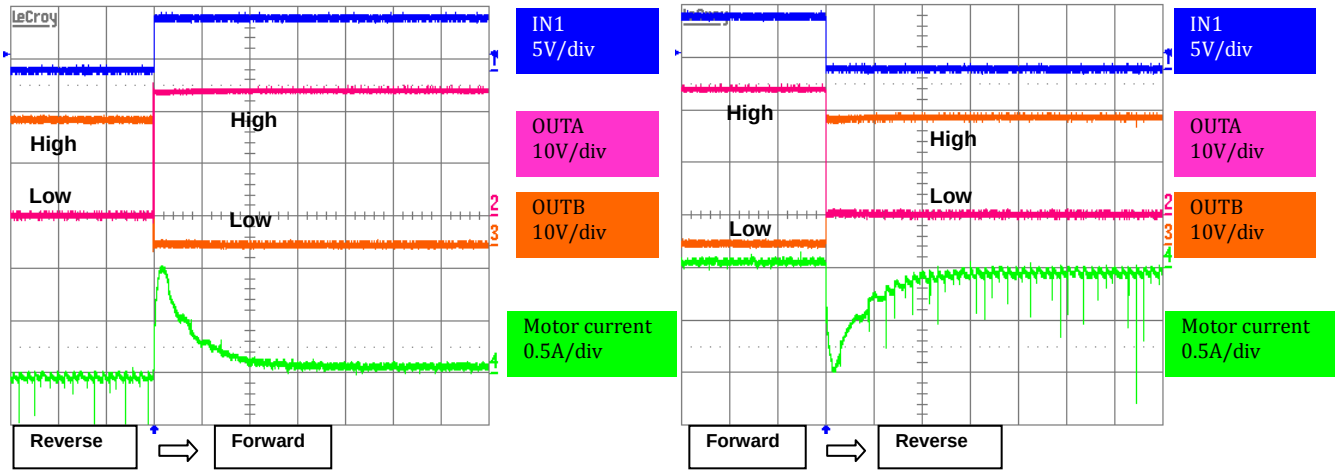
$$Im = (Vm-EMF)/Ra$$

Figure 20. Forward ↔ Brake switching
DC_motor load, PS=High, IN1=High
Vcc=VREF=5V, VM=24V, RNF=GND



You can put a brake on the DC motor by turning on both of the lower FETs of the H-Bridge while the motor is under rotation.
Here, the brake current Ibk = EMF/Ra flows against, which is generated from the EMF occurred during motor rotation.

Figure 21. Forward ↔ Reverse switching
IN1 and IN2 are input by the reversed phase
DC_motor load, PS=High
Vcc=VREF=5V, VM=24V, RNF=GND



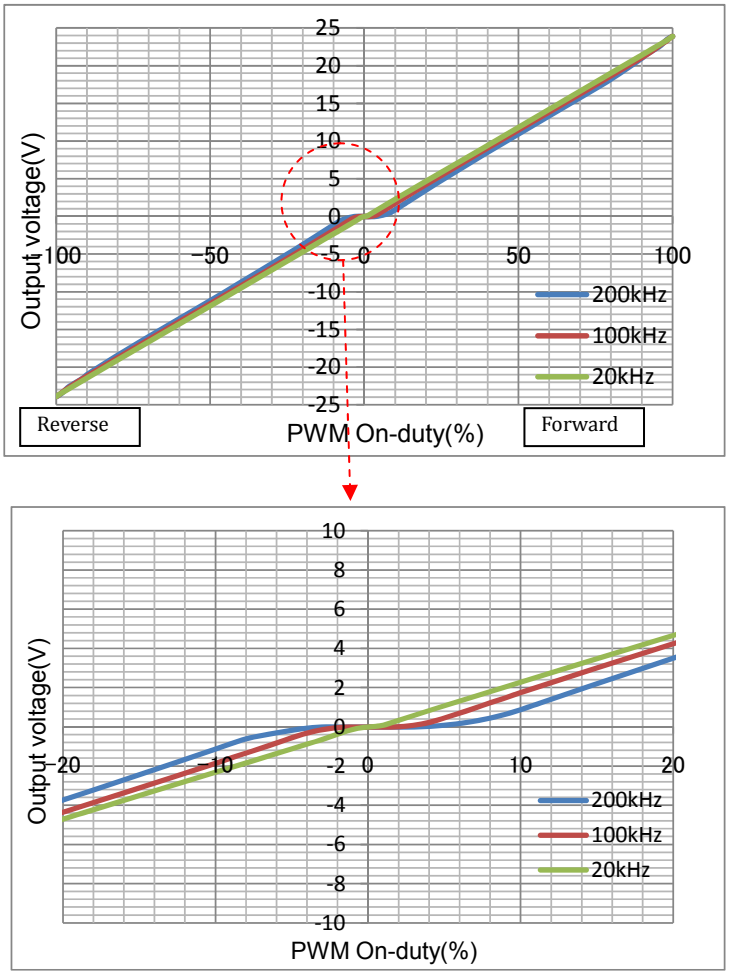
When the counterpart FET is turned on while the DC motor is under rotation, rotation will change rapidly because the rotation direction is switched. Since Vm voltage is powered reversely in addition to the EMF, reverse current Irev = (EMF+Vm)/Ra flows against the opposite direction.

Since reverse current Irev is about double the startup current, the current may exceed the ratings depends on applied loads. Hence, it is recommended to set brake mode when you switch the rotational direction of motors.

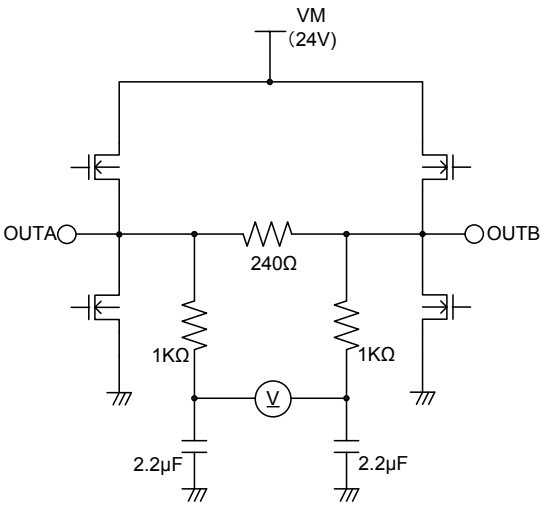
3. PWM (Pulse Width Modulation) control

LV8760T/LV8761V can perform H-Bridge direct PWM control to IN1, and IN2 by inputting PWM signal. The maximum frequency of PWM signal is 200 kHz. However, dead zone is generated when On-Duty is around 0%. Make sure to select optimum PWM frequency according to the target control range.

Figure 22. Input-Output Characteristics of H-Bridge(Reference data)
Forward/Reverse ↔ Brake
Vcc=5V,VM=24V,VREF=1.5V



Measurement connection diagram



4. Current Limit control

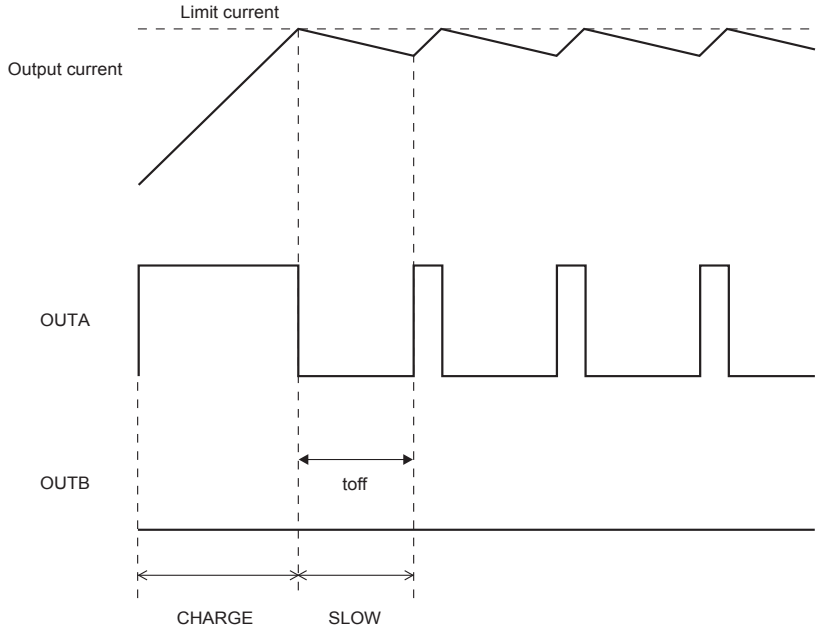


Figure 23. Current limit control timing chart

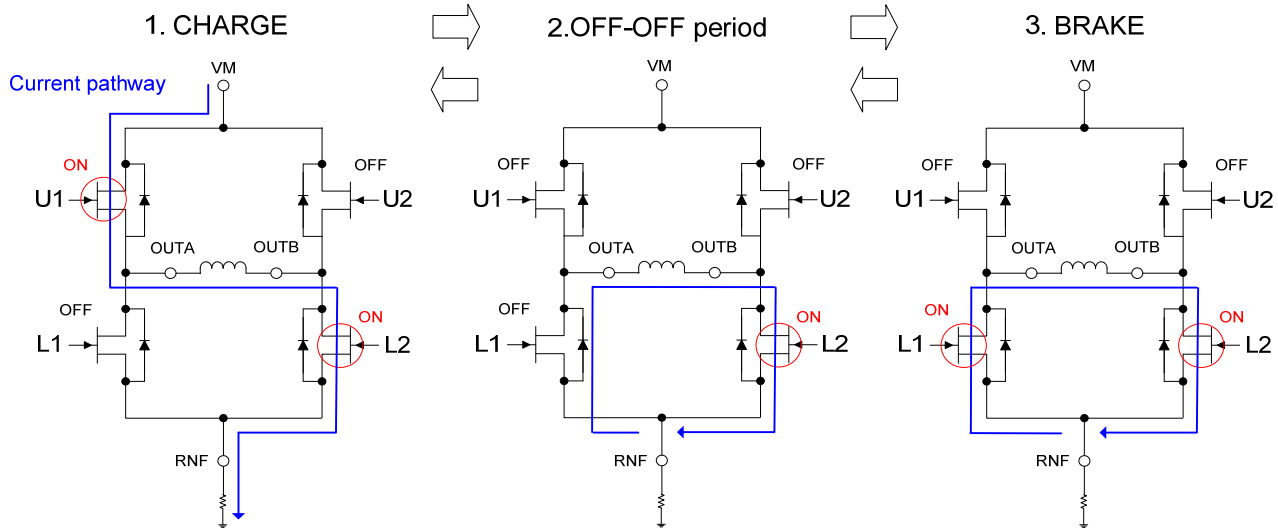


Figure 24. Output transistor operation sequence

Output FET control function

IN1 = High, IN2 = Low (Forward)

Output control input	CHARGE	BRAKE
U1	ON	OFF
U2	OFF	OFF
L1	OFF	ON
L2	ON	ON

IN1 = Low, IN2 = High (Reverse)

Output control input	CHARGE	BRAKE
U1	OFF	OFF
U2	ON	OFF
L1	ON	ON
L2	OFF	ON

5. Setting the current limit value

Current limit control is feasible by connecting current sensing resistor between RNF and GND and powering reference voltage to VREF.

The current limit value is determined by the following formula:

Ilimit [A] = (VREF [V] /5) /RNF [Ω])

Given that VREF = 1.5V, RNF = 0.22Ω, the current limit is obtained as follows:

Ilimit = 1.5V/5/0.22Ω = 1.36A

When output current reaches to the current limit setting value, current control is performed by chopping output FET as Figure 24 shows: 1→2→3→2→1→…
After the chopping drive, when the mode switches from CHARGE to Brake mode, the upper and the lower FET are turned off to prevent penetration current. The off period is set between 200 and 300nsec. During off period, the current is regenerated through parasitic diode generated between drain and source of the FET because the lower FET (L1 side) is off.

6. Setting the Braking time

Braking operation time can be set by connecting a capacitor between SCP and GND pins.
The value of the capacitor can be determined by the following formula:

Timer latch-up: Tscp

$Tscp \approx C \times Vthscp / Iscp$ [sec]

Vthscp: Comparator threshold voltage (1V typical)
Iscp: SCP charge current (5μA typical)

When a capacitor with a capacitance of 100pF is connected across the SCP and GND pins, for example, Tscp is calculated as follows:

$Tscp = 100pF \times 1V/5\mu A = 20\mu s$

This setting is the same as the following time setting required to turn off the outputs when an output short-circuit occurs as explained in the section entitled "Output Short-circuit Protection Function."

7. Blanking time

If, when exercising PWM current control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in false over current detection. To prevent this false detection, a blanking time is provided to prevent the noise occurring during mode switching from being received. During this time, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.

The blanking time, tBLANK (μs),is approximately

tBLANK≈2μs

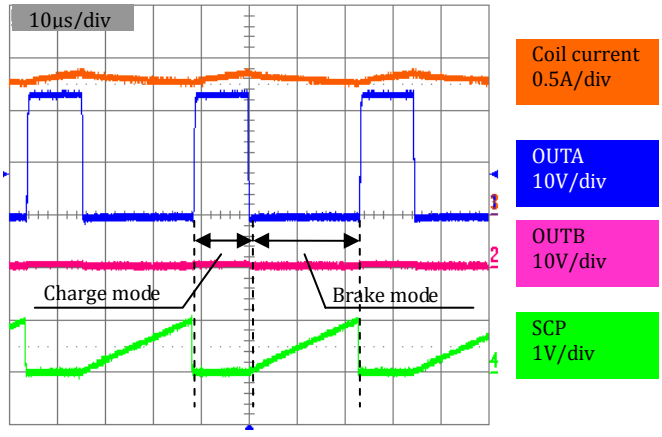


Figure 25. Current limit operation
Vcc=5V,VM=24V,VREF=1.5V
RNF=0.22Ω,SCP=105pF

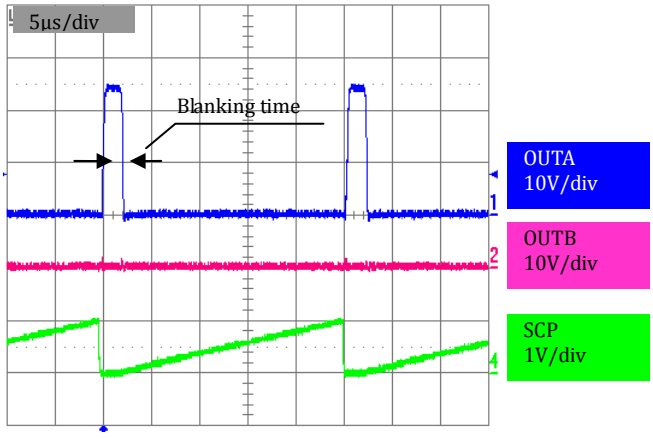
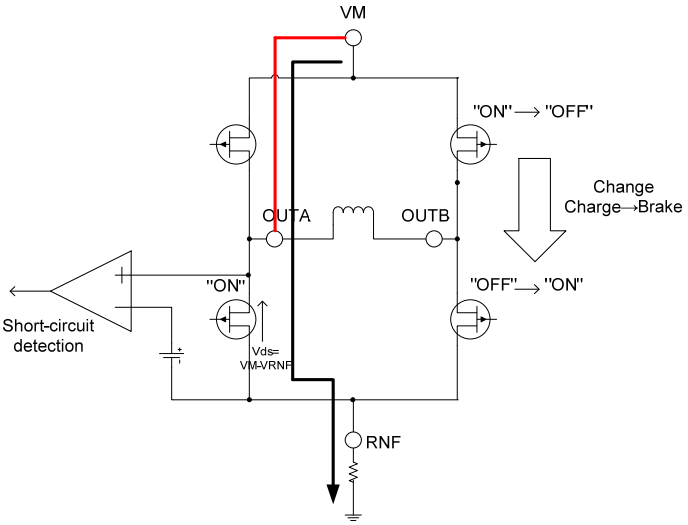


Figure 26. Blanking time
Vcc=5V,VM=24V,VREF=1.5V
RNF=0.4V,SCP=105pF

Output short-circuit protection function

The LV8760T/LV8761V incorporates an output short-circuit protection circuit that turns off the output to prevent the IC from fatal damage when the output is short-circuited due to short-to-power or short-to-ground fault.

1. Short-circuit state detection operation

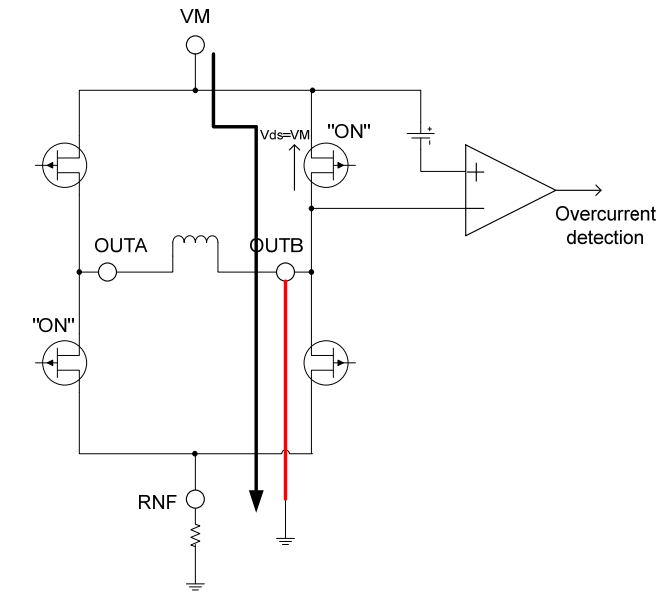


VM-Output pin short

High current flows as follows:

VM power supply→ lower FET→ RNF resistor.

When the voltage of RNF becomes high, the mode switches from Charge to Brake. However since the lower FET is on, comparison is performed to the Vds of the lower FET and short detection reference voltage. As a result, protector circuit operates and the output is turned off.

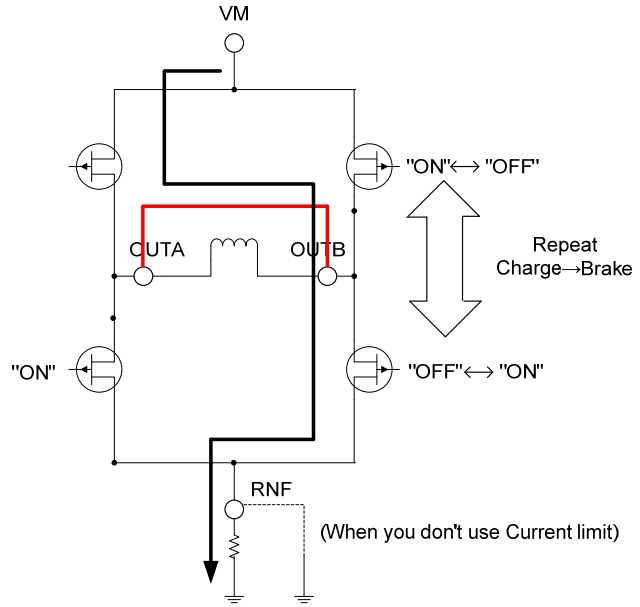


Output pin-GND short

High current flows as follows:

The upper FET → GND

After the Vds of the upper FET and short detection reference voltage is compared.
As a result, protector circuit operates and the output is turned off.



Output pin-Output pin short

High current flows as follows:
VM power supply→ the upper FET→ the lower FET→RNF resistor.
When the voltage of RNF becomes high, the mode switches from Charge to Brake. Therefore, the flow of the current is stopped and short state is not detected. After the Brake mode is over, the upper FET turns on again and high current flows, but brake is set immediately. Since such operation is repeated, short state is not detected.
Without use of current limit function (RNF-GND short), since the mode is not switched to brake with high current, short state is detected and the output is turned off by protector circuit.

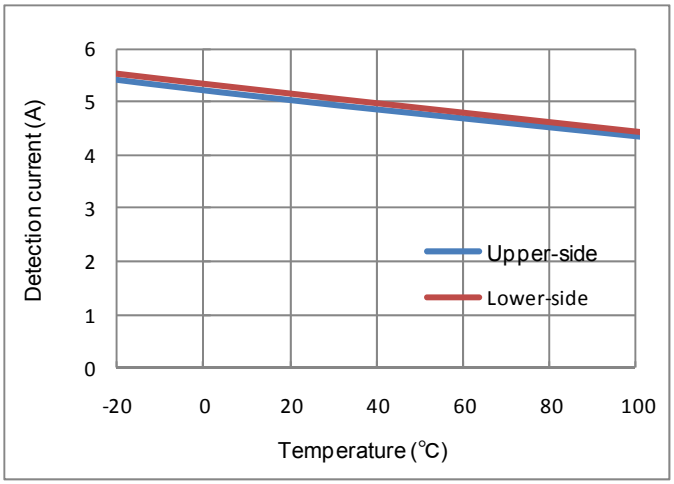
2. Output short-circuit protection detect current

Short protector operates when abnormal current flows into the output transistor.
However, please note that there is a temperature property in the detection current.

Ta = 25°C (typ), RNF-GND short (Reference value)

Output FET	LV8760T/LV8761V
Upper-side FET	5A
Lower-side FET	5A

Figure 27. Detection Current vs Temperature (Reference data)



3. Short-circuit Protection Mode

There are 2 operation modes for short protector circuit: 1. [Latch-type] latches output off state. 2. [Auto reset-type] repeats on/ off of output. LV8760T includes Latch-type only. LV8761V includes selectable Latch-type and Auto reset-type.

	Control Pin	Short-circuit Protection Mode
LV8760T	—	Latch type (fix)
LV8761V	EMM (36pin) = Low	Latch type
	EMM (36pin) = High	Auto reset type

4. Latch-type (LV8760T/LV8761V common)

The short-circuit protection circuit is activated when it detects the output short-circuit state. If the short-circuit state continues for the internally preset period (≈ 4μs), the protection circuit turns off the output from which the short-circuit state has been detected. Then it turns the output on again after a lapse of the timer latch time described later. If the short-circuit state is still detected, it changes all the outputs to the standby mode and retains the state. The latched state is released by setting the PS to L.

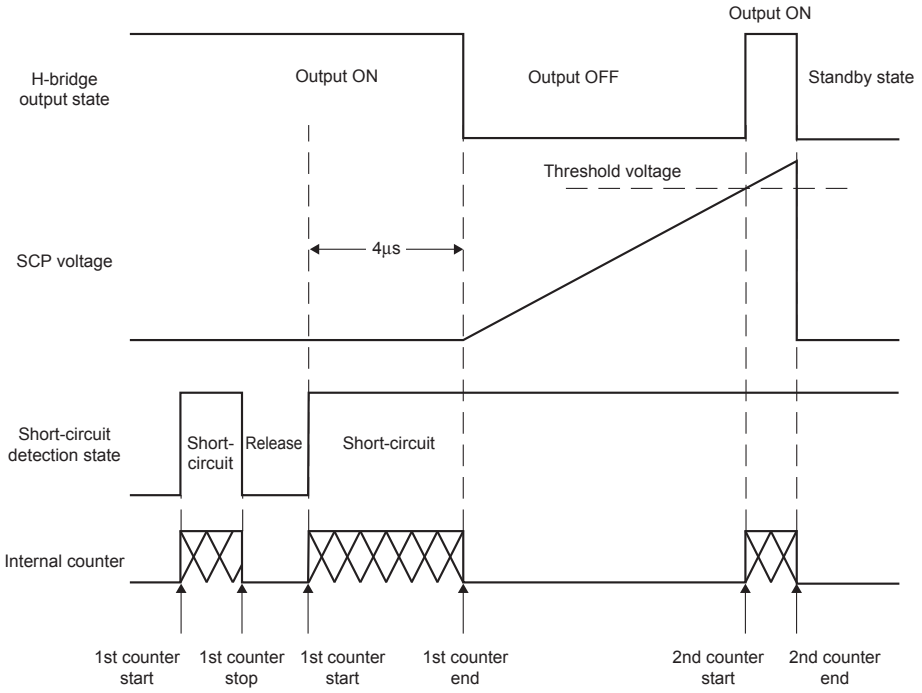


Figure 28. Short-circuit protection Latch-type timing chart

5. How to set the SCP pin constant (timer latch-up setting)

The user can set the time at which the outputs are turned off when short-circuit occurs by connecting a capacitor across the SCP and GND pins. The value of the capacitor can be determined by the following formula:

Timer latch-up: Tscp $Tscp \approx C \times Vthscp/Iscp$ [sec]

Vthscp: Comparator threshold voltage (1V typical)

Iscp: SCP charge current (5μA typical)

When a capacitor with a capacitance of 100pF is connected across the SCP and GND pins, for example, Tscp is calculated as follows:

$Tscp = 100pF \times 1V/5\mu A = 20\mu s$

6. Auto Reset Type (LV8761V only)

In LV8761V, short circuit protection mode becomes Auto reset type at EMM = high.
The sequences up to the detection of an output short-circuit state are identical to those which are explained in Section 1, "Protection Function Operation (Latch Type).
After output is turned off on detection of an output short-circuit condition, the internal counter starts counting and repeats turning on and off the output as shown in the figure below.
This state continues until the over current state is eliminated.

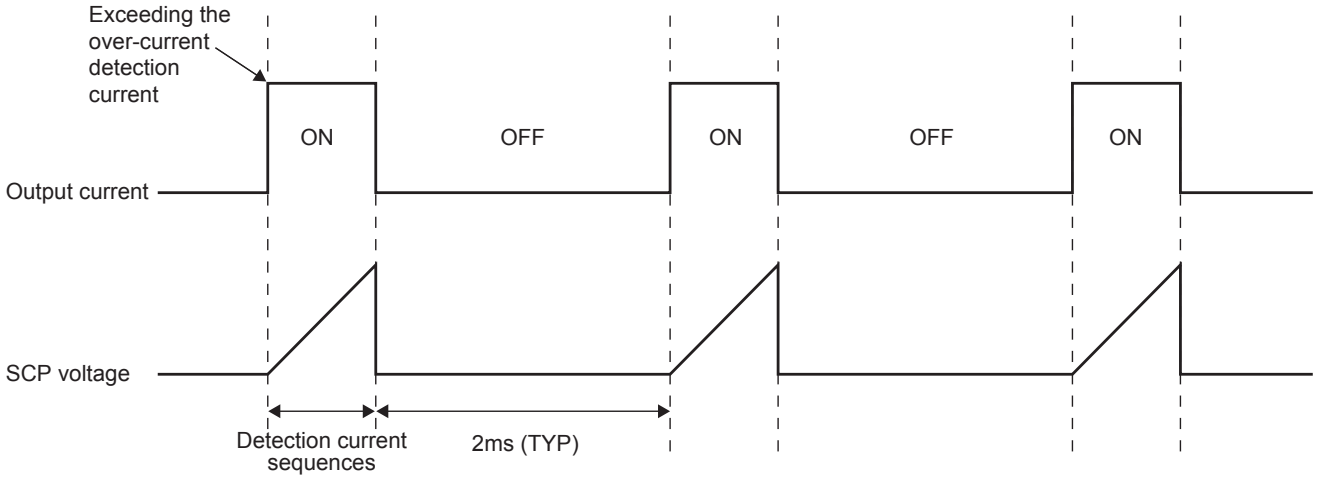


Figure 29. Short-circuit protection Auto Reset type timing char

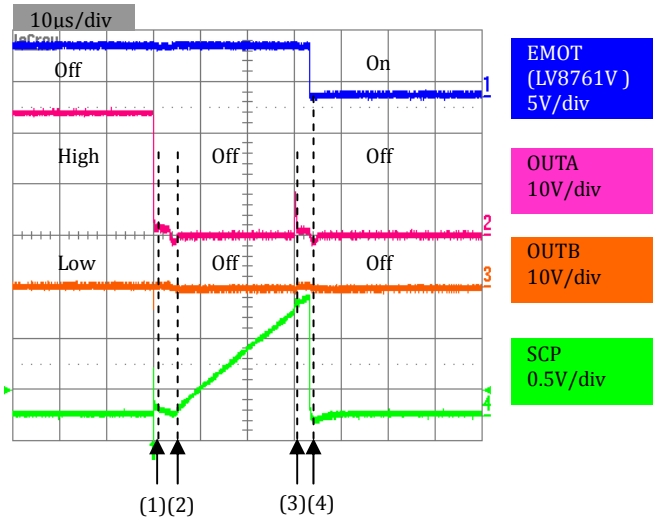
7. Unusual Condition Warning Output Pin: EMOT (LV8761V only)

The LV8761V is provided with the EMOT pin which notifies the CPU of an unusual condition if the protection circuit operates by detecting an abnormal condition of the IC. This pin is of the open-drain output type and requires a pull-up resistor when to be used.
The EMOT pin is placed in the ON state when one of the following conditions occurs.

1. Shorting-to-power or shorting-to-ground occurs at the output pin and the output short-circuit protection circuit is activated.
2. The IC junction temperature rises and the thermal protection circuit is activated.

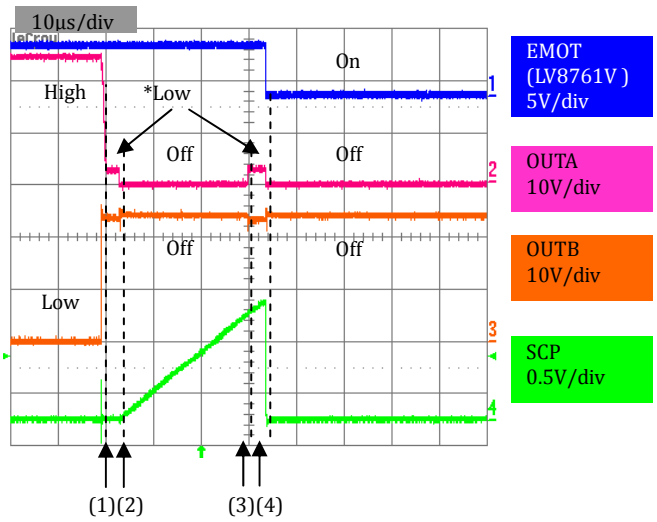
The EMOT pin is set to the OFF state when the relevant protection operation is eliminated.

Figure 30. Short-circuit Protection(Latch-type)
OUTA-GND short
Vcc=5V,VM=24V,RNF=0.22Ω,SCP=105pF
PS=High,IN1=High,IN2=Low



(1) OUTA-GND short.
(2) Short-circuit state detection.
The output is turned off.
(3) The output is turned on again.
(4) The output off state is latched.
Warning Output (EMOT) is turned on.

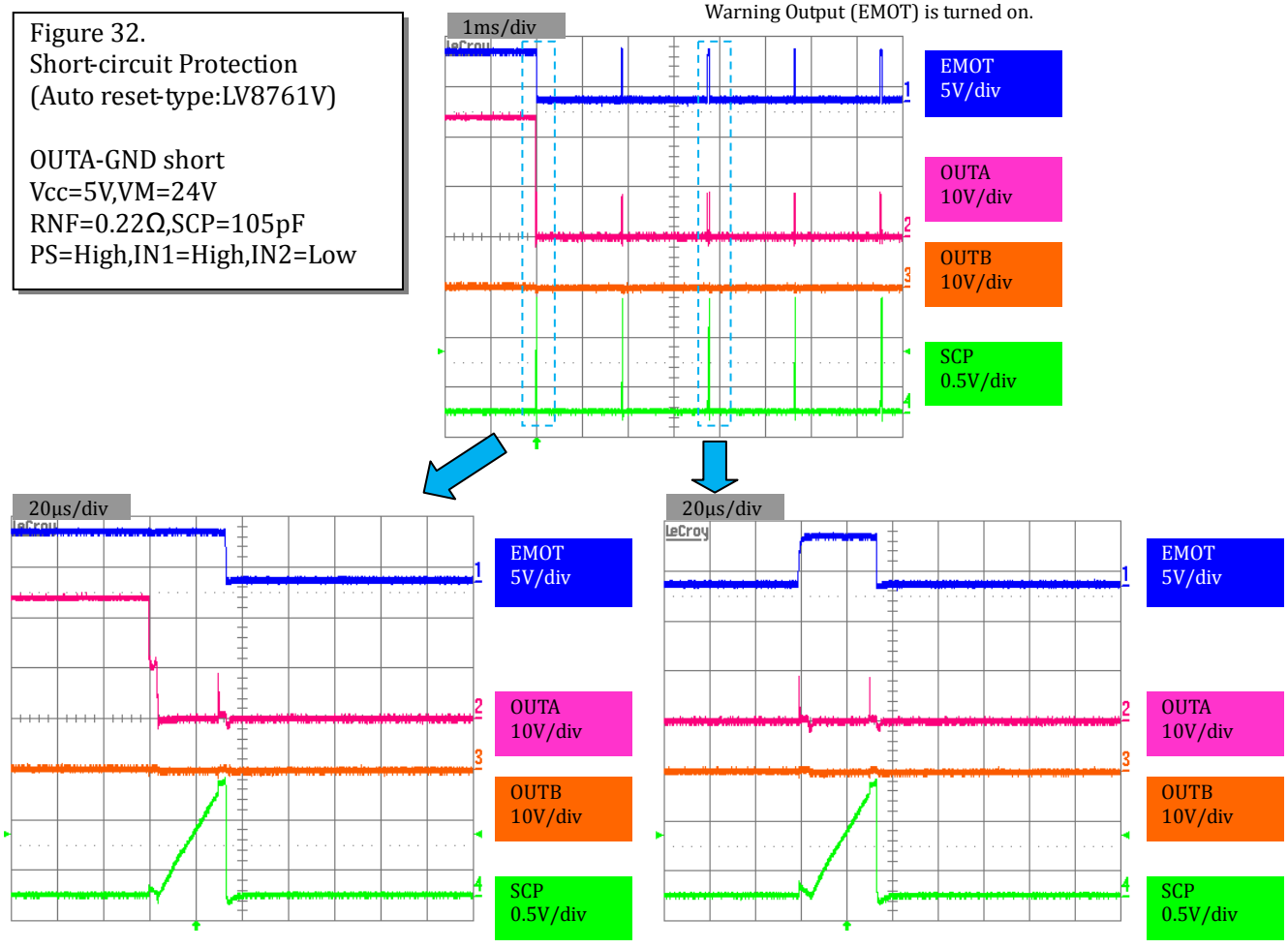
Figure 31. Short-circuit Protection(Latch-type)
OUTB-VM short
Vcc=5V,VM=24V,RNF=0.22Ω,SCP=105pF
PS=High,IN1=High,IN2=Low



(1) OUTB-VM short.
*The voltage increases as a result of current to RNF resistor. Consequently the mode shifts from charge to brake mode. Therefore, OUTA=Low.
(2) Short-circuit state detection.
The output is turned off.
(3) The output is turned on again.
(4) The output off state is latched.
Warning Output (EMOT) is turned on.

Figure 32.
Short-circuit Protection
(Auto reset-type:LV8761V)

OUTA-GND short
Vcc=5V,VM=24V
RNF=0.22Ω,SCP=105pF
PS=High,IN1=High,IN2=Low



Charge Pump Circuit

When the PS pin is set High, the charge pump circuit operates and the VG pin voltage is boosted from the VM voltage to the VM + REG5 voltage. If the VG pin voltage is not boosted sufficiently, the output cannot be controlled, so be sure to provide a wait time of tONG or more after setting the PS pin High before starting to drive the motor.

.

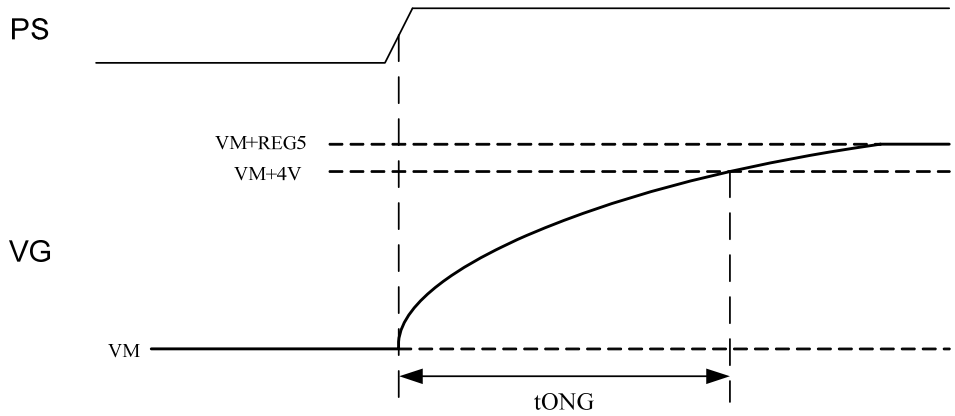


Figure 33. Charge Pump circuit timing char

VG voltage is used to drive upper output FET and REG5 voltage is used to drive lower output FET.
Since VG voltage is equivalent to the addition of VM and REG5 voltage, VG capacitor should allow higher voltage.
The capacitor between CP1 and CP2 is used to boost charge pump. Since CP1 oscillates with 0V↔REG5 and CP2 with VM↔VM+REG5, make sure to allow enough capacitance between CP1 and CP2.
Since the capacitance is variable depends on motor types and driving methods, please check with your application before you define constant to avoid ripple on VG voltage.

(Recommended value) VG: 0.1μF
CP1-CP2: 0.1μF

Figure 34. Charge Pump Operation
Oscillation frequency
Vcc=5V,VM=24V
PS=High
CP1-CP2=0.1μF
VG=0.1μF

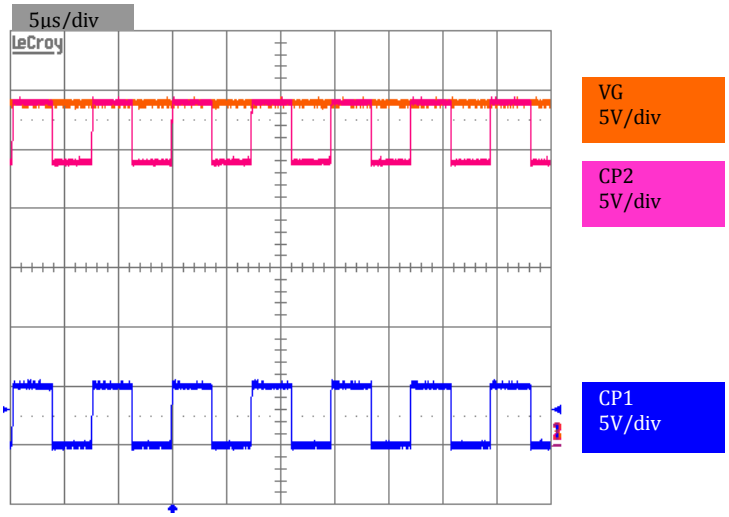


Figure 35.Charge Pump Operation
tONG
Vcc=5V,VM=24V
PS=High
CP1-CP2=0.1μF
VG=0.1μF

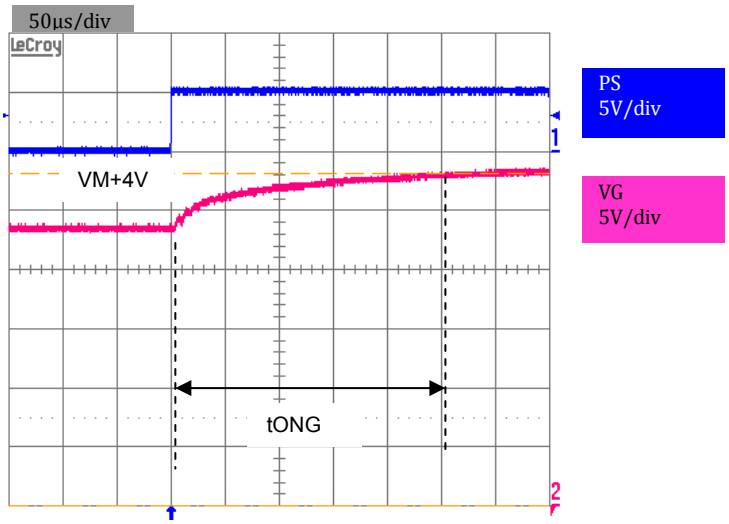
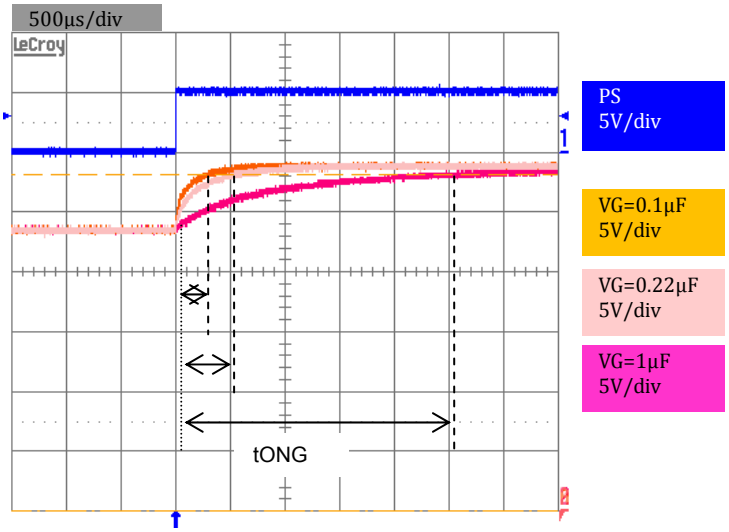


Figure 36.Startup time with different VG capacitor
Vcc=5V,VM=24V
PS=High
CP1-CP2=0.1μF
VG=0.1μF/0.22μF/1μF



Thermal shutdown function

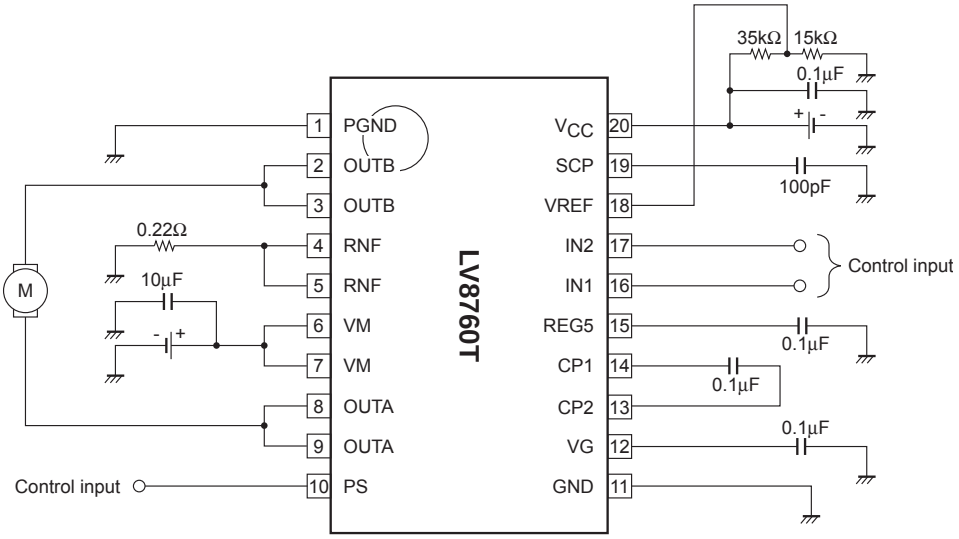
The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds 180°C and the abnormal state warning output is turned on (The warning output function is only LV8761V). As the temperature falls by hysteresis, the output turned on again (automatic restoration). The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax=150°C.

TSD = 170°C (typ)
ΔTSD = 40°C (typ)

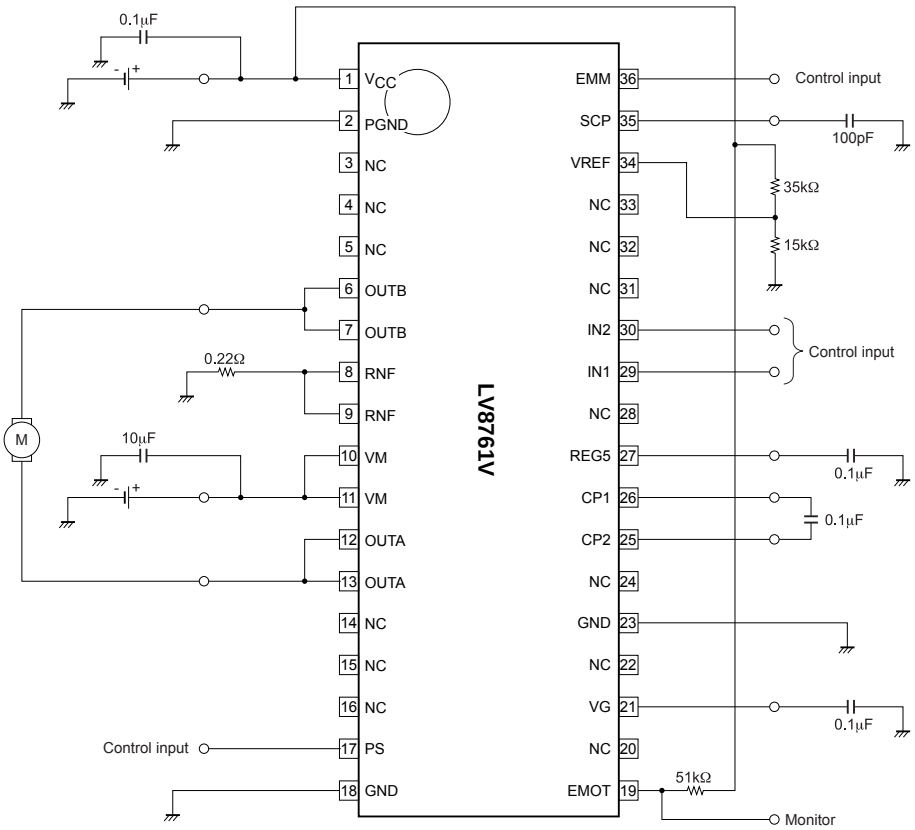
Application Circuit Example

1. When you use the current limit function

<LV8760T>



<LV8761V>



Setting the current limit value

When V_{CC} = 5V,

Vref = 1.5V

Ilimit = Vref/5/RNF

= 1.5V/5/0.22Ω = 1.36A

Setting the current limit regeneration time and short-circuit detection time

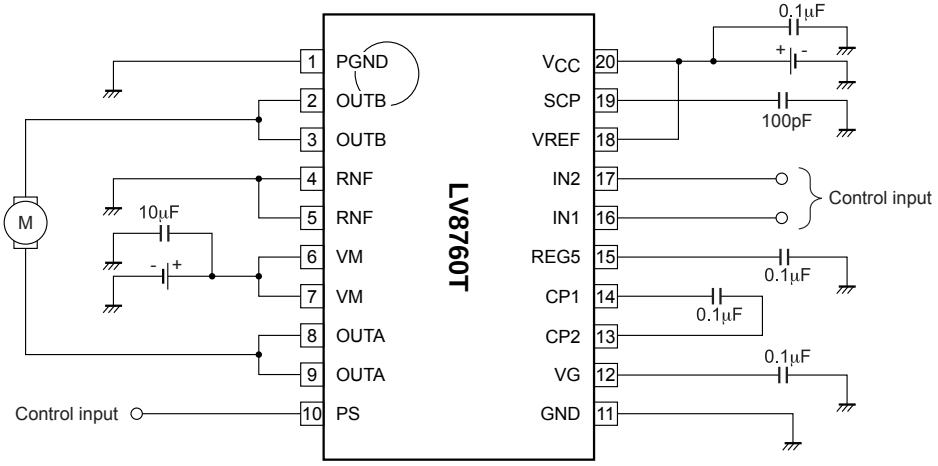
Tscp ≈ C × Vthscp/Iscp

= 100pF × 1V/5μA

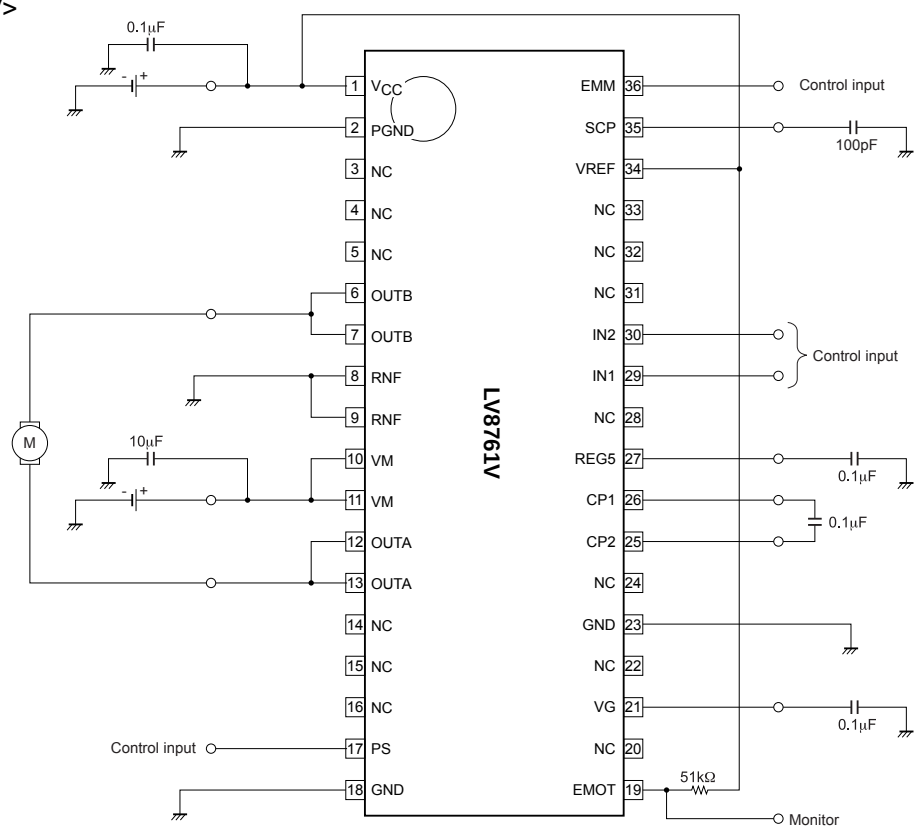
= 20μs

2. When you do not use the current limit function

<LV8760T>



<LV8761V>



Setting at short-circuit state detection time

Tscp ≈ C × Vthscp/Iscp

= 100pF·1V/5μA

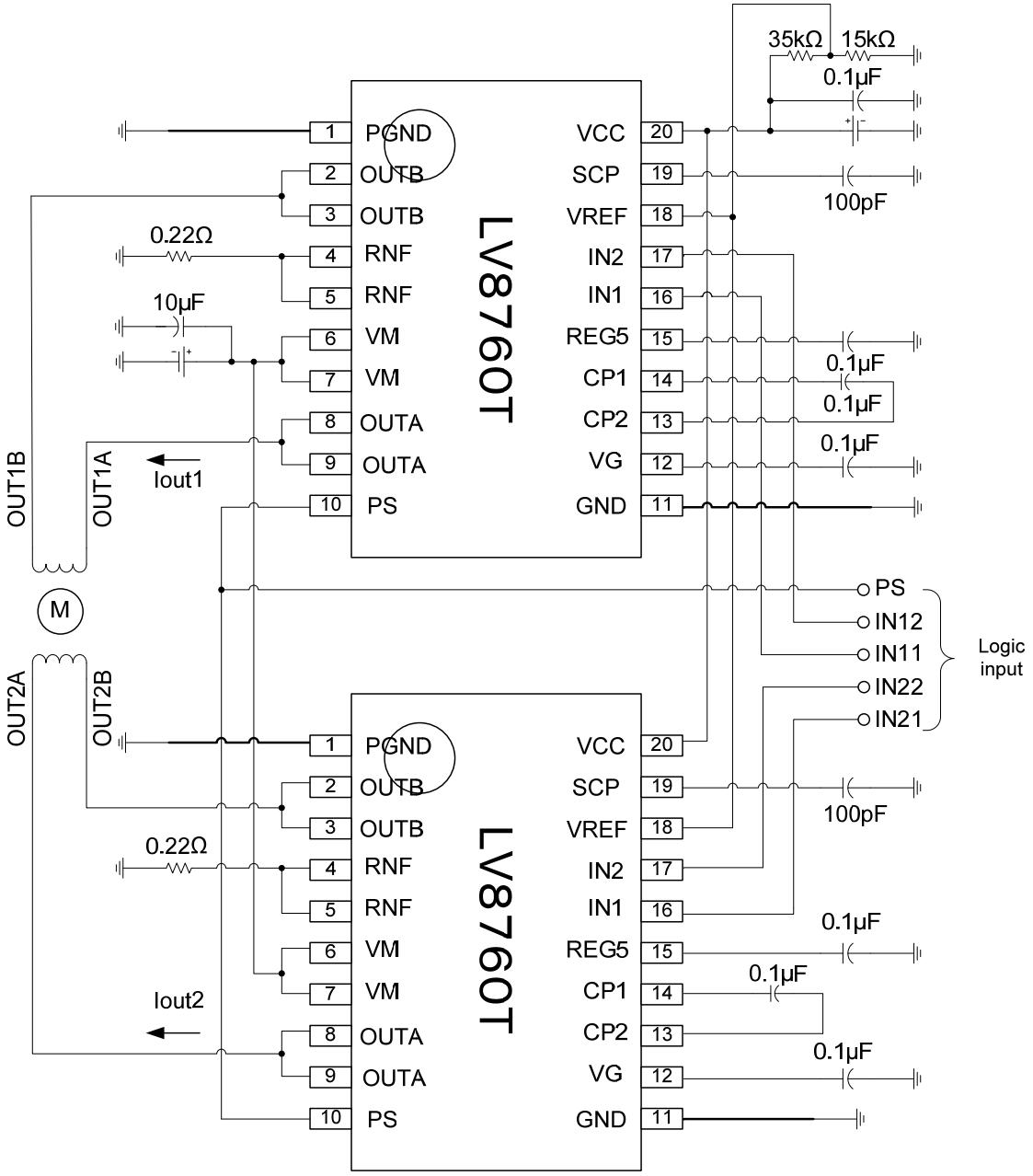
= 20μs

*Do the following processing when you do not use the current limit function.

- It is short between RNF-GND.
- The pin VREF is hung on suitable potential of V_{CC} or lower.

3. Stepping motor drive application

<LV8760T>



Note: LV8761V is similar.

Setting the constant current value

When V_{CC} = 5V,

Vref = 1.5V

Iout = Vref/5/RNF

= 1.5V/5/0.22Ω = 1.36A

Setting at slow-decay time of constant current control and short-circuit detection time

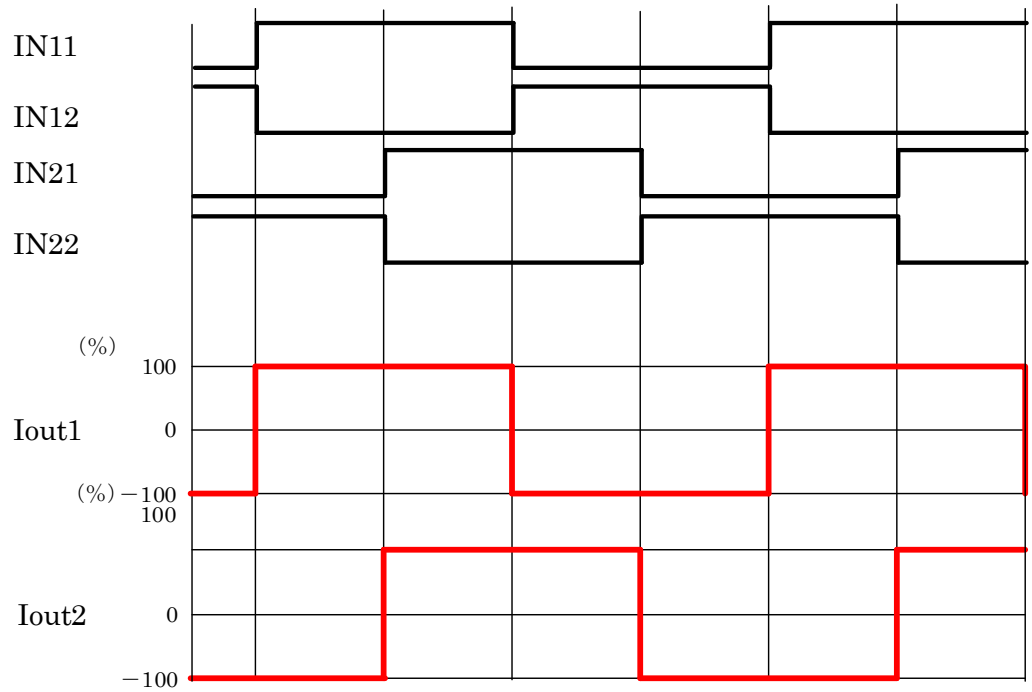
Tscp ≈ C × Vthscp/Iscp

= 100pF × 1V/5μA

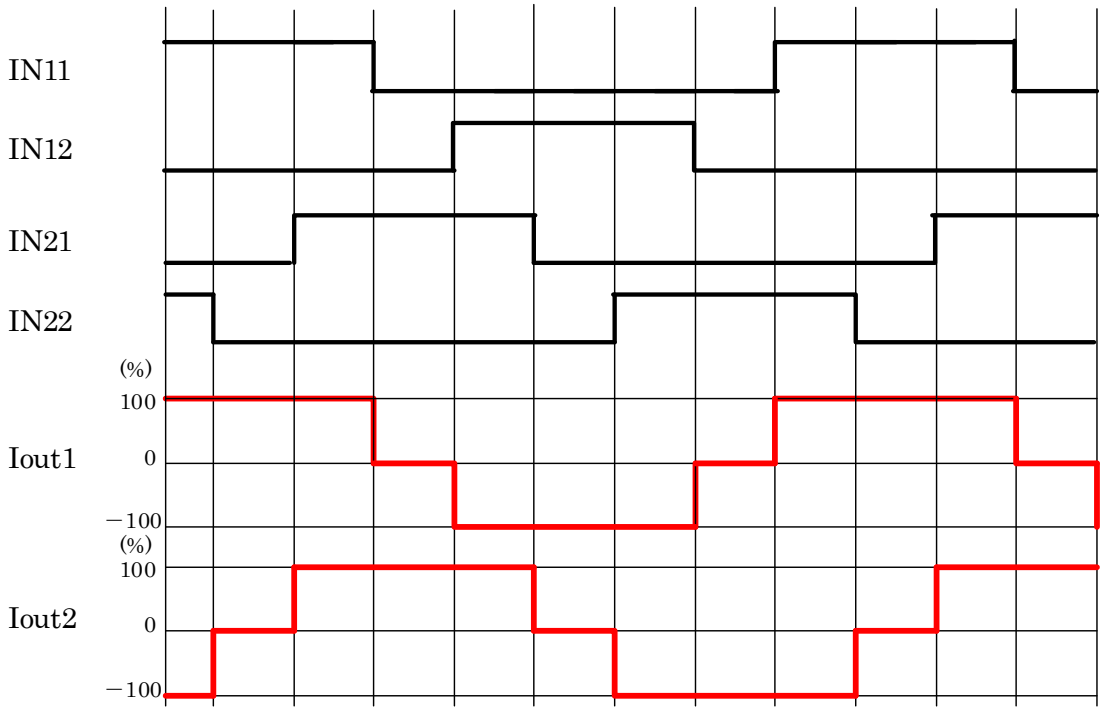
= 20μs

4. Input example of Stepping motor drive application

Full-step excitation control



Half-step excitation control

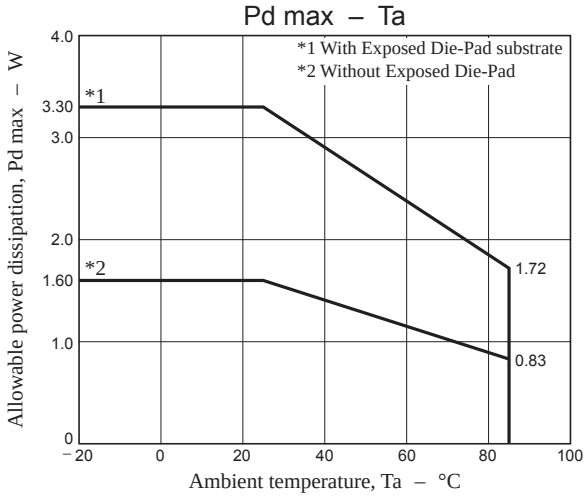


Allowable power dissipation

The pad on the backside of the IC functions as heatsink by soldering with the board. Since the heat-sink characteristics vary depends on board type, wiring and soldering, please perform evaluation with your board for confirmation.

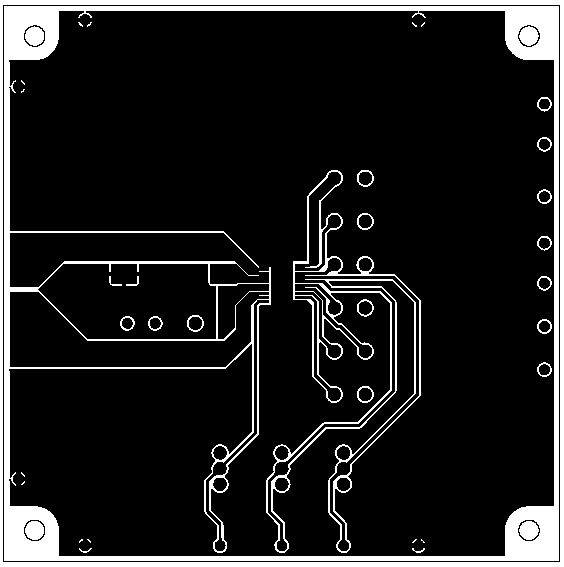
The following Pd-Ta chart is based on the measurement result using ON semi's evaluation board and the ICs.

<LV8760T>

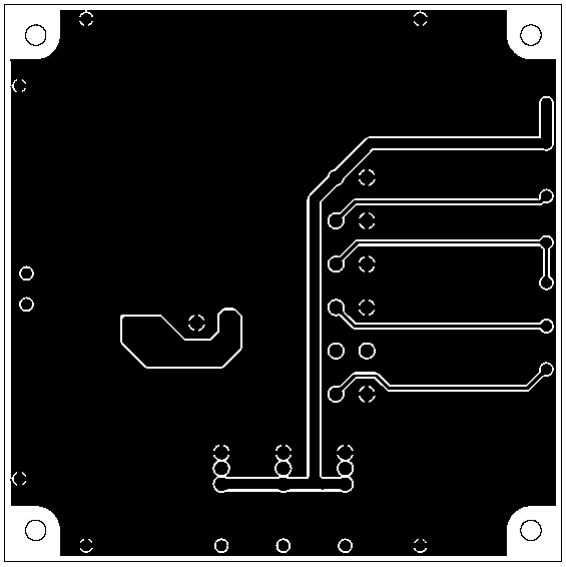


Substrate Specifications (Substrate recommended for operation of LV8760T)

Size	: 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material	: Glass epoxy
Copper wiring density	: L1 = 95% / L2 = 95%

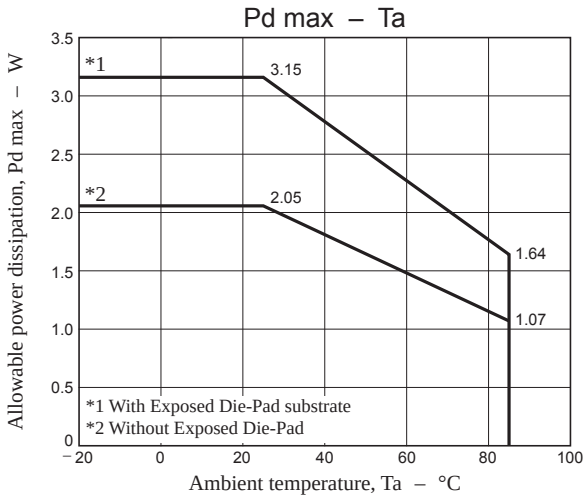


L1 : Copper wiring pattern diagram



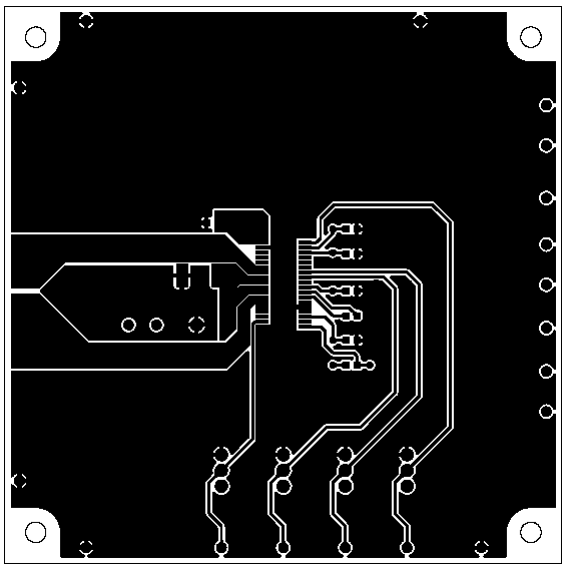
L2 : Copper wiring pattern diagram

<LV8761V>

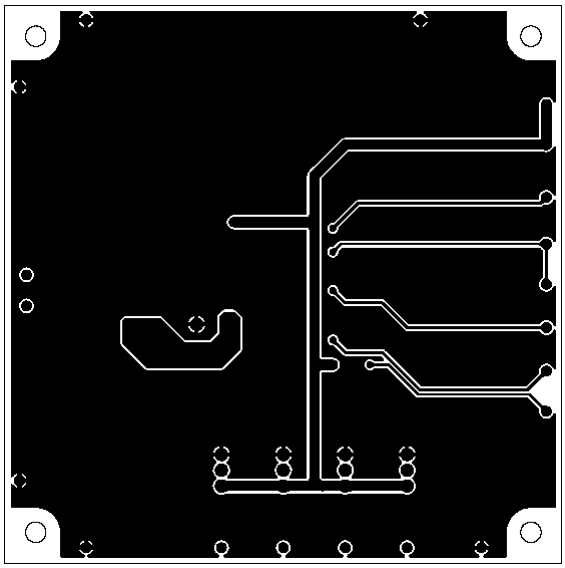


Substrate Specifications (Substrate recommended for operation of LV8761T)

Size	: 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material	: Glass epoxy
Copper wiring density	: L1 = 95% / L2 = 95%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

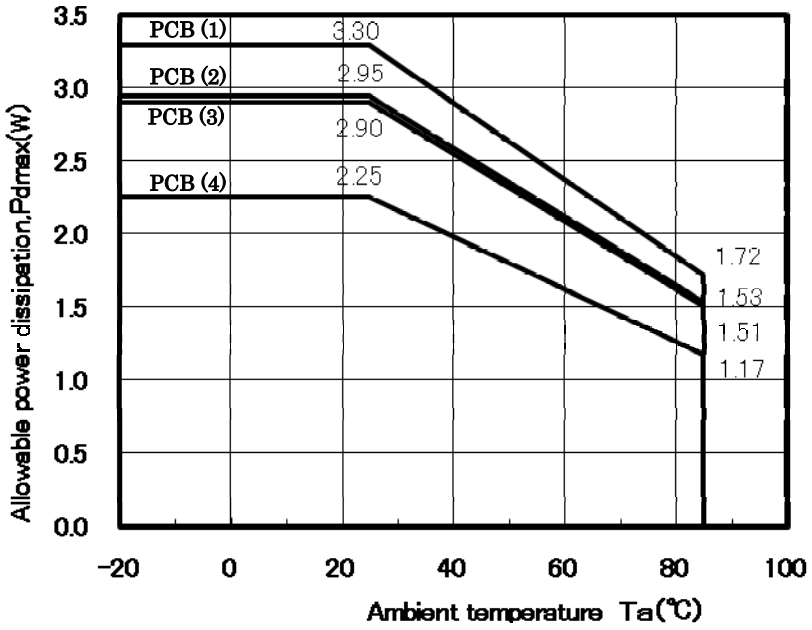
Cautions (LV8760T/LV8761V common)

1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below:
(1)Maximum value 80% or lower for the voltage rating
(2)Maximum value 80% or lower for the current rating
(3)Maximum value 80% or lower for the temperature rating

3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

LV8760T's Allowable power dissipation in each PCB size (Reference value)

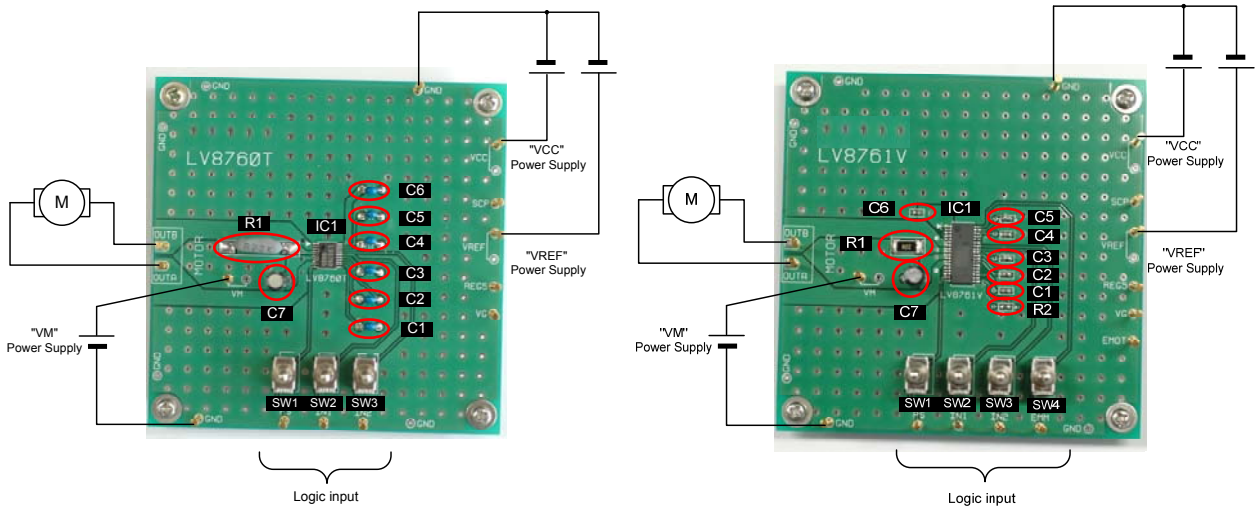


PCB SIZE
(1) 90mm × 90mm × 1.6mm (two-layer substrate [2S0P] with backside mounting)
(2) 70mm × 70mm × 1.6mm (two-layer substrate [2S0P] with backside mounting)
(3) 60mm × 60mm × 1.6mm (two-layer substrate [2S0P] with backside mounting)
(4) 40mm × 40mm × 1.6mm (two-layer substrate [2S0P] with backside mounting)

The above chart shows the relation between Pdmax and PCB size.
PCB (1) provides the reference value based on ON semi's evaluation board of LV8760T. Above Pdmax values are obtained from the boards which are shrunk accordingly as stated above, where IC mounting position is the center. Pdmax may fluctuate depending on board layout.

Evaluation board

1. Completed PCB with Devices

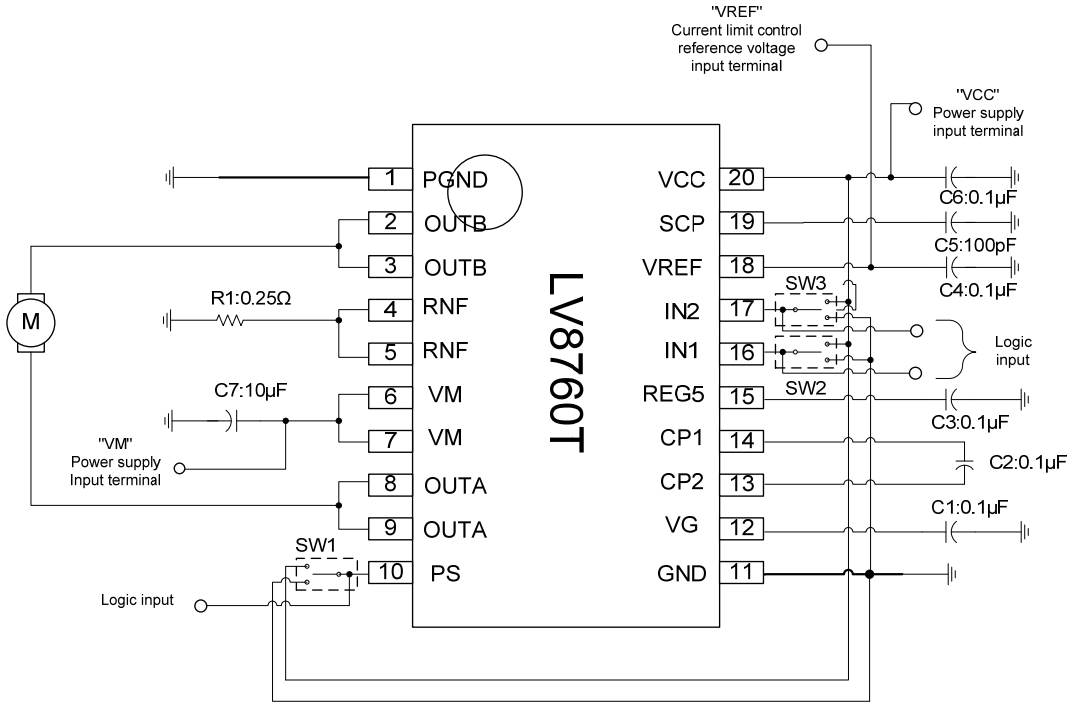


2. Bill of Materials for LV8760T and LV8761V Evaluation Board

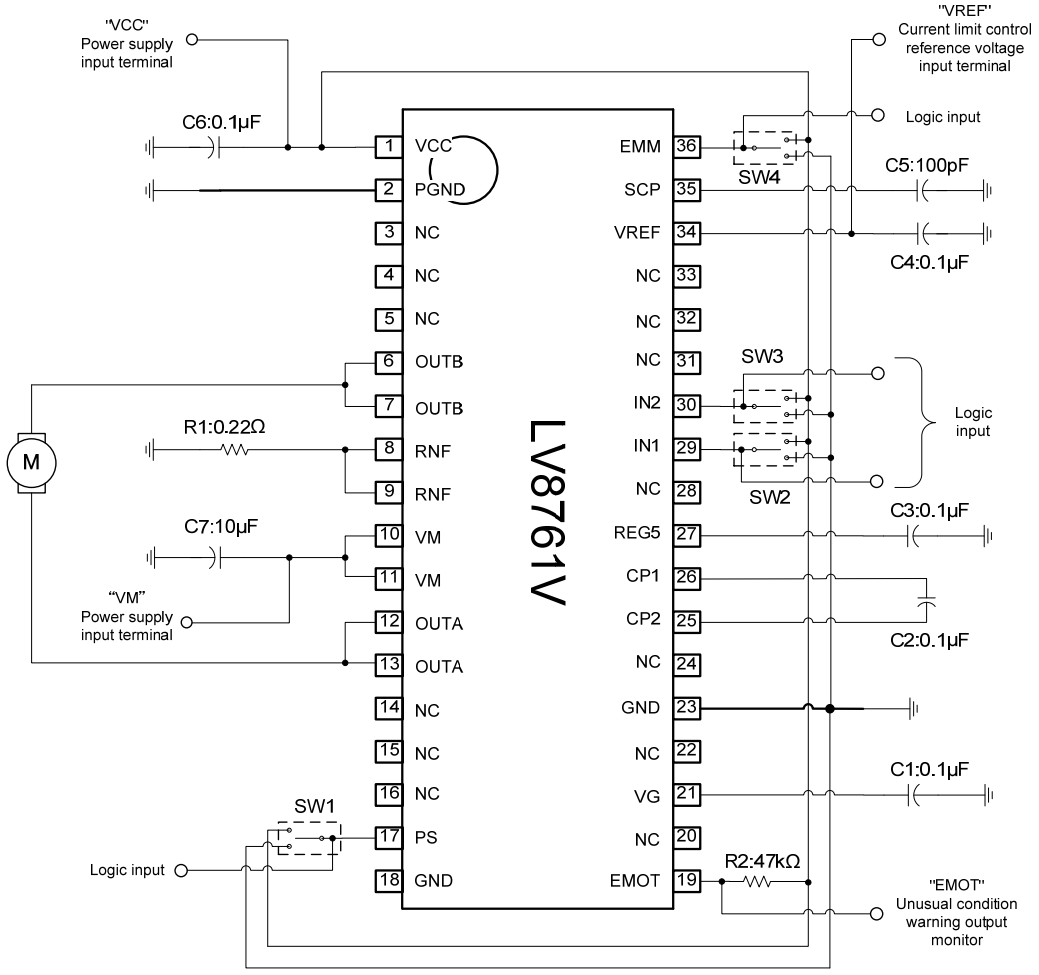
Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free	Adjustment product
C1	1	Capacitor for Charge pump	0.1µF, 50V	±10%		TDK	FK28X7R1H104K	Yes	Yes	LV8760T
	1		0.1µF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes	LV8761V
C2	1	Capacitor for Charge pump	0.1µF, 50V	±10%		TDK	FK28X7R1H104K	Yes	Yes	LV8760T
	1		0.1µF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes	LV8761V
C3	1	REG5-out stabilization Capacitor	0.1µF, 50V	±10%		TDK	FK28X7R1H104K	Yes	Yes	LV8760T
	1		0.1µF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes	LV8761V
C4	1	VREF stabilization Capacitor	0.1µF, 50V	±10%		TDK	FK28X7R1H104K	Yes	Yes	LV8760T
	1		0.1µF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes	LV8761V
C5	1	Capacitor to set SCP timer	100pF, 50V	±5%		TDK	FK28COG1H101J	Yes	Yes	LV8760T
	1		100pF, 50V	±5%		Murata	GRM1882C1H101JA01*	Yes	Yes	LV8761V
C6	1	VCC Bypass Capacitor	0.1µF, 50V	±10%		TDK	FK28X7R1H104K	Yes	Yes	LV8760T
	1		0.1µF, 100V	±10%		Murata	GRM188R72A104KA35*	Yes	Yes	LV8761V
C7	1	VM Bypass Capacitor	10µF, 50V	±20%		SUN Electronic Industries	50ME10HC	Yes	Yes	LV8760T LV8761V
R1	1	Output current detective Resistor	0.22Ω, 2W	±5%		JAPAN RESISTOR MFG	KNP2WR22J/R0	Yes	Yes	LV8760T
	1		0.22Ω, 1W	±5%		ROHM	MCR100JZHJLR22	Yes	Yes	LV8761V
R2	1	Pull-up Resistor for pin EMOT	47kΩ, 1/10W	±5%		KOA	RK73B1JT**473J	Yes	Yes	LV8761V
IC1	1	Motor Driver			TSSOP20 J(225mil)	ON Semiconductor	LV8760T	No	Yes	LV8760T
	1				SSOP36J (275mil)		LV8761V	No	Yes	LV8761V
SW1-SW3	3	Switch				MIYAMA ELECTRIC	MS-621C-A01	Yes	Yes	LV8760T
SW1-SW4	4									LV8761V
TP1-TP13	13	Test Point				MAC8	ST-1-3	Yes	Yes	LV8760T
TP1-TP15	15									LV8761V

3. Evaluation board circuit

<LV8760T>



<LV8761V>



4. Evaluation Board Manual

[Supply Voltage] VM (9 to 35V): Motor Power Supply
VCC (3 to 5.5V): Control Power Supply
VREF (0 to VCC-1.8V): Current Limit Control Reference Voltage

[Toggle Switch State] Upper Side: High (VCC)
Middle: Open, enable to external logic input
Lower Side: Low (GND)

[Operation Guide]

1. **Initial Condition Setting:** Set “Open or Low” all switches.
2. **Motor Connection:** Connect the Motor between OUTA and OUTB.
3. **Power Supply:** Supply DC voltage to VM, VCC and VREF.
4. **Ready for Operation from Standby State:** Turn “High” the PS pin toggle switch.
5. **Motor Operation:** Set IN1, IN2 and EMM (at LV8761V) pins according to the purpose (See LV8760T or LV8761V‘s logic table).

[Setting for External Component Value]

1. Current limit value

At VREF = 1.5V
Ilimit = VREF [V]/5/R1 [ohm]
= 1.5 [V] / 5 / 0.22 [ohm]
= 1.36 [A]

2. Current limit regeneration time and short-circuit detection time

Tscp ≈ C5 [pF]× Vthscp[V]/Iscp[μA]
= 100[pF] × 1[V]/5[μA]
= 20[μs]

5. Evaluation board waveform (DC motor drive)

Figure 37. Forward ↔ Output off
DC_motor load,PS=High,IN2=Low
Vcc=VREF=5V, VM=24V, RNF=GND

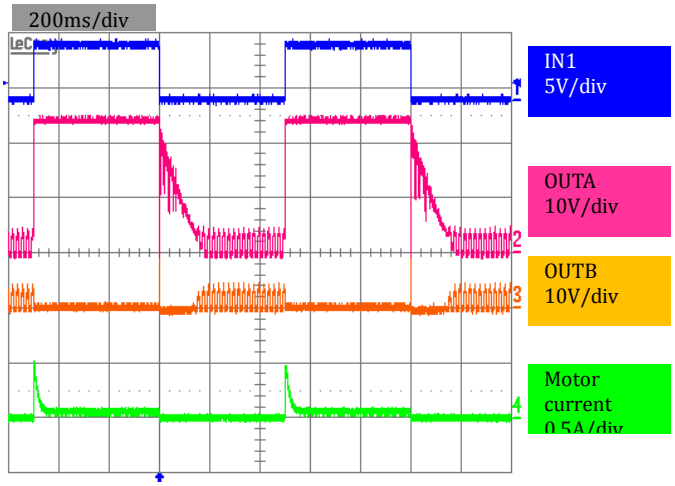
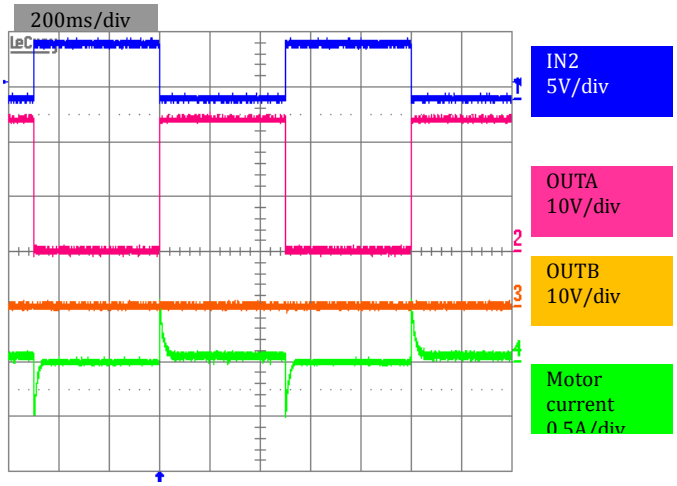


Figure 38. Forward ↔ Brake
DC_motor load,PS=High,IN1=High
Vcc=VREF=5V, VM=24V, RNF=GND



Cautions for layout:

●Power supply connection pin [VM,VCC]
- ✓ VCC is a control power supply, and VM is a motor power supply.
- ✓ Make sure that supply voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.
- ✓ Caution is required for VM supply voltage because this IC performs switching.
- ✓ The bypass capacitor of the VM power supply should be close to the IC as much as possible to stabilize voltage. Also if you intend to use high current or back EMF is high, please augment enough capacitance.

●GND pin [GND, PGND, RNF-resistor GND line, exposed die pad]
- ✓ High current flows into the PGND and GND side of RNF resistor; therefore, connect PGND and RNF – GND independently.
- ✓ On the other hand, since PGND and GND are connected through silicon board, if the line of PGND is too long, difference of electric potential occurs between PGND and GND which creates gradient to the GND electric potential within the IC board. This can be the cause of the IC malfunction. Hence make sure to connect PGND and RNF – GND independently so that the pins do not share the common impedance with GND. And GND, PGND, and RNF should be single-point grounded to the low impedance GND area near the IC. Also the capacitor between VM and GND should be connected adjacent to the IC.
- ✓ The exposed die-pad is connected to the board frame of the IC. Therefore, do not connect it other than GND. Independent layout is preferable. If such layout is not feasible, please connect it to signal GND. Or if the area of GND and PGND is larger, you may connect the exposed die pad to the GND.
  (The independent connection of exposed die pad to PGND is not recommended.)

●Internal power supply regulator pin [REG5]
- ✓ REG5 is a reference supply of the charge pump circuit and the power supply to drive output FET (typ 5V).
- ✓ When VM supply is powered and PS is “High”, REG5 operates.
- ✓ Please connect capacitor for stabilize REG5. The recommendation value is 0.1uF.
- ✓ Since the voltage of REG5 fluctuates (±10%), do not use it as reference voltage that requires accuracy.

●Input pin
- ✓ The logic input pin incorporates pull-down resistor (100kΩ).
- ✓ When you set input pin to low voltage, please short it to GND because the input pin is vulnerable to noise.
- ✓ The input is TTL level (H: 2V or higher, L: 0.8V or lower).
- ✓ VREF pin is high impedance.

●OUT pin [OUTA, OUTB]
- ✓ During chopping operation, the output voltage becomes equivalent to VM voltage, which can be the cause of noise. Caution is required for the pattern layout of output pin.
- ✓ The layout should be low impedance because driving current of motor flows into the output pin.
- ✓ Output voltage may boost due to back EMF. Make sure that the voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.

●Current sense resistor connection pin [RNF]
- ✓ To perform current limit control, please connect resistor to RNF pin.
- ✓ To perform saturation drive (without current limit control), please connect RNF pin to GND, and connect VREF pin to VCC.
- ✓ If RF pin is open, then short protector circuit operates. Therefore, please connect it to resistor or GND.
- ✓ The motor current flows into RF – GND line. Therefore, please connect it to common GND line and low impedance line.

●NC pin
- ✓ NC pin is not connected to the IC.
- ✓ If VM line and output line are wide enough in your layout, please use NC.