LV8805SV

ON Semiconductor®

http://onsemi.com

Bi-CMOS LSI

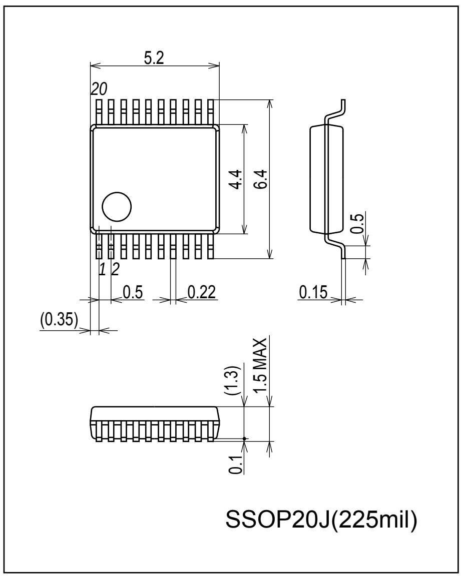
PC and Server
Fan Motor Driver
Application Note

Overview
LV8805SV is a 3-phase sensorless motor driver IC.
3-phase driver allows low power consumption and low vibration. And Hall sensorless drive allows reduction of the size of a motor system.
This IC is suitable for use in products which require high reliability and long life such as server fan and refrigerator fan.

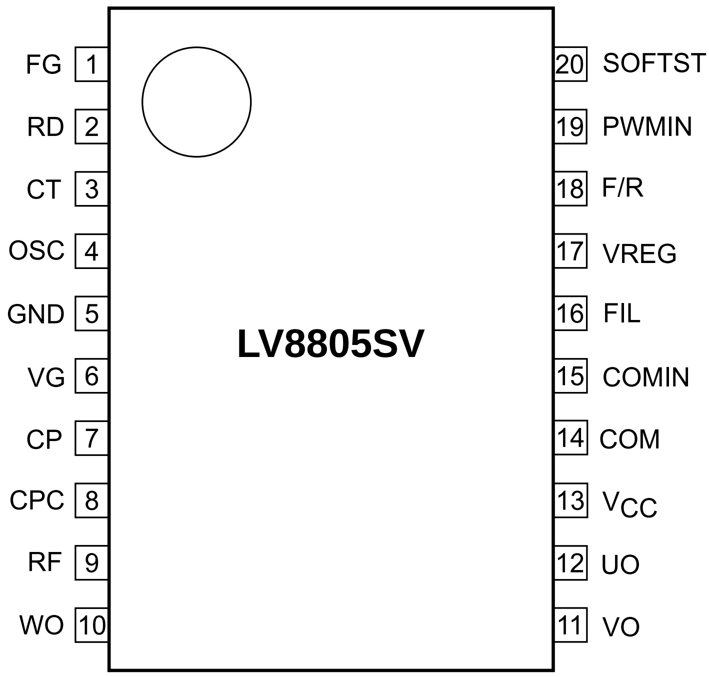
Function
- Direct PWM three-phase sensorless motor driver
- Built-in current limit circuit (Operates when RF resistance is 0.25 ohm and Io=1A)
- NchDMOS output transistor
- Built-in lock protection and auto-recovery circuit
- FG (rotation count) output signal pin / RD (lock detection) output signal pin
- Built-in TSD (thermal shutdown) circuit
- Direct PWM signal input for speed control (PWMIN pin)
- Motor startup with soft-start (SOFTST pin)

Typical Applications
- Server
- Refrigerator
- Desktop Computer

Package Dimensions
unit : mm (typ)



Pin Assignment

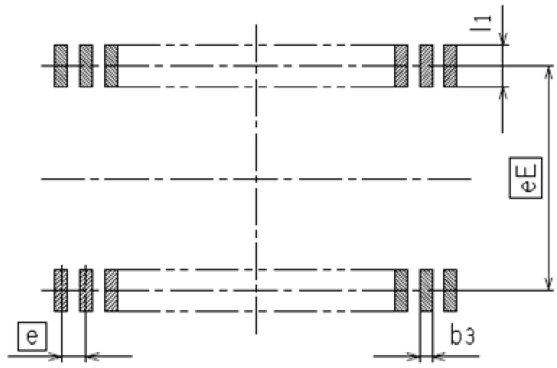


Caution: The package dimension is a reference value, which is not a guaranteed value.

Top view

December, 2013

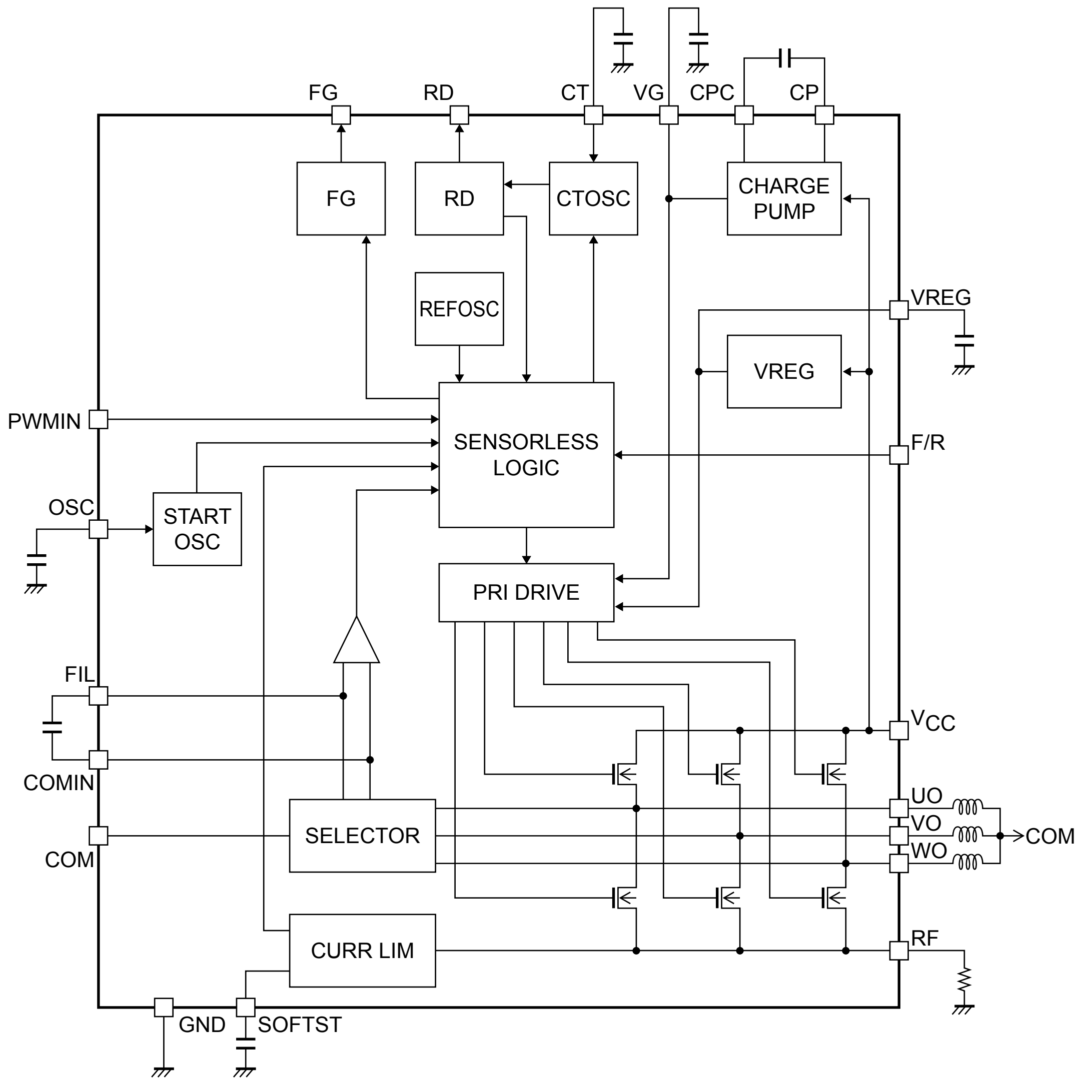
Recommended Soldering Footprint



(Unit:mm)

Reference Symbol	SSOP20J (225mil)
eE	5.80
e	0.50
b3	0.32
l1	1.00

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} maximum supply voltage	V_{CC} max		16	V
VG maximum supply voltage	VG max		21	V
OUT pin withstand voltage	V_{OUT} max		16	V
OUT pin maximum output current	I_{OUT} max	UO pin, VO pin, WO pin	1.2	A
SOFTST pin withstand voltage	V_{SOFTST} max		6	V
FR pin withstand voltage	V_{FR} max		6	V
PWMIN pin withstand voltage	V_{PWMIN} max		6	V
FG output pin withstand voltage	V_{FG} max		16	V
FG pin output current	I_{FG} max		5	mA
RD output pin withstand voltage	VRD max		16	V
RD pin output current	IRD max		5	mA
Allowable Power dissipation	Pd max1	Independent IC	0.3	W
	Pd max2	Mounted on designated board *1	0.95	W
Operating temperature	Topr		-40 to +95	°C
Storage temperature	Tstg	*2	-55 to +150	°C

* : When mounted on the designated 76.1mm × 114.3mm × 1.6mm, glass epoxy board (single-layer)

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} supply voltage	V_{CC}		6		15	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current 1	$I_{CC}1$			2.6	3.6	mA
Charge pump block						
Charge pump output voltage	V_{VG}			17		V
Regulator block						
5V regulator voltage	V_{VREG}		4.75	5	5.25	V
Output on resistance						
Sum of high-/low-side output transistor on resistance	Ron (H+L)	I_O = 0.7A, V_{CC} = 12V, VG = 17V		1.2	2	Ω
Startup oscillator (OSC) pin						
OSC pin charge current	$I_{OSC}C$			-2.5		μA
OSC pin discharge current	$I_{OSC}D$			2.5		μA
PWM input (PWMIN) pin						
High-level input voltage range	$V_{PWMIN}H$		2.3		VREG	V
Low-level input voltage range	$V_{PWMIN}L$		0		1	V
Range of PWM input frequency	f_{PWMIN}		15		60	kHz
Forward/reverse switching pin						
High-level input voltage range	$V_{FR}H$	Order of current application : UOUT→VOUT→WOUT	2.3		VREG	V
Low-level input voltage range	$V_{FR}L$	Order of current application : UOUT→WOUT→VOUT	0		1	V

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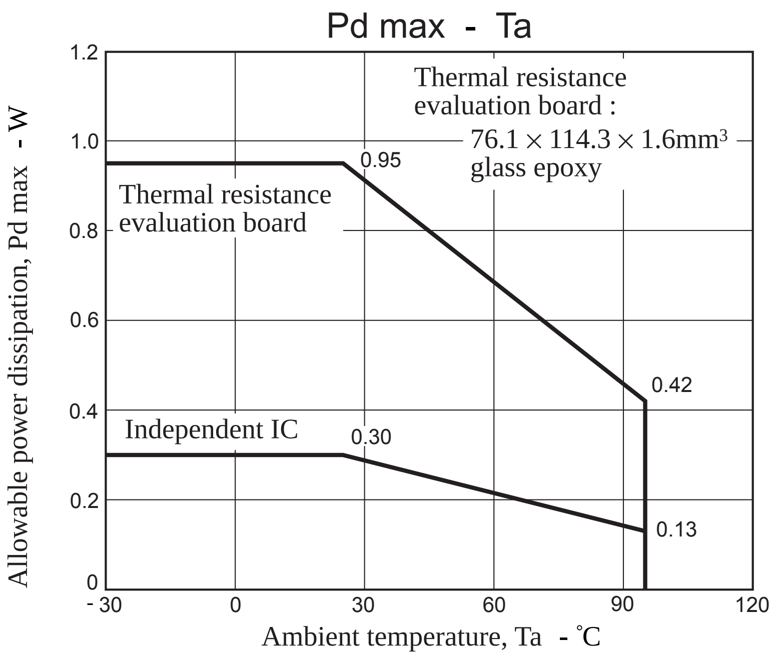
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG and RD output pins						
FG output pin low-level voltage	V_{FG}	When I_O is 2mA		0.25	0.35	V
FG output pin leak voltage	ILFG	When V_{FG} is 16V			1	μA
RD output pin low-level voltage	V_{RD}	When I_O is 2mA		0.25	0.35	V
RD output pin leak voltage	ILRD	When V_{RD} is 16V			1	μA
Current limiter circuit						
Limiter voltage	V_{RF}	Limit current set to 1A when RF is 0.25Ω.	0.225	0.25	0.275	V
Constraint protection circuit						
CT pin high-level voltage	$V_{CT}H$		2.25	2.8	2.95	V
CT pin low-level voltage	$V_{CT}L$		0.43	0.5	0.65	V
CT pin charge current	$I_{CT}C$		-2.9	-2.5	-2.1	μA
CT pin discharge current	$I_{CT}D$		0.21	0.25	0.32	μA
ICT charge/discharge ratio	R_{CT}		7	10	13	
Soft start circuit						
Soft start releasing voltage	V_{SOFTST}			2.5		V
SOFTST pin charge current	I_{SOFTST}			0.6		μA
Thermal protection circuit						
Thermal protection circuit operating temperature	TSD	Design target *	150	180	210	°C

*Design target value and no measurement is made. The thermal protection circuit is incorporated to protect the IC from burnout or thermal destruction. Since it operates outside the IC's guaranteed operating range, the customer's thermal design should be performed so that the thermal protection circuit will not be activated when the fan is running under normal operating conditions.



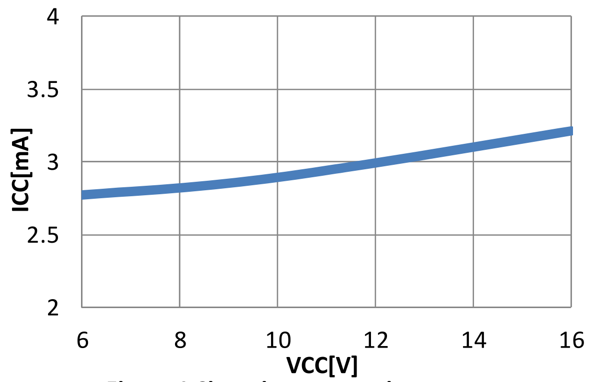


Figure 1 Ciurcuit consumption cueernt vs Supply voltage

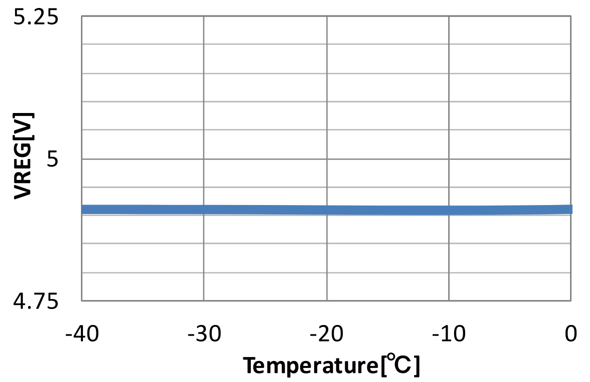


Figure 2 VREG pin output voltage vs Temperature

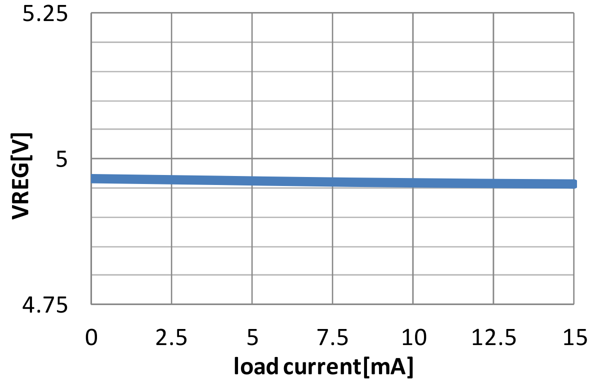


Figure 3 VREG pin output voltage vs load current

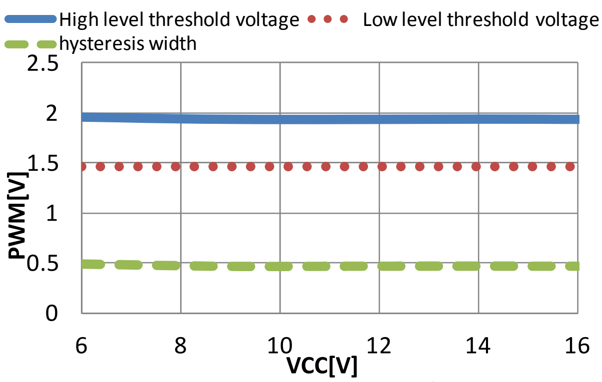


Figure 4 PWM pin output voltage vs VCC

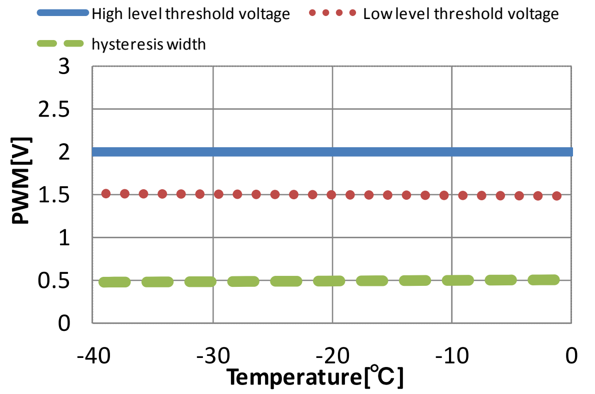


Figure 5 PWM pin output voltage vs Temperature

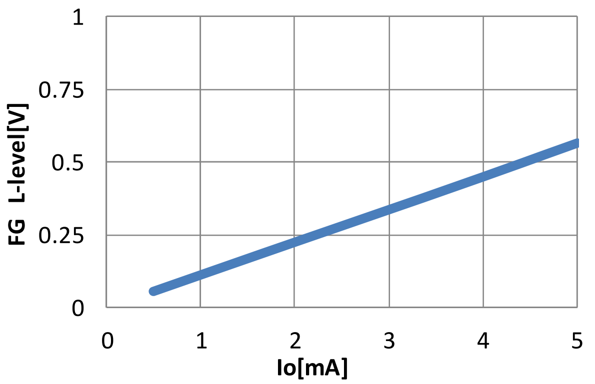


Figure 6 FG Low level voltage vs output current(Io)

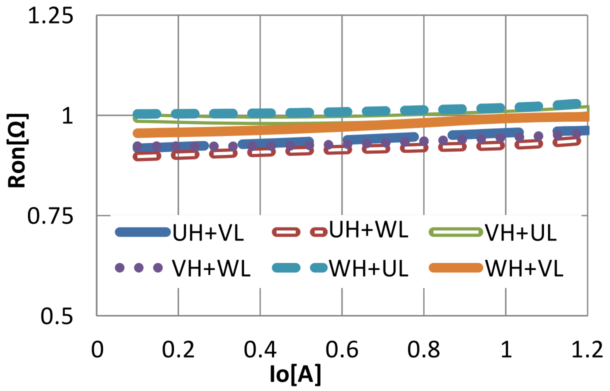


Figure 7 output on resistance vs output current (Io)

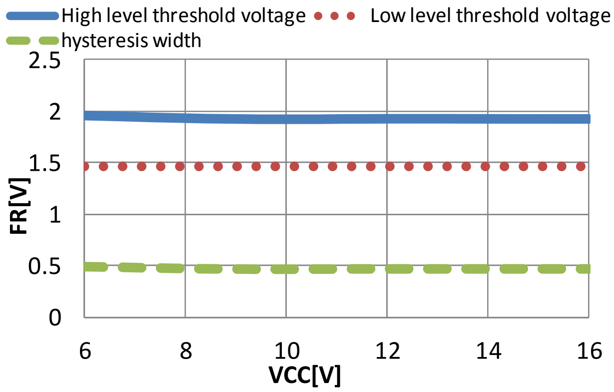


Figure 8 FR pin Hi-Lo level threshold voltage vs VCC

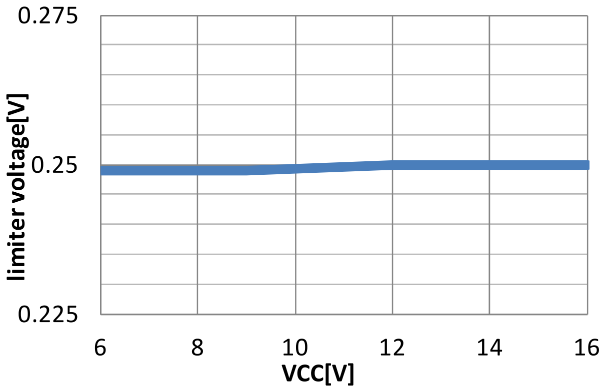
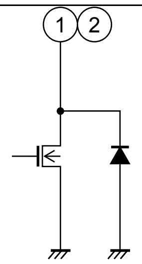
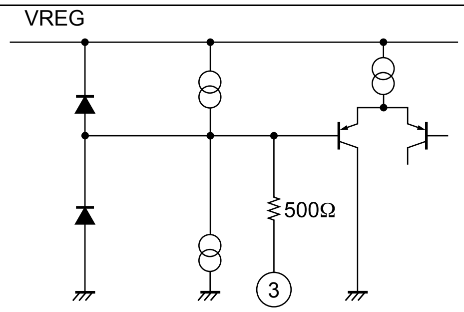
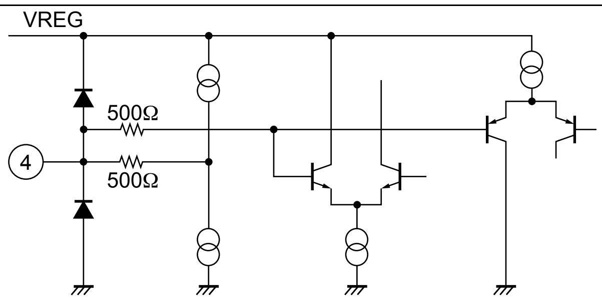
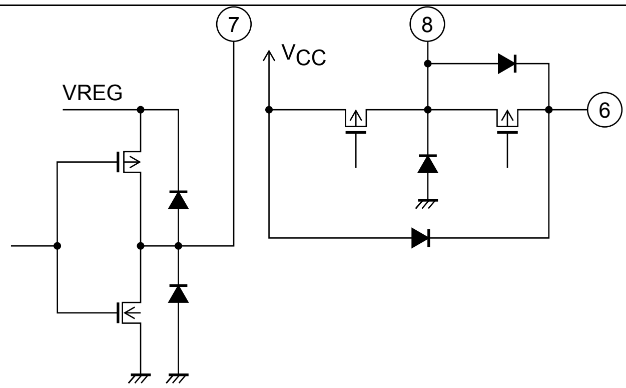
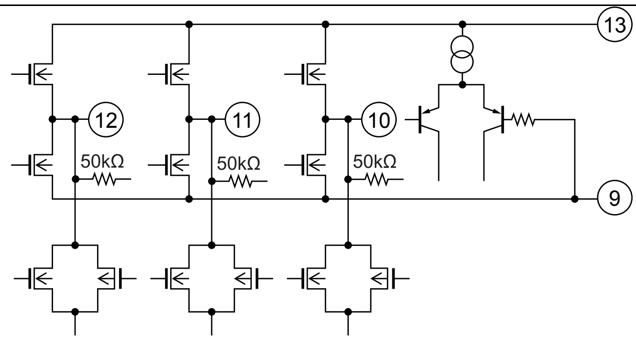


Figure 9 RF pin limiter voltage vs VCC

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	FG	FG pulse output. This pin outputs a Hall sensor system equivalent pulse signal.	
2	RD	Motor lockup detection output. Output is fixed high when motor is locked up.	
3	CT	Motor lockup detection time setting. When the motor lockup condition is detected, the protection time period before the protection circuit is activated is set by connecting a cacacitor between this pin and ground.	
4	OSC	Motor startup frequency setting. A capacitor must be connected between this pin and ground. The startup frequency is adjusted by controlling the charge/discharge current and capacitance of the capacitor.	
5	GND	GND pin	
6	VG	Charge pump step-up voltage output. A capacitor must be connected between this pin and the V_{CC} pin or ground.	
7	CP	Charge pump step-up pulse output pin. A capacitor must be connected between this pin and the CPC pin (pin 8).	
8	CPC	Charge pump step-up pin. A capacitor must be connected between this pin and the CP pin (pin 7).	
13	V_{CC}	Power supply for the IC and motor. Capacitors must be connected between these pins and ground.	
12 11 10	UO VO WO	Output pins. Connect these pins to the U, V, and W of the motor coil.	
9	RF	Output current detection pins. The drive current is detected by connecting a resistor between these pins and ground.	

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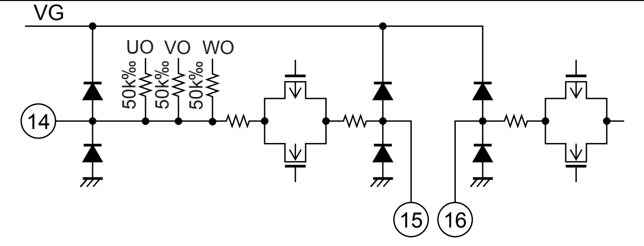
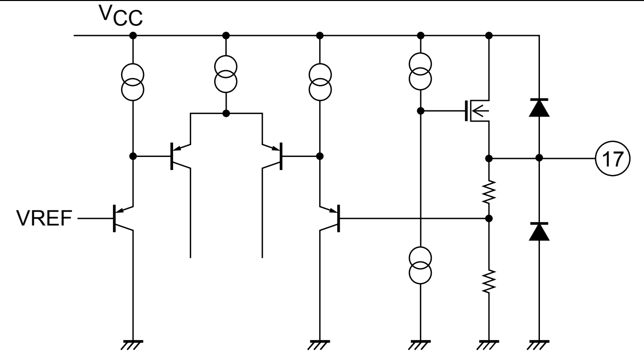
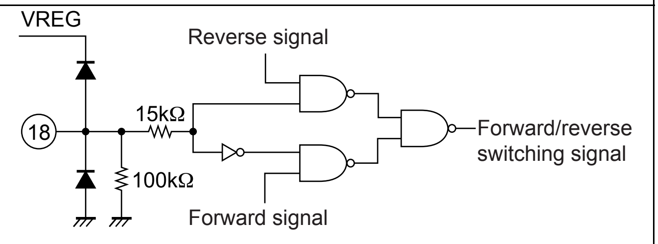
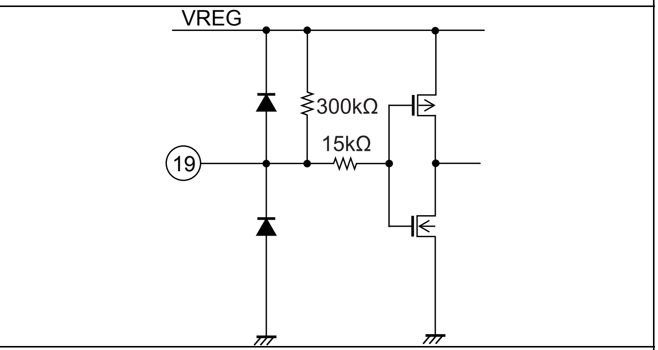
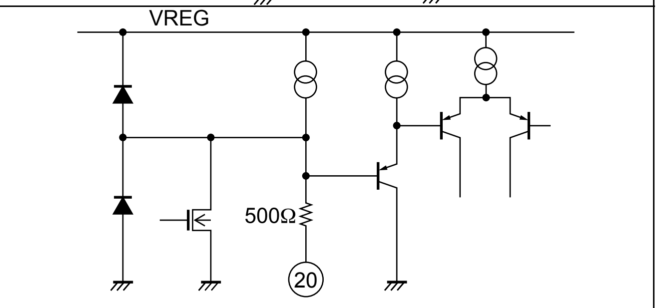
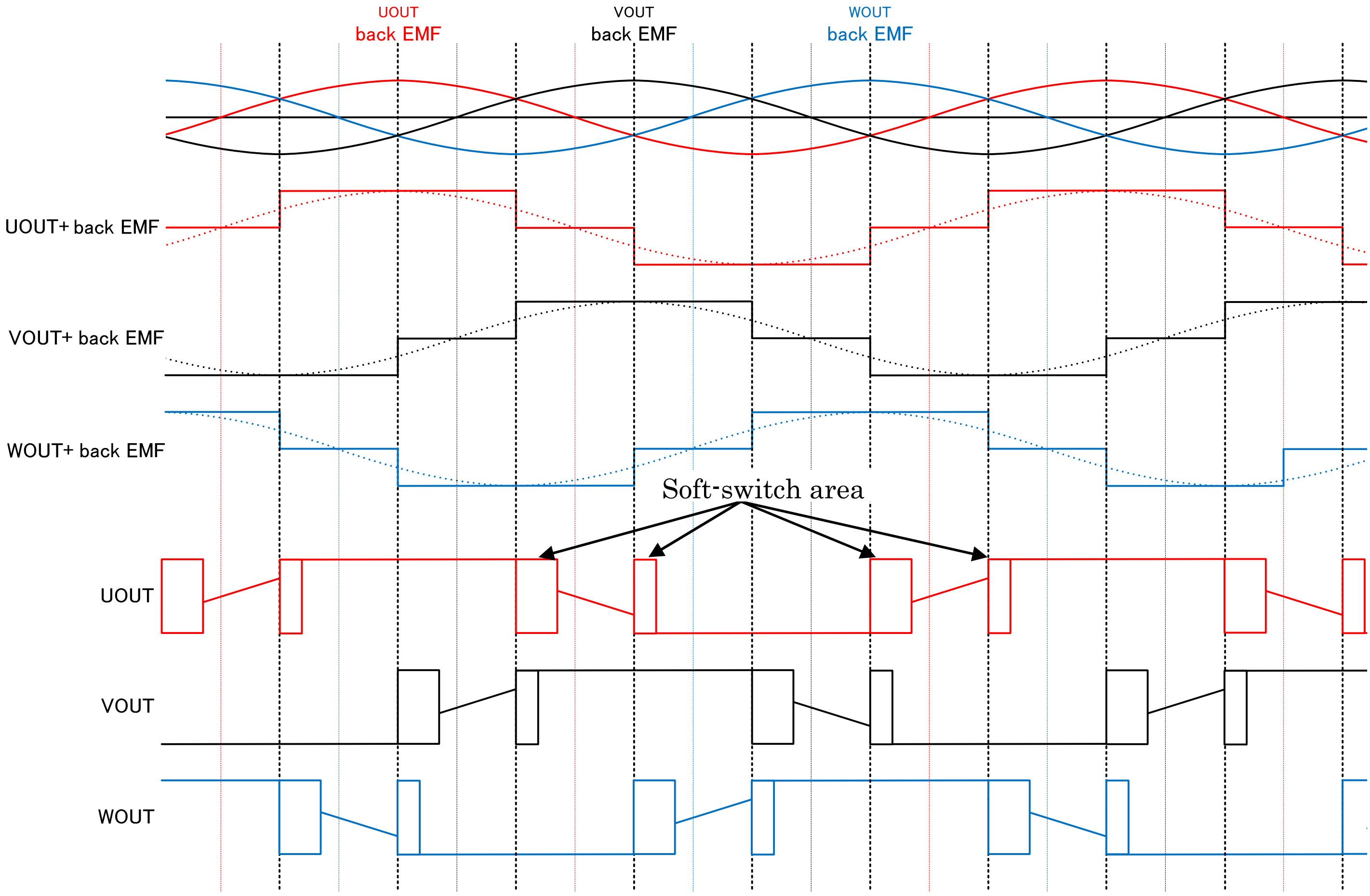
Pin No.	Pin name	Function	Equivalent circuit
14	COM	Motor middle point connection.	
15	COMIN	Motor position detection comparator filter pin. A capacitor must be connected between this pin and the FIL pin (pin 16).	
16	FIL	Motor position detection comparator filter pin. A capacitor must be connected between this pin and the COMIN pin (pin 15).	
17	VREG	Regulator voltage (5V) output. A capacitor must be connected between these pins and ground.	
18	F/R	Motor rotation direction switching. A high-level input causes current to flow into the motor in the order of U, V, and W and a low-level input in the order of U, W, and V. Changing the order of current application turns the motor in the opposite direction.	
19	PWMIN	PWM signal input pin. "H" The output transistor is turned on by the level voltage input. "L" The output transistor is turned off by the level voltage input, and the motor stops. The speed of the motor is controlled by controlling Duty of the input signal. When the pin opens, the motor becomes all velocities.	
20	SOFTST	Soft start time setting. The motor can be started smoothly by connecting a capacitor between this pin and ground.	

1. Operation overview

LV8805 is a PWM three-phase sensor less motor driver.
In the sensor less drive, the timing of motor commutation switch is determined by comparing back EMF signal generated from a motor and the voltage of CON pin (motor middle point voltage).
After power activation, supply any PWM signal input to PWMIN pin to impress output voltage to the motor coil.

- The FG signal of the frequency is output according to motor rotation.
- RD Output is fixed high when motor is locked up and it is fixed low while motor is driving.
- Speed of motor rotation is controllable by changing PWM signal input voltage of PWMIN pin.
- Motor can start up slowly by connecting a capacitance between SOFTST pin and GND pin.
- Motor locking time is settable by connecting a capacitance between CT pin-GND.

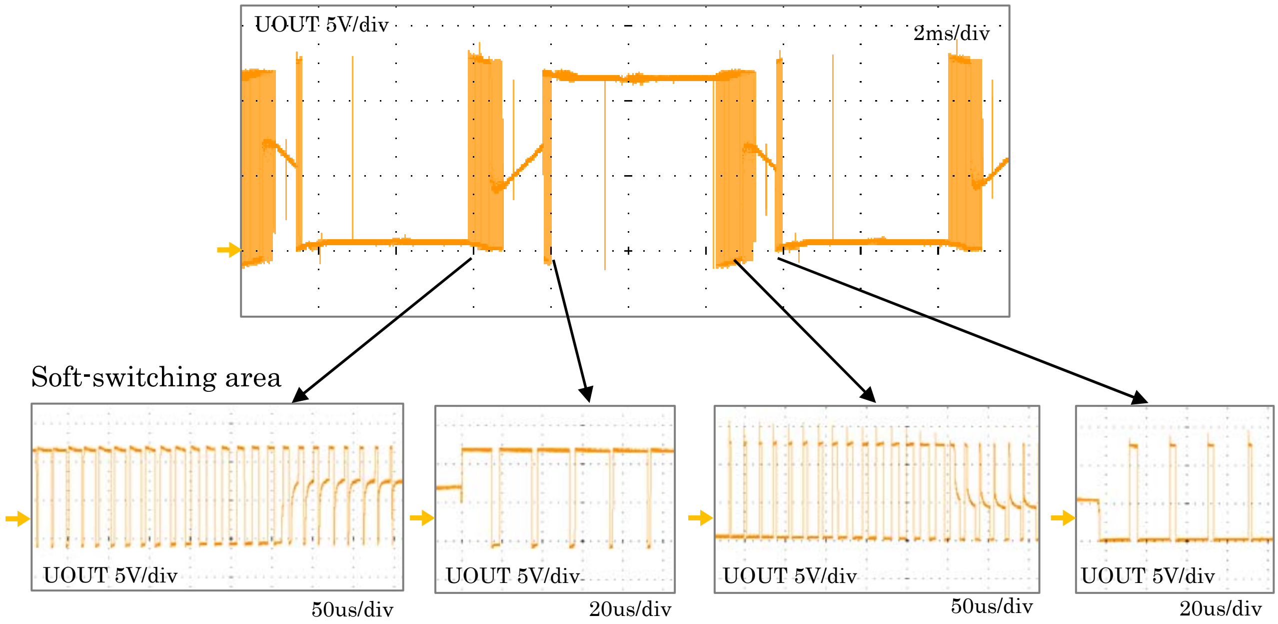


Output waveform

Full speed drive (PWM100%)

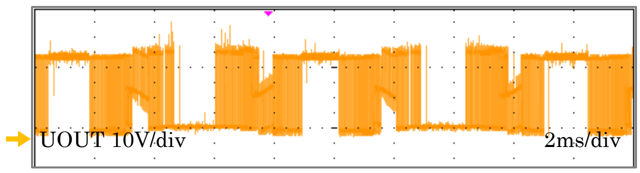
The waveform of output voltage of UOUT pin and FG pin are as follows. This graph shows the waveform when motor drives at full speed.

The waveform of output voltage for UOUT, VOUT and WOUT are the same.

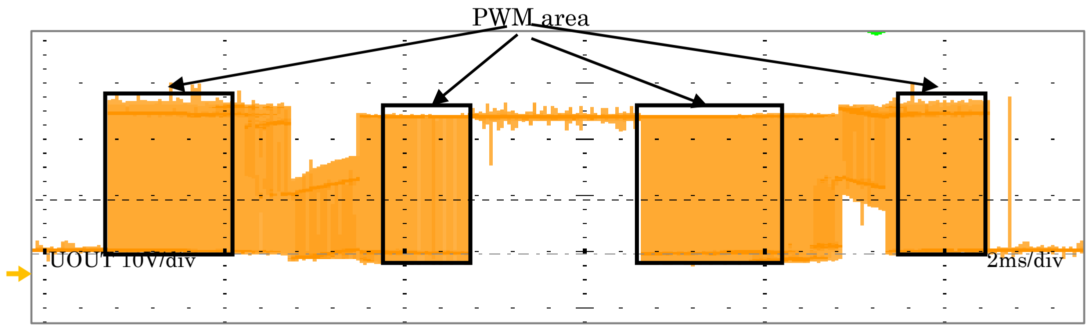


There are soft switching zone in UOUT signal. Soft switching smoothes out a motor coil current and enables silent drive.

PWM drive



The waveform of output voltage of UOUT pin and FG pin are as shown above. This is when the speed of motor is controlled by PWM.



There are soft switching zones and PWM zones in UOUT signal.

2. Sensor less control

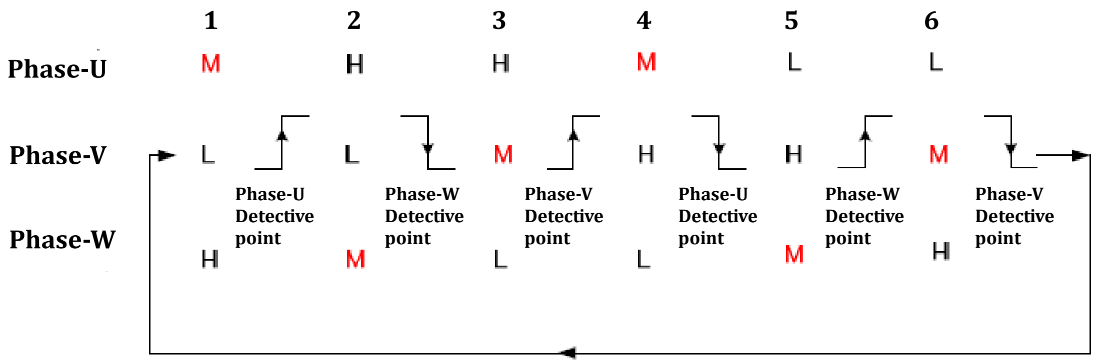
LV8805 is a sensorless motor driver which detects back EMF signal during motor rotation to detect a rotor position. According to a detected rotor position, a specified output transistor turns on or off, which enables motor rotation.

When starting up a motor, it is impossible to detect the rotor position because back EMF signal is not generated. Therefore, motor starts up by turning on and off a specified output transistor by an oscillation frequency defined by a capacitor between OSC pin and GND pin (startup mode). Then after the startup, a rotor position is detected by back EMF signal (driving mode).

Principle for Motor starting operation

1) Start up mode → 2) Driving mode

Switching pattern of output transistor when the motor start up



* M: output Tr OFF H: upper output Tr ON L: lower output Tr ON

In the above figure, UOUT is OFF (Middle), VOUT turns on lower output Tr (Low) and WOUT turn on upper output Tr (High). The back EMF signal of motor coil is detected by comparing back EMF signal of UOUT and voltage of COM pin (motor middle point). And output energization pattern is changed as follows: 2→3→4→5→6→1.

If the back EMF signal of motor coil cannot be detected after pattern "1", output transistor moves on to the next pattern "2" at the switching timing defined by a capacitor between OSC pin and GND pin. If back EMF signal of motor coil is detected at WOUT, output energization pattern changes to "3→4→5→6→1→2".

The timing when the change of output energization takes place varies depends on motor types.
Hence it is necessary to set up an optimum OSC capacitor for the motor. (Refer to "Start up pin setting")

3.1 How to set pin

Startup pin

In order to adjust startup characteristics of a motor, it is necessary to set OSC pin (OSC-GND capacitor) and COMIN pin FIL pin (COMIN-FIL capacitor) with optimal capacitances.

The best capacitance depends on motor and condition (power supply, coil current, number of rotation). Hence be sure to make an adjustment to each motor to find an optimal capacitance.

3.1.1 OSC-GND capacitance setup

(Recommendation value 470pF - 4700pF)

Startup frequency is defined by OSC capacitance.

The output energizing pattern is changed at the time of startup by the 1/134 of OSC frequency.

OSC frequency is determined by repeating charge and discharge to OSC capacitor.

The formula for obtaining OSC frequency is as follows.

$$Fosc = \frac{1}{Toscc + Toscd}$$

$$Toscc = \frac{(Vosch - Voscl) \times Cosc}{Ioscc}$$

$$Toscd = \frac{(Vosch - Voscl) \times Cosc}{Ioscd}$$

OSC pin frequency: fosc

OSC capacitor charge time: Toscc

OSC capacitor discharge time: Toscd

OSC capacitance: Cosc

OSC pin high-level voltage: Vosch=1.1V(TYP)

OSC pin low-level voltage: Voscl=0.6V(TYP)

OSC pin charge current: Ioscc

OSC pin discharge current: Ioscd

In general, low OSC capacitance tends to be used if a usage motor runs at a high speed. And high OSC capacitance is used if a usage motor runs at low speed.

- When a capacitance is high and:
  - Startup is slow and fails.
  - Startup time varies widely.

Example) fan motor startup test of LV8805

Condition: Vcc=12V

OSC capacitance=1500 pF

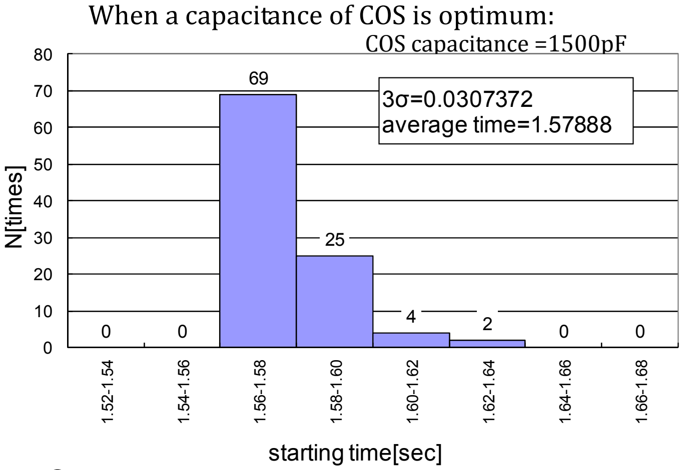
SOFTST capacitance =1 uF

Goal number of revolutions=4500 rpm*

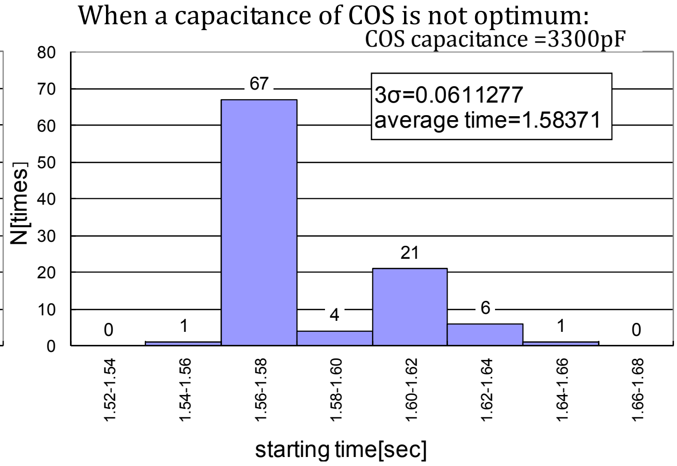
COMIN-FIL capacitance =2200 pF

Test count=100 times

When a capacitance of COS is optimum:



When a capacitance of COS is not optimum:



◎If such behavior is witnessed, use a lower capacitor instead.

*refer to “**8. Relation between FG frequency and number of rotation**”

- When a capacitance is low and:
  - Startup fails.
  - Beat lock* occurs.

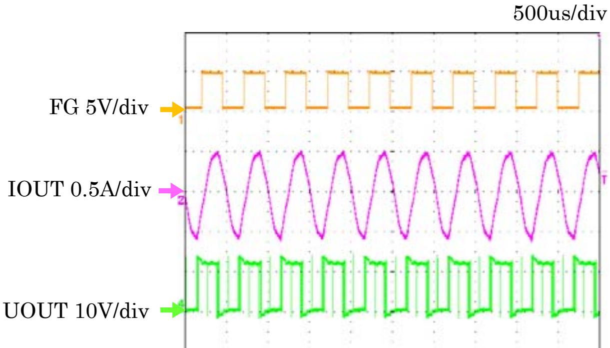


Fig. The output waveform with beat lock

◎If such behavior is witnessed, use a higher capacitor.

Select a capacitance values that allows the shortest possible startup time to achieve target speed and minimal variations in startup time.
The optimum OSC constant depends on the motor characteristics and startup current, so be sure to recheck them when either motor or circuit specifications is changed.
(* Refer to **"3.3 Beat lock"**)

3.1.2 COMIN-FIL capacitance setting

(Recommendation value: 1000 ~ 10000pF)
Compare the back EMF signal from motor and the voltage of CON pin (motor middle point voltage) to detect the rotor position. The switch timing of motor commutation is determined according to the detected rotor position. Based on the information, energization timing of motor is determined.
Insert a filter capacitor between the COMIN pin and FIL pin to prevent startup failure caused by noise.

- When a capacitance is high and:
  - The timing of output energization is slow during motor rotation. → Driving efficiency falls.

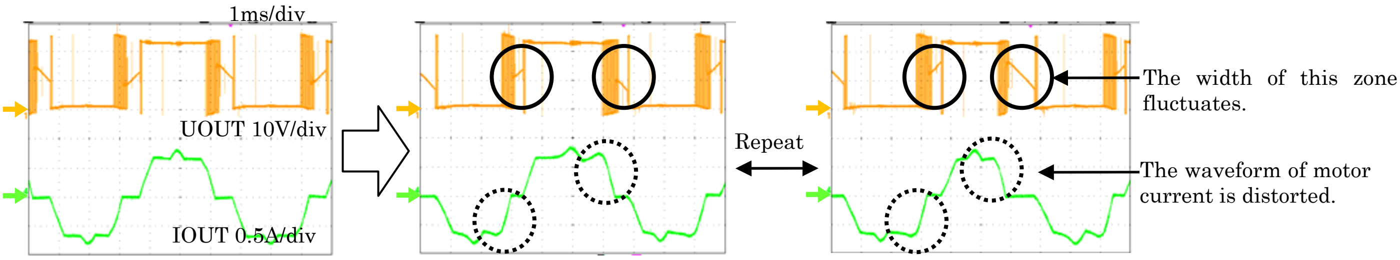


Fig. normal waveform   Fig. waveform when FIL-COMIN capacitance is too large.

◎If such behavior is witnessed, use a lower capacitor instead.

- When a capacitance is low and:
  - Beat lock* occurs.
  - If the capacitor is connected to CT pin, it is hard to switch to Lock protection ** mode.

◎If such behavior is witnessed, use a higher capacitor instead.

A capacitor is selected by checking a usage motor. Run the motor to see whether there is any issue with startup.
(* Refer to **3.2 Beat lock on next page.**)
(** Refer to **3.3 CT pin setup.**)

3.2 Beat lock

Beat lock may occur when a motor is stopped abruptly during motor operation or OSC capacitor is too low. Output waveform under the influence of beat lock is as shown below.

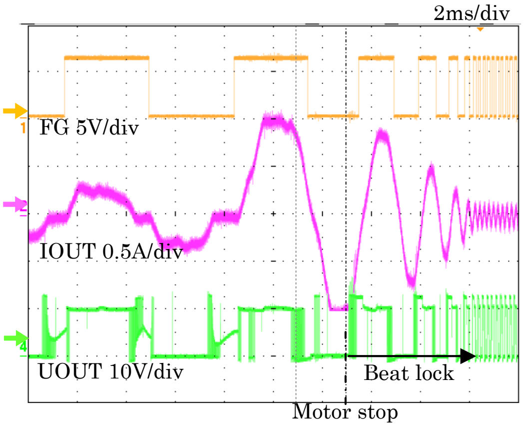


Fig. The beat lock caused by a motor quick stop

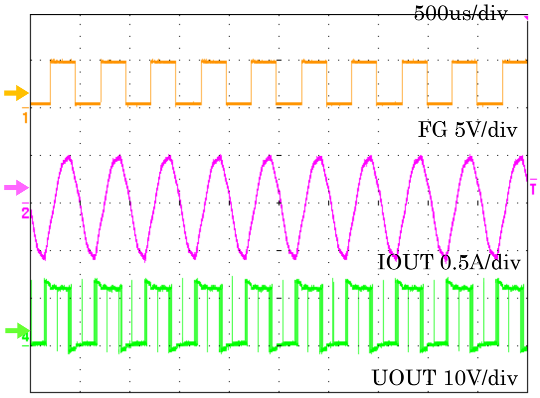


Fig. The beat lock weave form.

{Behavior}

- There is intense switching sound from transistor and then the motor stops.
- Waveform of OUT pin and FG pin shows the influence of noise.
- Motor cannot restart automatically after motor rotation stops.

Countermeasures:

1) False detection of the internal comparator is prevented by adjusting a capacitor between COMIN and FIL. Basically, the number of false detection by the internal comparator decreases with a higher capacitor between COMIN and FIL.
However, care must be taken for the adjustment since excessively high capacitance will give rise to deterioration in efficiency and delays in the output power-on timing while the motor is running at high speed.

2) Increase the OSC capacitance. By doing so, OSC frequency decreases, which prevents false detection by the internal comparator due to delay in the output power-on timing. Consequently, beat lock is prevented.

3) Connect a resistor between COMIN pin and GND pin. By doing so, offset is added to the zero-cross detection comparator. This addition of offset decreases the false detection by the comparator.
As a result, beat lock is prevented.
Offset voltage is obtained by the following formula:

Offset voltage

$$= \frac{1}{2}\mathrm{Vcc} - \left(\frac{1}{2}\mathrm{Vcc} \times \frac{\text{between COMIN and GND resistance}}{\text{between COM and COMIN resistance} + \text{between COMIN and GND resistance}}\right)$$

(The resistance between COM and COMIN is about 10kohm, which is determined by the internal circuit.)

Example: VCC=12V, The resistance between COMIN and GND =1M ohm

$$\text{Offset voltage} = 12 \times 1/2 - \left(12 \times 1/2 \times \frac{1\mathrm{Mohm}}{10\mathrm{kohm} + 1\mathrm{Mohm}}\right) \fallingdotseq 59.4\mathrm{mV}$$

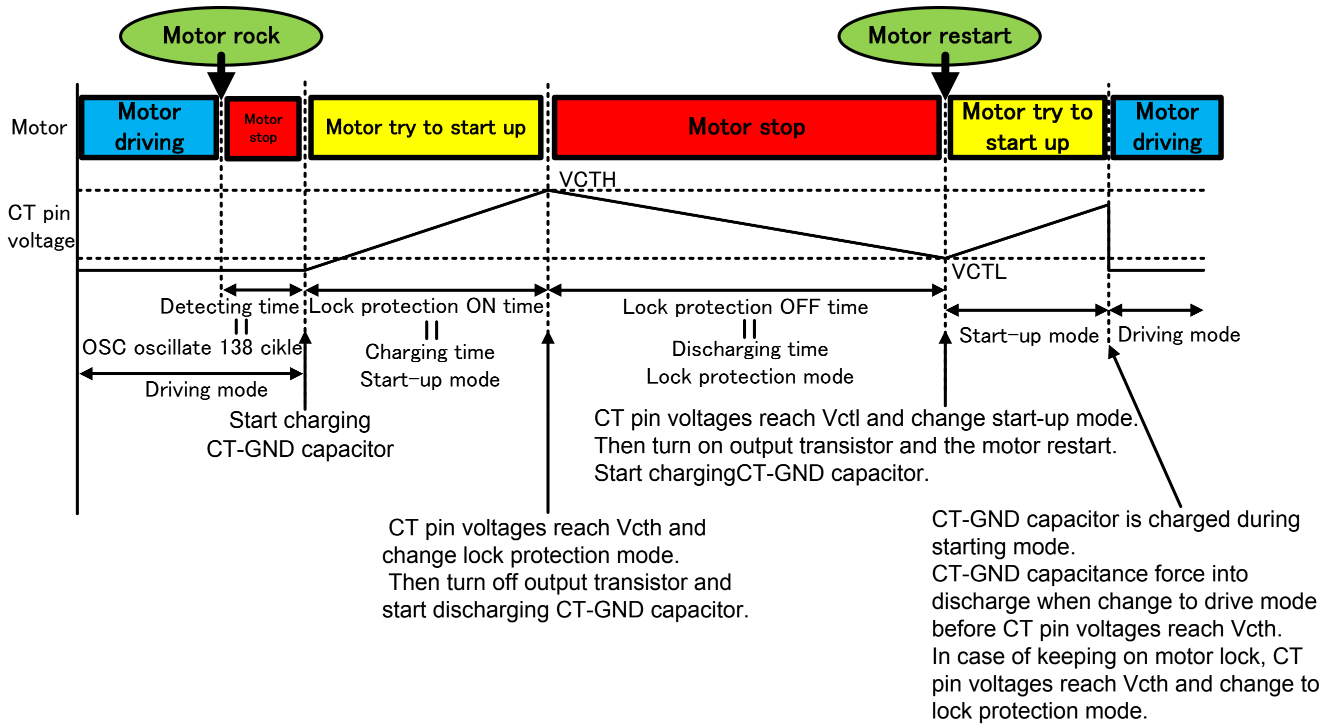
Approximately 60 mV of offset voltage is generated.

Recommended value of the resistance is approximately 1Mohm.
If a usage motor is replaced, please check the motor startup behavior again.

3.3 CT pin setting

Output transistors are turned off when the motor is stopped by some external factors. (Lock protection)

LV8805 Lock protector circuit Timingchart



Lock protection ON/OFF time is set by capacitor connected between CT pin and GND pin.
Lock protection ON time is the time between the start of charge for CT-GND capacitor by CT pin charge current and at the point where CT pin obtains high-level voltage (2.8Vtyp).
Lock protection OFF time is the time between the start of discharge for CT-GND capacitor by CT pin discharge current and at the point where CT pin obtains low-level voltage (0.5Vtyp).
Recommended capacitance for CT pin is 0.47uF-1uF.
Lock protection time is calculated by the following formula.

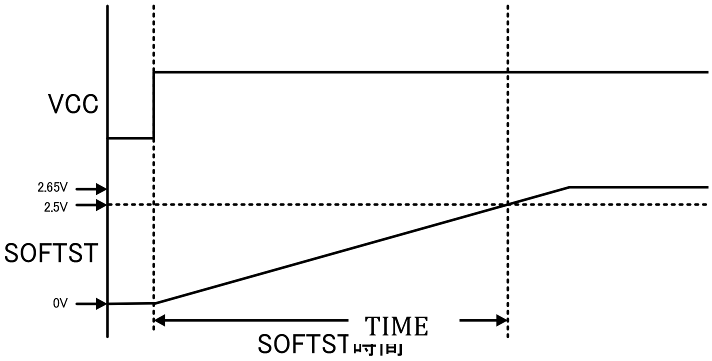
$$Tlon = \frac{Vcth \times Cct}{Ictd}$$

$$Tloff = \frac{(Vcth - Vctl) \times Cct}{Ictd}$$

Loc protection on time: Tlon
Loc protection off time: Tloff
CT pin high-level voltage: Vcth
CT pin low-level voltage: Vctl
CT pin capacitance: Cct
CT pin charge current: Ictc
CT pin discharge current: Ictd

When the power is ON or CTL pin is set from OFF to driving mode, IC always start from startup mode. Startup can fail if the motor does not start up before “lock protect on time”.
The timing depends on the relation of startup between the IC and motors. Hence it is necessary to check the startup behavior of usage motors. If CT pin is unused, connect this pin to GND.

3.4 SOFTST pin setting



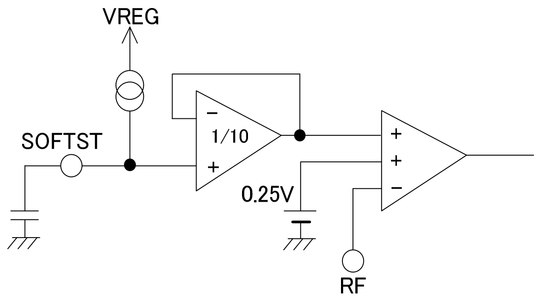


Fig. Block diagram of SOFTST pin.

As soon as the capacitor connected to SOFTST pin is charged, the voltage of SOFTST pin increases.
And SOFTST operation continues until the voltage of SOFTST pin reach to the point of “soft start cancel voltage” (2.5Vtyp). The soft start time is adjustable by changing capacitor connected between SOFTST pin and GND.
During soft start operation where the voltage of SOFTST is lower than “soft start releasing voltage”; current limit drive is performed by the limit current obtained by the following formula.

$$I = \frac{\text{voltage of SOFTST pin}}{10 \times \text{RF resistance}}$$

From the above formula we know that current limit value increases along with the voltage increase of SOFTST pin.
Motor rotation increases slowly because sharp current increase when starting up motor is under control.
Recommended capacitance of SOFTST pin is 0.47uF-1uF.
Softstart time is obtained by the following formula:

$$T_{soft} = \frac{V_{soft} \times C_{soft}}{I_{soft}}$$

Softstart time: T_{soft}
Softstart releasing voltage: V_{soft}=2.5V (TYP)
SOFTST pin capacitance:C_{soft}
SOFTST pin charge current: I_{soft}=0.6uA (TYP)

Note that if SOFTST pin capacitance is too high, the starting torque of motor is insufficient since the increase of motor current is moderate. As a result, lock protection may operate before the startup of motor. Therefore, it is necessary to check the optimum capacitance with a usage motor.
Connect pull-up resistor to VREG pin when SOFTST pin is unused.
Pull-up resistor should be approximately 10kohm (Recommended value).

3.5 Operating principle of charge pump and how to select a capacitor for VG pin and a capacitor between CP pin and CPC pin

Charge pump is a circuit which generates voltage to drive output transistors in LV8805.
LV8805 is a sensor-less motor driver which detects back EMF signal during motor rotation to determine a rotor position and runs the motor.
Back EMF from motor is detected by the internal comparator whose power source is the charge pump.
The operation principle of charge pump is as follows:

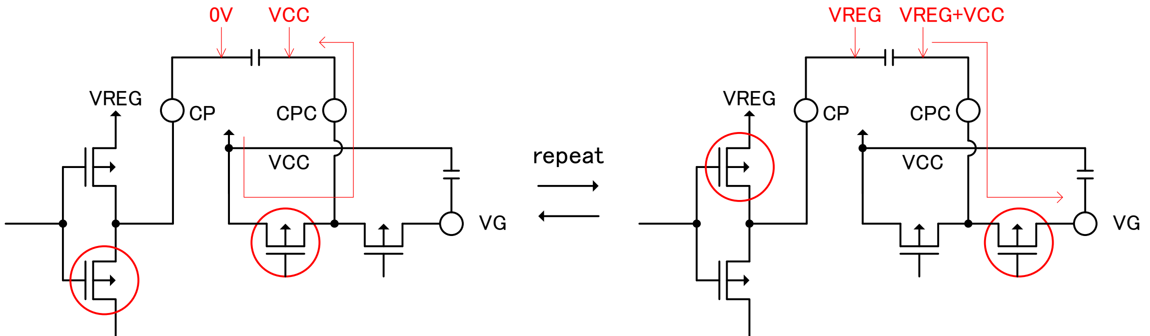


Fig. 1 Fig. 2

First, the transistors in red circles in Fig. 1 turn on. Then the capacitor between CP pin and CPC pin is charged and the voltage of CP pin turns 0V and CPC pin turns Vcc voltage, respectively.
Second, the transistors in red circles in Fig. 2 turn on. Then the electric charge in the capacitor between CP pin and CPC pin transfers to VG pin. Since the voltage of CP pin becomes VREG voltage, the voltage of CPC pin and GV pin is as follows: VREG voltage + Vcc voltage.

Last, through repeating the operations of Fig. 1 and Fig. 2, VG pin voltage increases and stabilizes at VREG voltage+ Vcc voltage.
Actually, VG voltage is a little lower than VREG voltage+ Vcc voltage since efficiency is not 100% and there is internal power consumption.

The function of capacitor between VG pin and VCC pin is to retain electric charge and to stabilize voltage.
(The capacitor connected to VG pin has the same function even when it is connected to GND.
The only difference is whether the initial voltage of VG pin is either GND or Vcc.)

When the capacitor between CP pin and CPC pin or VG pin is too low, voltage of VG pin decreases since power supply cannot catch up with the power consumption by circuits.
Therefore, the minimum VG pin voltage should be above Vcc+4V.
Also make sure that no ripple of voltage is observed in VG pin through checking oscilloscope when the IC is in operation.

Recommended capacitances of Charge pump are as follows:
The capacitance between CP pin and CPC pin: 0.033uF-0.1uF
The capacitance between VG pin and VCC pin: 0.1uF ~ above 0.22uF
The capacitors should be in the following relation:
The capacitance between CP pin and CPC pin ≤ The capacitance between VG pin and VCC pin

3.6 input signal condition of PWMIN pin

LV8805 is a direct PWM signal input system for speed control.
Recommendation Condition

High-level input voltage :	0 [V]
Low-level input voltage :	5 [V]
PWM frequency range :	20k-50k [Hz]

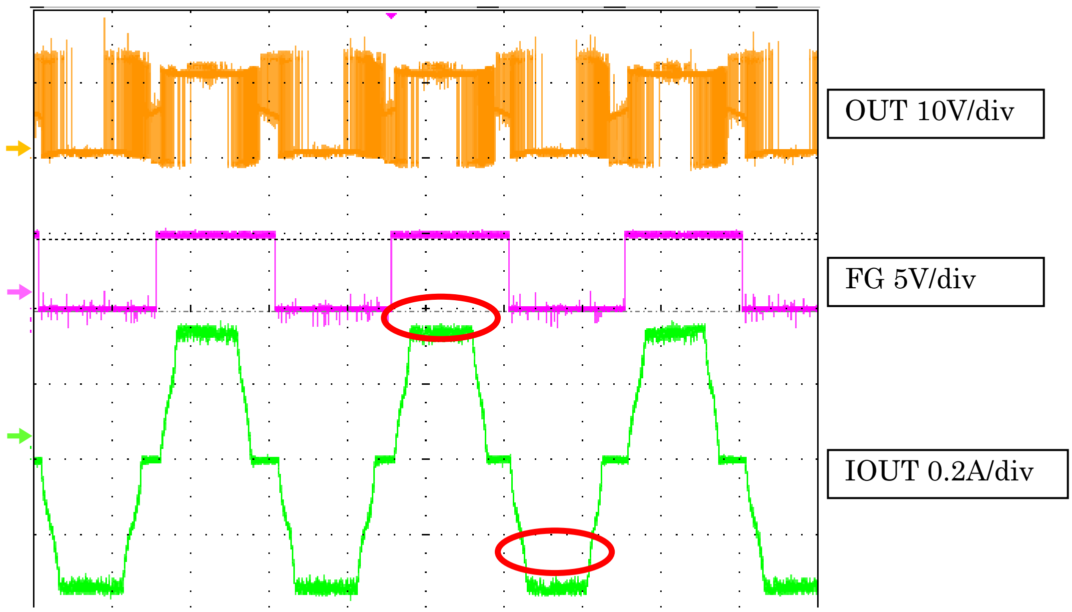
*Caution: The minimum pulse width of PWM signal is 0.2u [sec] (= duty of 1% at 50k [Hz])

4. Other protection circuits

4.1 Current limier

Current limiter is configured by adjusting the resistance between RF and GND.
When the pin voltage exceeds 0.25V, the current is limited, and regeneration mode is set. In the application circuit, the current limit setting voltage is 0.25V; therefore the current limit operates at 1A.
The calculation formula is given below.
RF resistance = 0.25V/target current limit value

Current limit driving

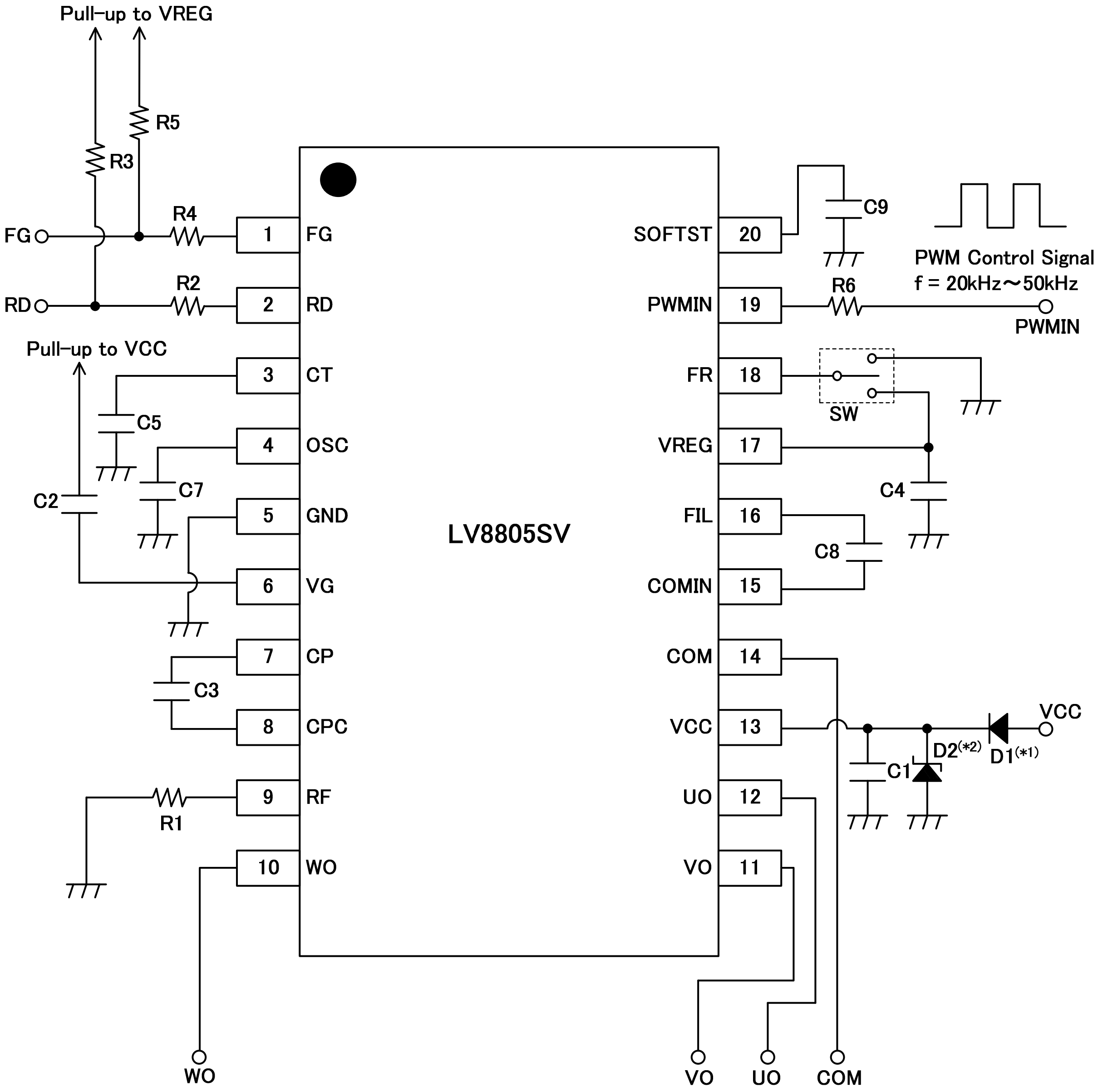


Red-circled IOUT is the current limited area.

4.2 Thermal protection circuit

LV8805 integrates thermal protection circuit. When Junction temperature, Tj exceeds 180°C, output transistor turns off.

5. Application Circuit Example



LV8805SV parts list

R1	0.25 ohm	C1	10uF/25V
R2	1K ohm	C2	0.1uF
R3	10K ohm	C3	0.1uF
R4	1K ohm	C4	1uF
R5	10K ohm	C5	1uF
R6	1K ohm	C7	1000pF
		C8	0.01uF
		C9	1uF

*This application circuit is only for example.
Please use this as reference when you design circuit for the first time.

6. Caution for the usage of evaluation board

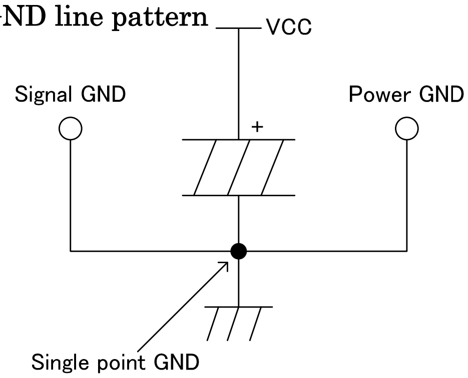
Parts that require connection as **close as possible to the IC**

- C1 (capacitor between Vcc-GND)
- C2 (capacitor between VG-Vcc)
- C3 (capacitor between CP-CPC)
- C4 (capacitor between VREG-GND)
- C7 (capacitor between OSC-GND)
- C8 (capacitor between COMIN-FIL)

Thick line (high current line)

- Vcc, GND, UO, VO, WO, RF

GND line pattern



(*1) Reverse connection protection diode (D1): This diode protects reverse connection.
Insert a diode between power supply and V_{CC} pin to protect the IC from destruction due to reverse connection. Connection of this diode is not necessary required.

(*2) LV8805 uses synchronous rectification for high efficiency drive. Synchronous rectification is effective for cutting heat and higher efficiency. However, it may increase supply voltage.
If the supply voltage shall increase, make sure that it does not exceed the maximum ratings by inserting a zener diode (D2) between power supply and GND.

(*3) The pins must be short-circuited on the print pattern.

- V_{CC} pins (13pin)
- GND pins (5pin)
- RF pins (9pin)
- VREG pins (17pin)

(*4) VREG pins (17pin) are the control system power supply pin and regulator output pin, which create the power supply of the control unit. Be sure to connect a capacitor between this pin and GND in order to stabilize control system operation.
Since these pins are used to supply current for control and generate the charge pump voltage, connect a higher capacitor than the capacitor connected to the charge pump.

(*5) Pin protection resistor (R2, R4, R6): It is recommended that resistors higher than 1k ohm are connected serially to protect pins against misconnection such as GND open and reverse connection.

Parts name and recommended value

Parts No.	name	Recommended value
C1	Vcc-GND	Over 10uF
C2	VG-Vcc(GND)	Over 0.1uF
C3	CP-CPC	0.033uF(about 1/3 of C2)
C4	VREG-GND	Above 1uF(larger than C2,C3)
C5	CT-GND	0.47uF~1uF
C7	OSC-GND	470~4700pF
C8	COMIN-FIL	1000~10000pF
C9	SOFTST-GND	0.47uF~1uF
R1	RF resistance	Above 0.25ohm(current limit=1A)
R2 R4 R6	Pin protection resistor	1k ohm (about 1/10 of R3,R5)
R3 R5	Pull-up resistance	10k ohm

7. Relation of thermal resistance

How to measure Tj

The surface temperature of IC is obtained from Tj of IC as follows:

In order to obtain a surface temperature of IC from a junction temperature of IC, a thermal resistance between junction part and case: θjc [°C/W] are required.
θjc is a thermal increase per power dissipation.
The calculation of θjc is quite difficult, so it should be obtained through measurement.
Jθjc of SSOP-20 package is 27°C/W when measured with independent IC, 17°C/W: with the glass epoxy board (size:76.1×114.3×1.6tmm)
The difference between the surface temperature of IC and junction temperature is obtained as follows:

Tj[°C] - Tc[°C]=Pd[W]×θjc[°C/W]
- Tj: Junction temperature
- Tc: Case temperature
- Pd: Power dissipation of the IC
- θjc: Thermal resistance between junction part and case

An approximate "Pd" value can be obtained by the following formula:

$Pd = Vcc \times Icc + Ron \times Im^2$
- Vcc: power supply
- Icc: circuit current by VCC
- Ron: Sum of the low and high side output transistor ON resistance
- Im: Current of motor drive

Where VCC=12V, ICC=4mA, Ron=2 ohm and Im=0.5A, Pd is obtained as follows:
12V × 4mA + 2 ohm × 0.5A × 0.5A = 548mW
When measured with independent IC without a board, Tj - Tc is 13.15°C.

* Caution
θjc is dependent on a board. Hence it is recommended to measure θjc with a usage board.

8. Relation between FG frequency and number of rotation

The relation between FG frequency (FG), number of motor rotations (N[rpm]) and pole number of motor magnetic (p) is as follows:

$$FG = \frac{p}{2} \times \frac{N}{60} \ [\mathrm{Hz}]$$

Based on the formula, number of motor rotations is obtainable from FG frequency.

$$\Rightarrow N = \frac{120 \times FG}{p} \ [\mathrm{Hz}]$$

Example) Where FG frequency=200Hz and pole number=4,

$$N = \frac{120 \times 200}{4} = 6000 \ [\mathrm{rpm}]$$

The maximum number of motor rotation controllable by LV8805 is:

$$\text{Maximum} = \frac{\text{PWM frequency(25kHz)} \times 60}{48 \times \text{p(pole number)}/2} \ [\mathrm{rpm}]$$

For example, the maximum number of motor rotation is approximately 15.6 k rpm when pole number is 4.
Make sure to use this device within this range of motor rotation.

9. Evaluation board manual

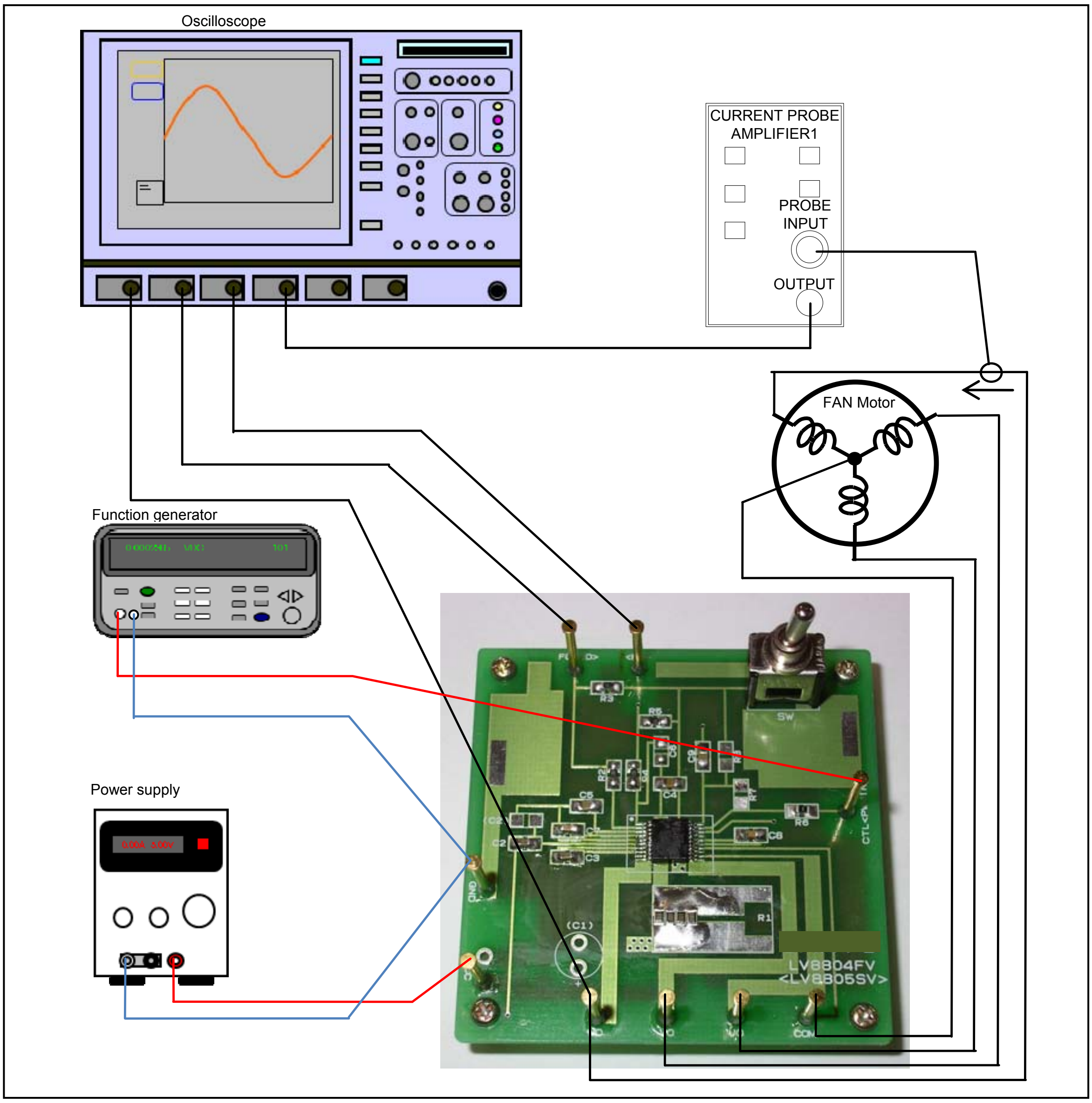


Table: Required Equipment

Equipment	Efficiency
Power supply	12V-1A
Function generater	PWM 0-5V /20-50kHz
Oscilloscope	4 channel
Current probe	
LV8805SV Evaluation Board	
Motor	12V-3W

Test Procedure:

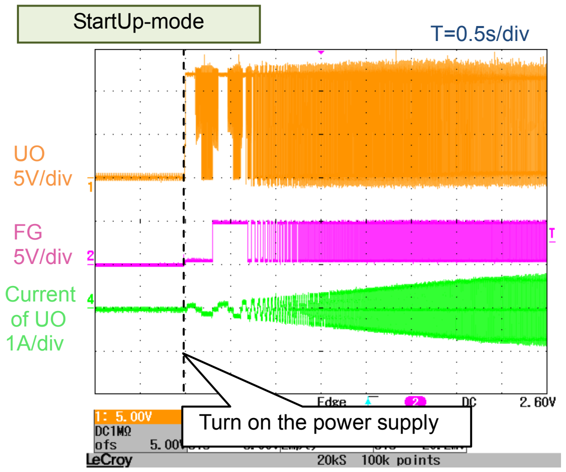
1. Connect the test setup as shown above.

2. Initial check
   Boot up at the VCC = 12V.
   PWMIN=5V (PWM 100%)
   Confirm that the motor rotates smoothly and in the right direction.
   Switch the FR switch when the motor rotation direction is different.

3. Booting check (StartUp-mode)
   Check whether a booting of a motor is stable. (Booting)
   Boot up at the VCC = 6V and 12V.
   When PWM input vary from 0% to 100%, check the change in the motor rotation speed.
   And then, at each VCC and PWM signal check whether a motor boots 100 times in 100times.

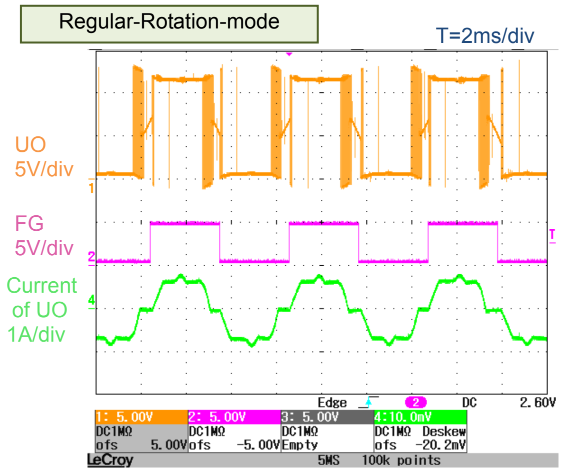
   Check the some waveforms. (Booting waveforms)
   Boot up at the VCC =12V.
   Check the WO, VO and FG voltage waveform at scope CH1, CH2 and CH3, and the output current waveform of WO at scope CH4 by the Oscilloscope.

   ex) These waveforms are different by each motor.



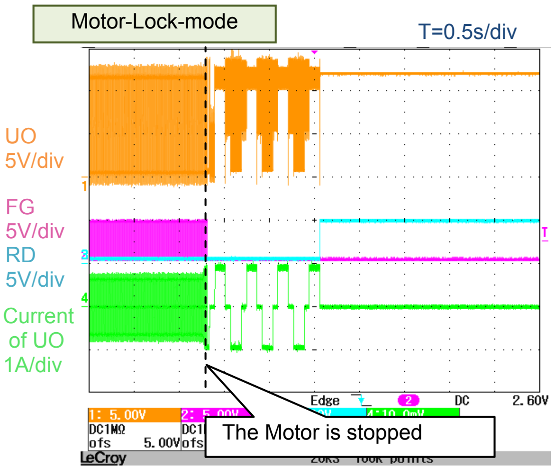
4. Normal rotation check (Regular-Rotation-mode)
   Check the some waveforms. (Rotation waveforms)
   Supply the VCC=12V. PWMIN=5V(PWM 100%)
   Check the WO, VO and FG voltage waveform at scope CH1, CH2 and CH3, and the output current waveform of WO at scope CH4 by the Oscilloscope.

   ex) These waveforms are different by each motor.



5. Lock detection check (Motor-Lock-mode)
   Check the Lock detection behavior. (Lock)
   Supply the VCC=12V. PWMIN=5V (PWM 100%)
   Check if the signal of WO, VO and UO is off when Motor is stopped manually.
   Then, check the WO, VO and FG voltage waveform at scope CH1, CH2 and CH3, and the output current waveform of WO at scope CH4 by the Oscilloscope.

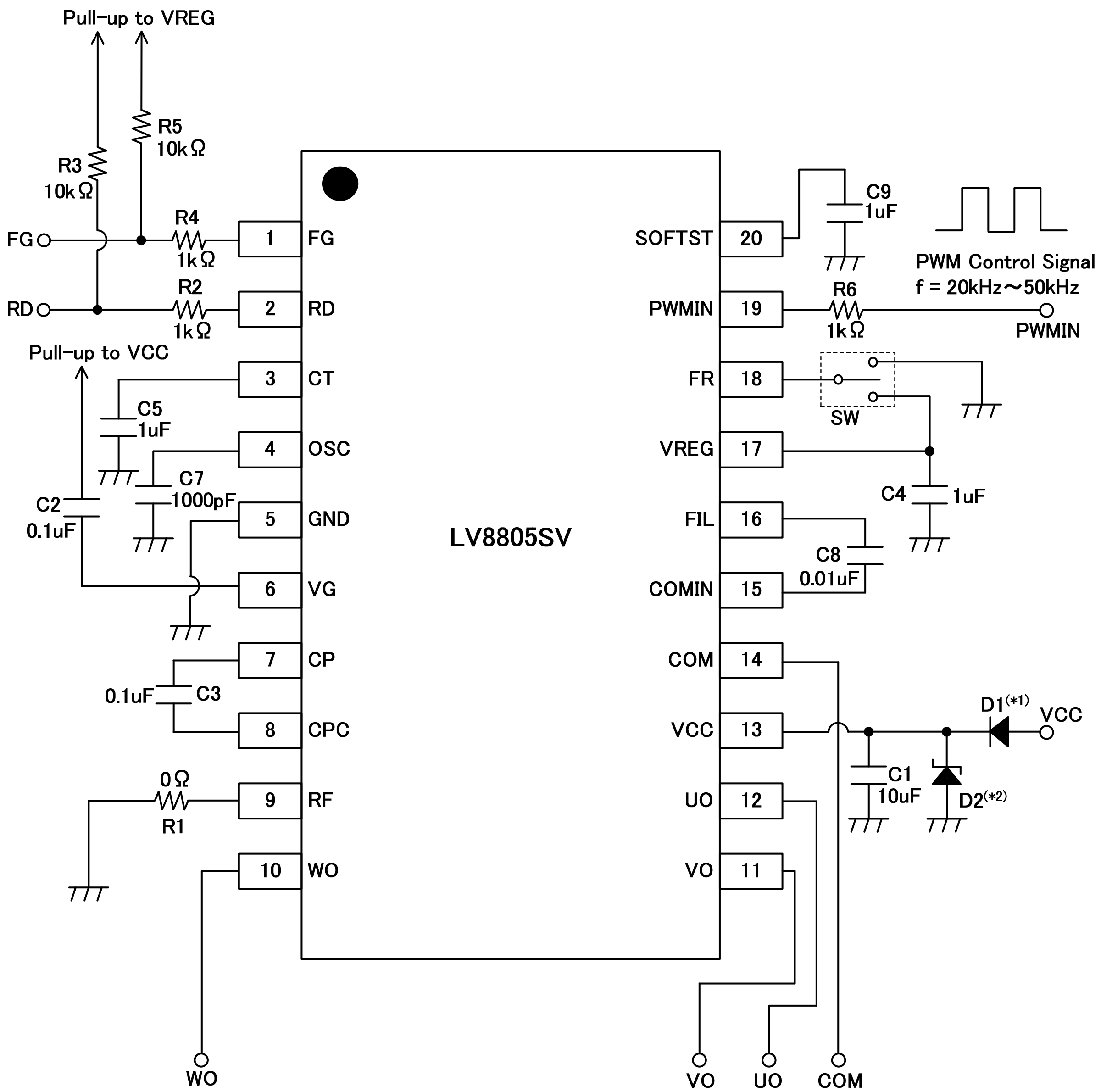
   ex) These waveforms are different by each motor.



6. Checking result
   A sample of checking result is shown below.

VCC	CTL voltage	Booting	Rotation speed (rpm)	Rotation waveforms	Io	Lock
12V	0V	100/100 OK		OK	value	OK
	1.5V	100/100 OK		OK	value	OK
	2.5V	100/100 OK		OK	value	OK
6V	0V	100/100 OK		OK	value	OK
	1.5V	100/100 OK		OK	value	OK
	2.5V	100/100 OK		OK	value	OK

Evaluation board circuit diagram

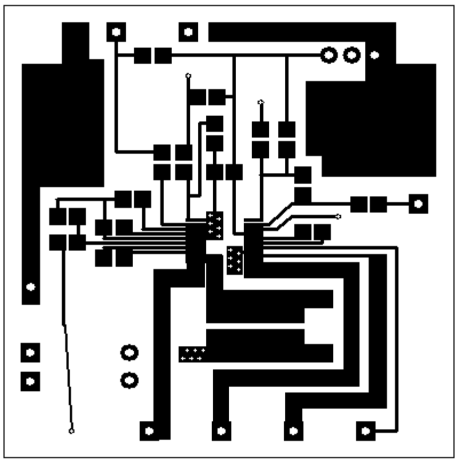


Bill of Materials for LV8805SV Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
IC1	1	Motor Driver			SSOP20J (225mil)	ON Semiconductor	LV8805SV	No	yes
C1	1	VCC Bypass capacitor	10μF 25V	±10%		murata	GRM32DR71E106KA12	yes	yes
C4,C5,C9	3	capacitor	1μF	±10%		murata	GRM21BR11E105KA99	yes	yes
C2,C3	2	capacitor	0.1μF	±10%		murata	GRM188R11E104KA01D	yes	yes
C7	1	capacitor	1000pF	±10%		murata	GRM188R11E102KA01	yes	yes
C8	1	capacitor	0.01μF	±10%		murata	GRM2192C1H103JA01D	yes	yes
R1	4	resistor	1ohm	±5%		rohm	MCR10EZHFL1R00	yes	yes
R2,R4,R6	3	resistor	1kohm	±5%		rohm	RK73B1JT102J	yes	yes
R3,R5	2	resistor	10kohm	±5%		rohm	RK73B1JT103J	yes	yes
SW1-SW4	1	Switch				MIYAMA	MS-621-A01	yes	yes
TP1-TP12	9	Test points				MAC8	ST-1-3	yes	yes
D2	1	zener diode				ON Semiconductor	1SMA5930BT3G	Yes	yes

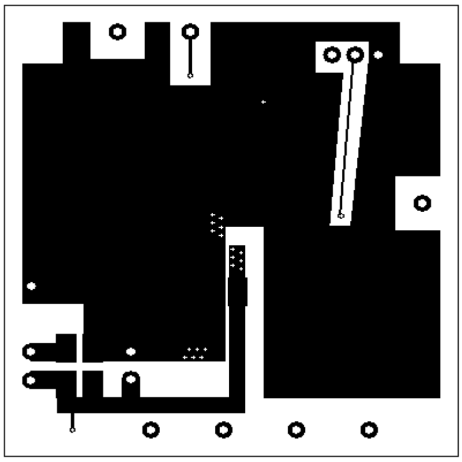
Evaluation Board PCB Design

50mm



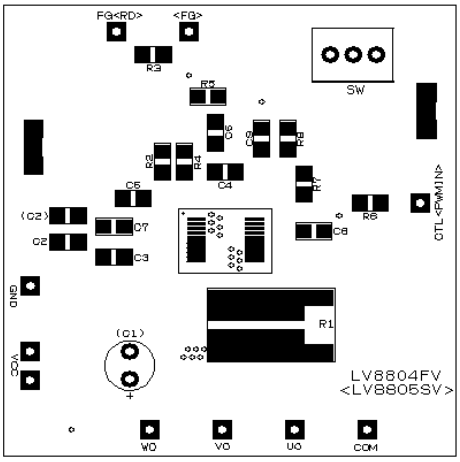
(Top side/ Pattern)

50mm

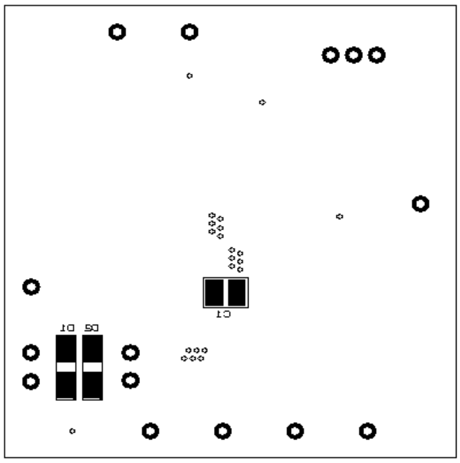


50mm

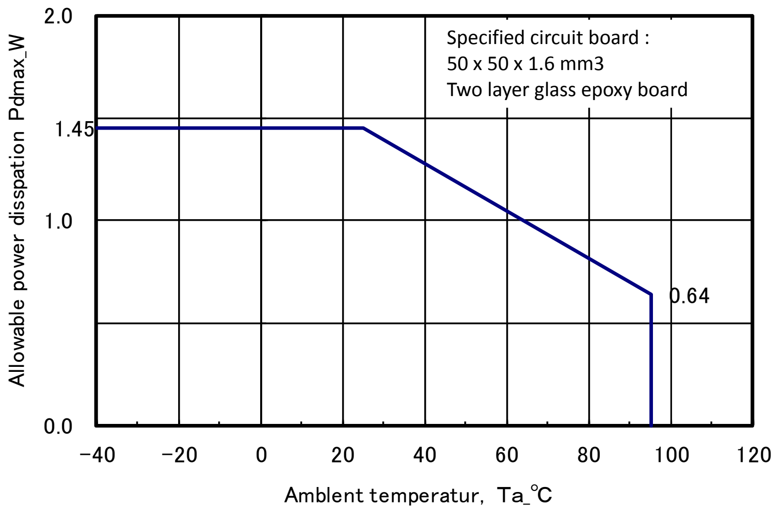
(Back side/ Pattern)



(Top side/ Resist&Silk)



(Top side/ Resist&Silk)



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