CS51031DEMO/D

Demonstration Note for CS51031

A 5–12 V In, 3.3 V/7 A Out Buck Regulator Using the CS51031 Fast PFET Buck Controller

ON Semiconductor®

http://onsemi.com

DEMONSTRATION NOTE

Description

The CS51031 Demonstration Board is a 5–12 V in, 3.3 V out DC/DC converter that delivers 7 A. It monitors Vcc and output voltage ripple to control the PWM and uses a 1.0 A power driver for quick, efficient switching of the gate of a discrete PFET. Utilizing buck topology, this demonstration board delivers excellent performance and protection and represents an extremely low cost solution. The CS51031 Buck Regulator responds to current transients in a very short period of time, providing a constant output voltage. The CS51031 provides hiccup mode short–circuit protection, eliminating the expense of a current sense resistor. The components and layout on the CS51031 demo board have been optimized to deliver superior performance and price in the hands of every motherboard manufacturer. To assist quick and simple evaluation, two switchable 3.5 A resistive loads and a Short Circuit switch are onboard. One of the 3.5 A loads is dynamically switchable. The CS51031 Demonstration Board is a two–layer 7″ × 3″ PCB with the DC/DC converter area being 2″ × 2″.

Features

- Provides 7 Amps of Output Current
- Low External Component Count and Solution Cost
- Provides 90% Efficiency Across Wide Current Range
- 5% DC Regulation and 4% AC Regulation
- 3.5 A, 7 A, Short Circuit and Dynamic Loads Onboard
- Hiccup Short Circuit Protection Minimizes Stress on Power Components
- 10 ms Soft Start
- Single P–Channel MOSFET Design
- 220 kHz Switching Frequency for Compact Magnetics
- BNC Connector at Vout Node for Easy Monitoring
- 5 V Supply Input with 4.25 V Undervoltage Lockout

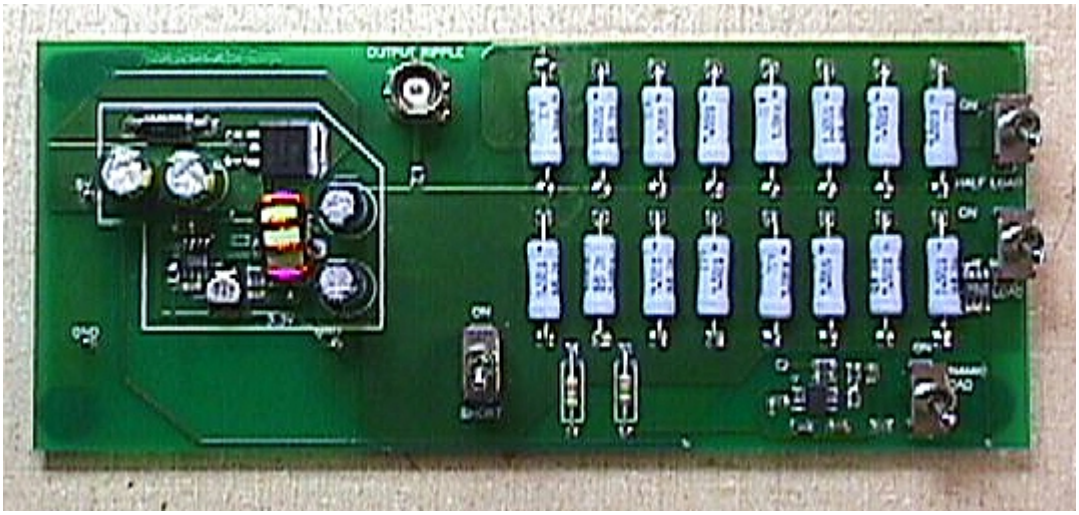


Figure 1. CS51031 Demonstration Board

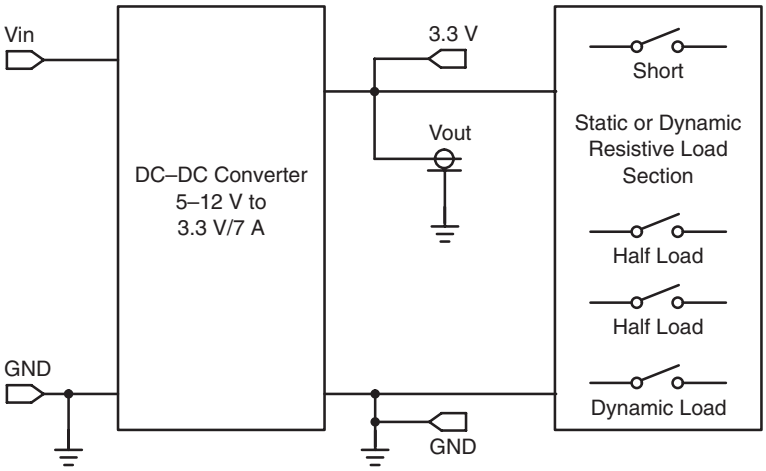


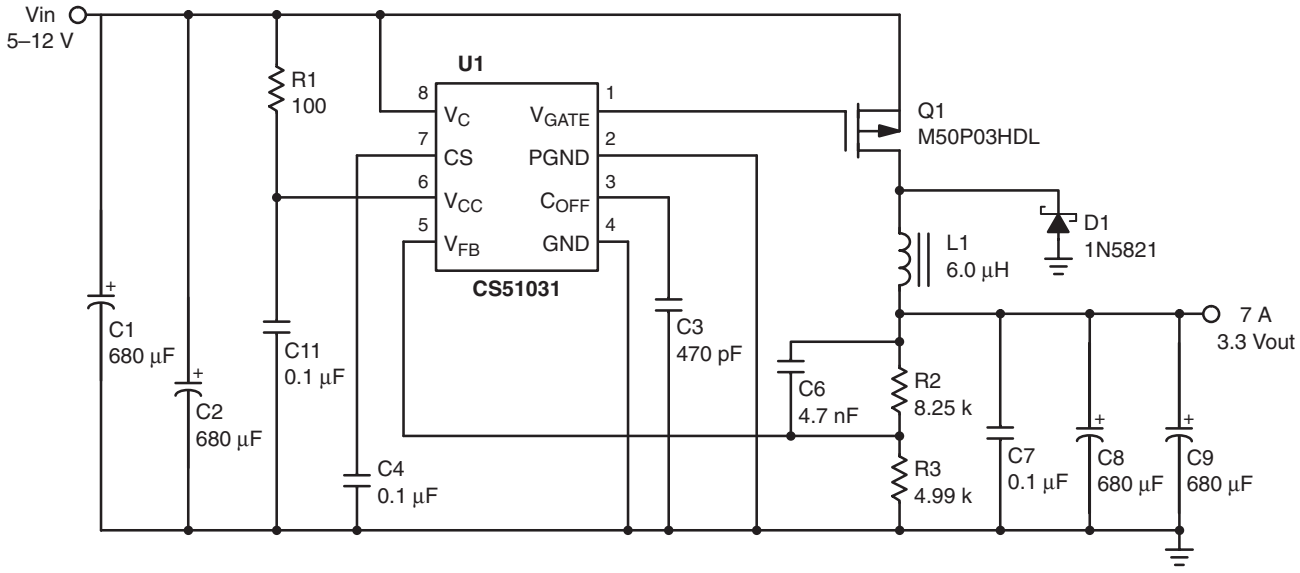
Figure 2. Application Diagram

MAXIMUM RATINGS

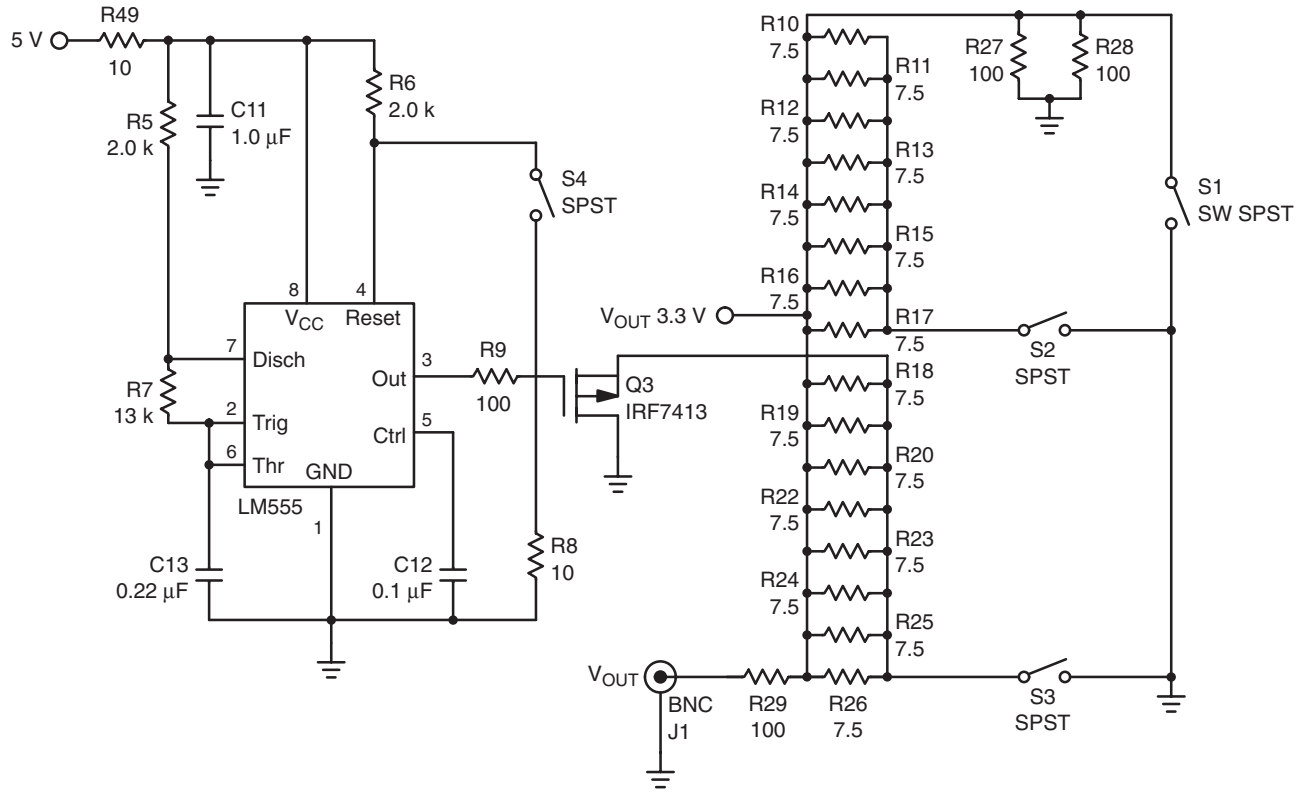
Pin Name	Maximum Voltage	Maximum Current
+5 V	+20 V/–0.3 V	5.8 Amp DC
V_{OUT}	+20 V/–0.3 V	7.0 Amp DC
GND	0 V	7.0 Amp DC

ELECTRICAL CHARACTERISTICS (0.75 V < 5 V_{IN} < 5.25 V, Iout = 0 (No Load), unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Output Voltage	0 < Iout < 7.0 A	3.135 –5.0	3.300 Vref	3.465 +5.0	Volts %
AC Voltage Regulation	3.5 A Load Step	3.201 –3.0	3.300 Vnom	3.399 +3.0	Volts %
Load Transient Response	Time required to settle to ±5% of Vout	–	60	100	μs
Ripple and Noise	0 < Iout < 7.0 A	30	40	50	mVpp
Load Regulation (DC)	0 < Iout < 7.0 A	5.0	20	50	mV
Line Regulation	Iout = 7.0 A	–	3.0	10	mV
Switching Frequency	0 < Iout < 7.0 A	195	215	235	kHz
Duty Cycle (Positive)	Measure (TON/T) × 100 of Switching FET during load transient response 0 < Iout < 7.0 A	3.3	–	80	%
Efficiency P(Vout)/P(5 Vin)	Iout = 7.0 A Iout = 0.5 A	80 –	85 45	90 50	% %
+5 V Start Threshold	Switching	4.2	4.4	4.6	V
+5 V Stop Threshold	Not switching	4.065	4.300	4.515	V
Hysteresis	Start – Stop	65	130	200	mV
Power–Up/Soft Start Time	0 < Iout < 7.0 A	0.5	1.0	3.0	ms



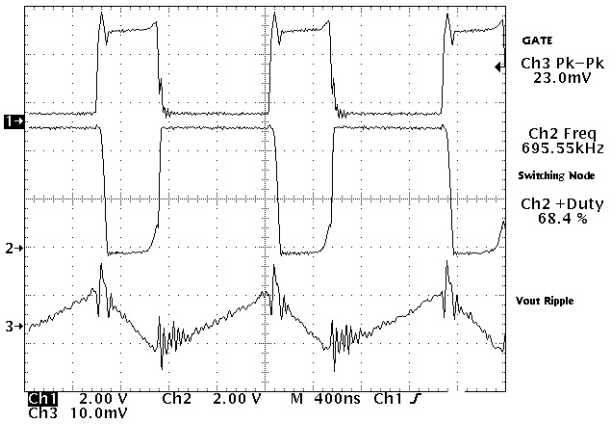
Buck Regulator Circuitry



Test Circuitry

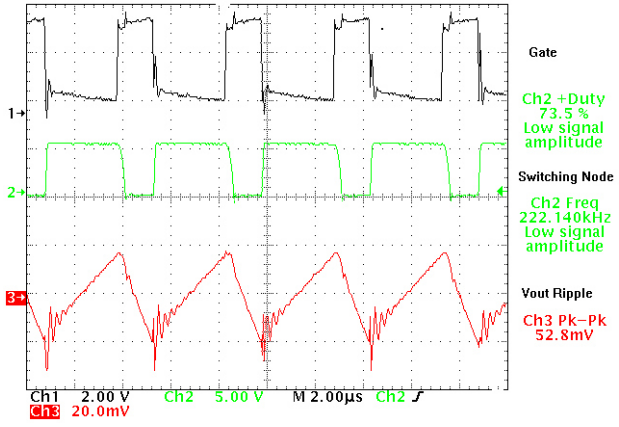
Figure 3. Demonstration Board Schematic

TYPICAL OSCILLOSCOPE WAVEFORMS



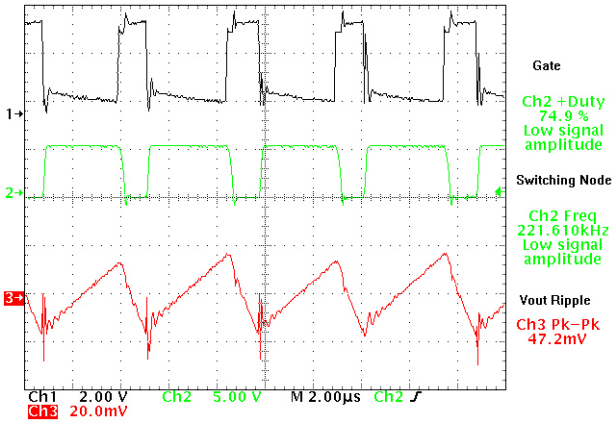
Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

Figure 4. CS51031 Demonstration Board Voltage Waveforms During Normal Operation (Discontinuous Mode), Load Current = 100 mA



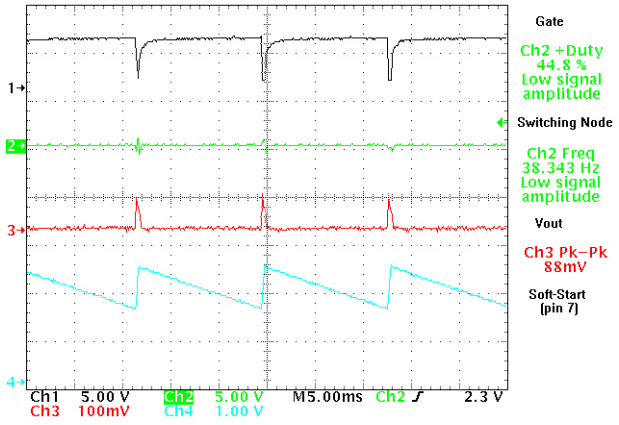
Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

Figure 5. CS51031 Demonstration Board Voltage Waveforms During Normal Operation, Load Current = 3.5 A



Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

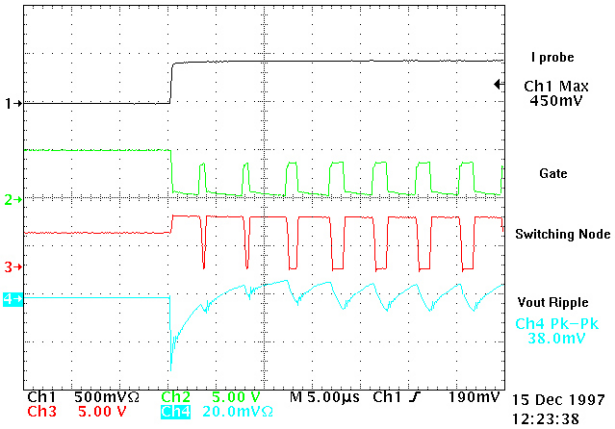
Figure 6. CS51031 Demonstration Board Voltages During Normal Operation, Load Current = 7.0 mA



Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = V_{OUT}
Trace 4 = Soft Start Pin (Pin 5)

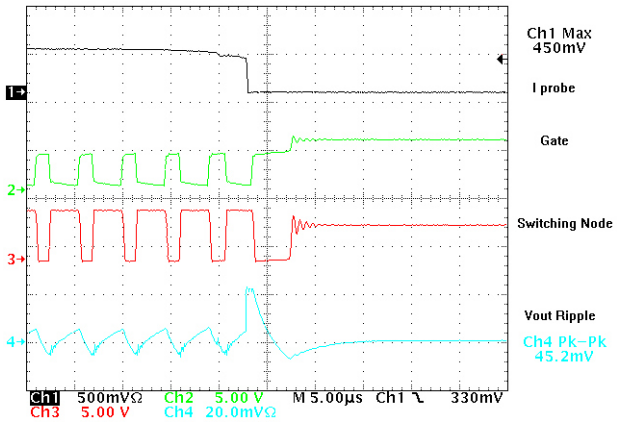
Figure 7. CS51031 Demonstration Board Voltage Waveforms During Hiccup Mode Short−Circuit Operation

TYPICAL OSCILLOSCOPE WAVEFORMS



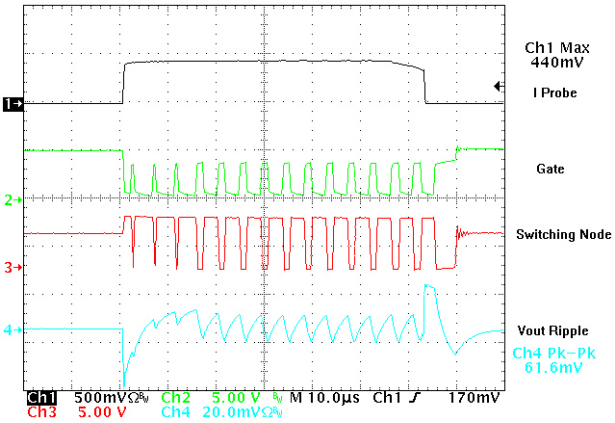
Trace 1 = Load Current 0.5 A/div.
Trace 2 = V_{OUT} Ripple
Trace 3 = FET Gate
Trace 4 = Inductor Switching Node

Figure 8. CS51031 Demonstration Board Voltage Waveforms During a 100 mA to 3.5 A Load Transient



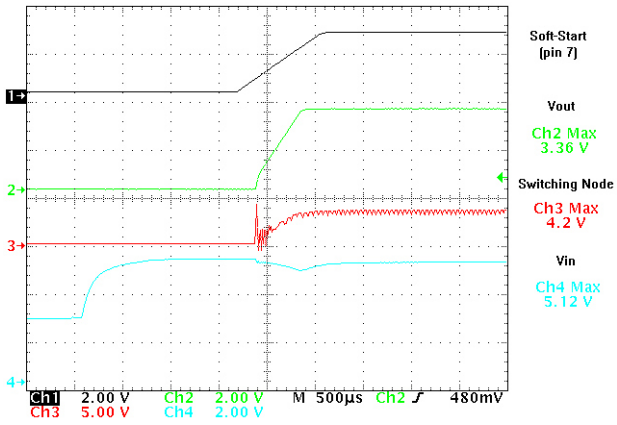
Trace 1 = Load Current 0.5 A/div.
Trace 2 = Gate
Trace 3 = Inductor Switching Node
Trace 4 = V_{OUT} Ripple

Figure 9. CS51031 Demonstration Board Voltage Waveforms During a 3.5 A Load to 100 mA



Trace 1 = Load Current = 500 mV
Trace 2 = Gate
Trace 3 = Inductor Switching Node
Trace 4 = V_{OUT} Ripple

Figure 10. CS51031 Demonstration Board Voltage Waveforms During a 3.5 A Load Transient



Trace 1 = Soft Start
Trace 2 = V_{OUT}
Trace 3 = Switching Node
Trace 4 = V_{IN}

Figure 11. CS51031 Demonstration Board Voltage Waveforms During Power Up

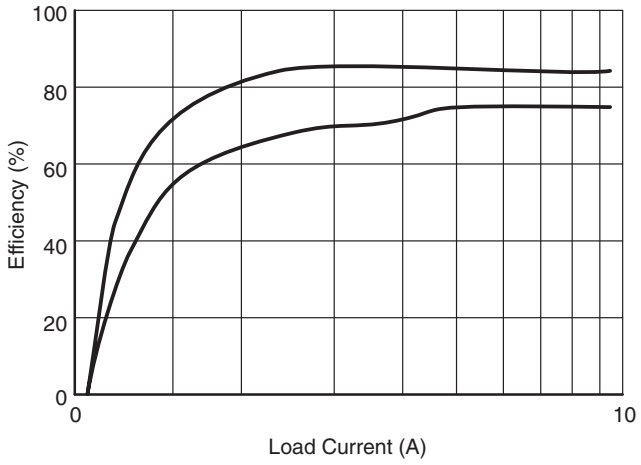


Figure 12.

ELTEST (AUTOMATED POWER SUPPLY TEST SYSTEM) DATA

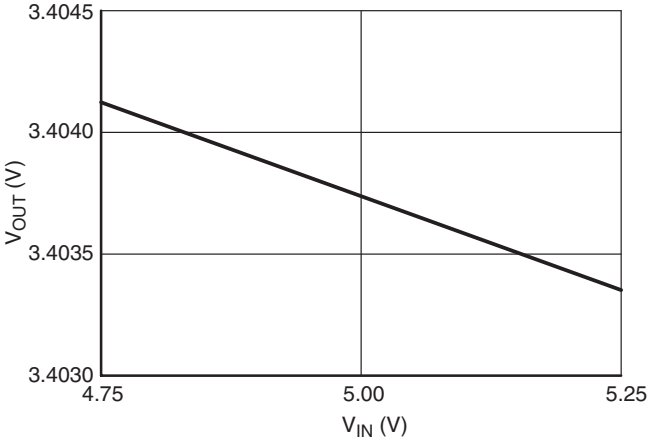


Figure 13. Demonstration Board Line Overvoltage Test 4.75 V < +5 V_{IN} < 5.25 V

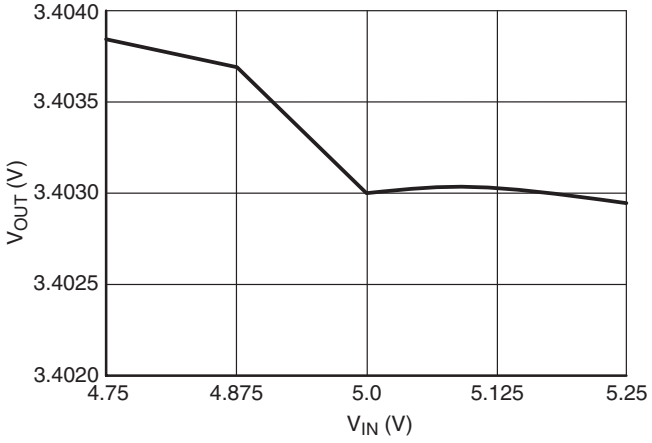


Figure 14. Demonstration Board Line Regulation Test 4.75 V < +5 V_{IN} < 5.25 V

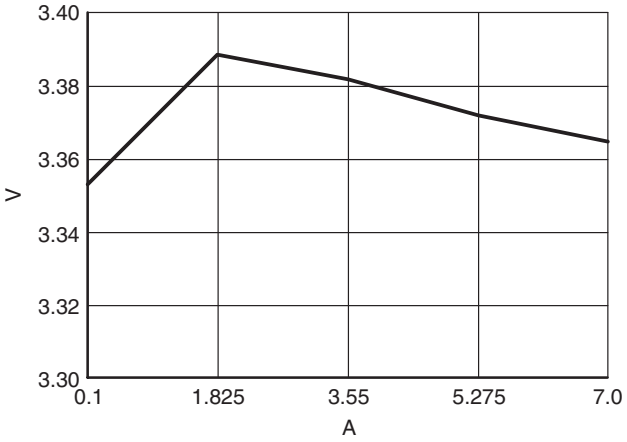


Figure 15. Demonstration Board Load Regulation Test 0.1 A < I_{LOAD} < 7.0 A

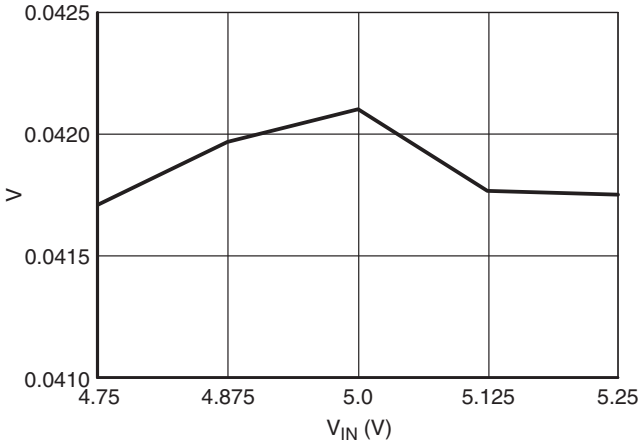


Figure 16. Demonstration Board Ripple Voltage Amplitude Test, 4.75 V < +5 V_{IN} < 5.25 V

OPERATION GUIDELINES

The CS51031 Demonstration Board is configured to exhibit all the unique performance features of the CS51031 Buck Controller IC.

- The +5 V and GND input terminals are located on the left side of the board, the Vout pin is next to the toroid and output GND is just to the right and below the Vout pin.
- The Output Ripple BNC connector is between the DC/DC convertor Section and Loads.
- The Half Load Switches S2 and S3 are on the right end of the board. These switches each connect a 3.5 A Load to the Convertor.
- The Short Circuit Switch S1 is in the center bottom of the Board. When on, the Convertor Output is grounded.
- The Dynamic Load Switch S4, located near the lower right enables a 555 Timer + FET circuit which parallels the Half Load Switch S2. When on, 3.5 A is switched on and off rapidly. This demonstrates the rapid reaction and efficient load handling of the Convertor.

THEORY OF OPERATION

Control Method

In this demonstration board, the output is controlled by the CS51031, which drives a PFET to step the input voltage down to the desired level. This output is generated using a non–synchronous buck topology that utilizes a constant frequency. The CS51031 regulates the 3.3 V output by adjusting the duty cycle of the switch to maintain regulation. A special digital control scheme eliminates the need for a traditional feedback loop with internal error amplifier. This significantly simplifies the design and operation of the power solution by removing the complex analysis and design in compensating the feedback loop. The conversion efficiency for the power solution will not be as high as a fully synchronous design. A non–synchronous converter will typically have efficiencies in the mid 80% range. Replacing the Schottky diode with a synchronous FET will increase the converter efficiency by 3% to 7%. Efficiency gains are significant as the output voltage becomes lower and the diode is on for a longer duration each cycle.

Startup

The CS51031 has an externally programmable soft start feature that controls the rate of output voltage increase upon initial powerup as well as following fault conditions. This prevents voltage overshoot at the output, which in turn protects devices connected to Vout. The soft start capacitor Css, along with soft start Charge Current Ics sets the rate of voltage rise. With the Css value of 0.1 μF, the Soft Start time is approximately 10 ms.

Fault Operation

When the demonstration board output Vout is shorted to ground, and the CS51031 is placed in hiccup mode, whereby gate pulses are delivered to the PFET as the soft–start capacitor charges, and cease while it discharges. The typical charge time is 3 ms, while the discharge lasts for 90 ms typically. If the short–circuit condition persists, the regulator output will not achieve the 1 V low Vfb comparator threshold before the soft–start capacitor is charged to its upper 2.5 V threshold. Then the cycle will repeat itself until the short is removed. If the short–circuit condition is removed, the output voltage will rise above the 1 V threshold, preventing the FAULT latch from being set, and allowing normal operation to resume.

The CS51031 implements short circuit protection by means of a lossless short circuit protection scheme. In this scheme, the short circuit comparator senses the output voltage and initiates hiccup operation when this voltage decreases below a pre–set threshold, due to the short circuit condition.

DESIGN GUIDELINES

Component Selection

Magnetics: This design uses only one inductor. This provides a ‘low–pass filter’ to the output switching ripple; to turn the AC to DC. The designer must be very aware of maximum current expected across the inductor. Switching frequency must also be considered in the core selection. Simple ferrite toroids, such as supplied by Koolμ and Micrometals can withstand the 100 k–1 MHz frequencies selected. The number of turns to use is an exercise in tradeoff between output voltage ripple levels and response time to load transients. An additional inductor may be inserted at the Vin connection to quiet the input current spikes seen by the supply sourcing Vin.

Input and Output Bulk Capacitors: Input caps must provide the maximum ripple current of the Switched input current. This can be initially estimated as one–half of the output current. Output caps control the output ripple voltage. This voltage is simply the inductor’s ripple current, multiplied by the ESR of the capacitors. Favorite tricks for ESR reduction are paralleling several caps and, if budget allows, lower ESR tantalums are available from TDK and AVX.

Semiconductors: The switching FET selection is primarily based upon maximum voltage and current ratings. Also to be considered is the R_{DSon}. This determines the power burned in the FET and must be removed. Too little

copper on the PC board to wick out this heat is a common cause of failure. In higher power convertors, heat sinks may be considered to keep the footprint down. The Schottky diode must also be selected by maximum current rating and voltage levels present. In this design, the continuous max is 7 A with peaks of 10 A. Average current is approximately (Vout/Vin)*Imax, so typically (3.3 V/5 V)*7 A = 2.3 A, so a 20 V, 5 A Schottky is a good choice.

Formulae

A few useful formulae for Buck architecture:

Duty Cycle: DTC = (Vout + Vdiode)/(Vin + Vdiode) = (3.3 + 0.5)/(5.0 + 0.5) = 69% (nominal)

Diode Current: Idiode = (1 – DTC) * $Iout_{max}$ = (1 – 0.69) * 7 A = 2.17 A (average max)

Power Loss: $P_{FET} = I^2 * R_{DSon} * DTC = 49 * 0.025 * 0.69$ = 845 mW

Thermal Data: Board Under Load

Tamb = 23°C Iout = 7.0 A	Vin = 12 V	Vin = 5.0 A
L1	120°C	82°C
D1 (1N5821)	108°C	80°C
Q1 (M50P03)	106°C	97°C
C1/C2	67°C	67°C
U1 (CS51031)	60°C	60°C

Board should only be run with Dynamic Load at Elevated Temperatures.

BILL OF MATERIALS

Ref. Des	Qty	Description	Manufacturer	Manufacturer P/N	Telephone
DC/DC Converter					
C1, C2, C8, C9	4	680 μF/10 V Electrolytic	Digikey	P5641	(800) 344–4539
C3	1	470 pF CAP 1206	Digikey	PCC471BCT–ND	(800) 344–4539
C4, C7	2	0.1 μF CAP 1206	Digikey	PCC104BCT–ND	(800) 344–4539
C6	1	4.7 nF CAP 1206	Digikey	PCC472BCT–ND	(800) 344–4539
C14	1	100 μF CAP	Digikey	PCE2039CT–ND	(800) 344–4539
D1	1	DIODE–FLYBACK	ON Semiconductor	1N5821	(401) 885–3600
L1	1	2.56–3.01 μH	XFMRS	S26–10006	(317) 834–1066
Q2	1	P–FET Dpak2	ON Semiconductor	MTB50P03HDL	(401) 885–3600
R1	1	10 Ω, RES. 1206	Digikey	P10 ECT–ND	(800) 344–4539
R2	1	8.25 kΩ RES. 1206	Digikey	P8.25K FCT–ND	(800) 344–4539
R3	1	4.99 kΩ RES. 1206	Digikey	P4.99K FCT–ND	(800) 344–4539
U1	1	CS51031 Controller	ON Semiconductor	CS51031YDR8	(401) 885–3600
Tp1–4	4	Turret Pin	Newark	40F6023	(800) 463–9275
Bumpons	4	Bumpons	Digikey	SJ5003–0–560	(800) 344–4539
Test Circuitry					
C11, C12	2	0.1 μF CAP 1206	Digikey	PCC104BCT–ND	(800) 344–4539
C13	1	0.22 μF CAP 1206	Digikey	PCT6224CT–ND	(800) 344–4539
J1	1	BNC Conn.	Farnell	583–558	
Q3	1	NFET, SO8	Digikey	IRF7413	(800) 344–4539
R4, F8	2	10 Ω 1206	Digikey	P10 ECT–ND	(800) 344–4539
R5, R6	2	2.0 kΩ 1206	Digikey	P2K ECT–ND	(800) 344–4539
R7	1	13 kΩ 1206	Digikey	P13K ECT–ND	(800) 344–4539
R9, R29	2	100 Ω 1206	Digikey	P100 ECT–ND	(800) 344–4539
R10–R20, R22–R26	16	7.5 Ω 3 W	Digikey	P7.5W–3BK	(800) 344–4539
S1–S4	4	Switch	Digikey	CKN1004	(800) 344–4539
R27, R28	2	100 Ω Res. 25 W	Digikey	100 Q BK–ND	(800) 344–4539
U2	1	LM 555 Timer	Digikey	LM 555 CM–ND	(800) 344–4539
TP5	1	Turret Pin	Newark	40F6023	(800) 463–9275

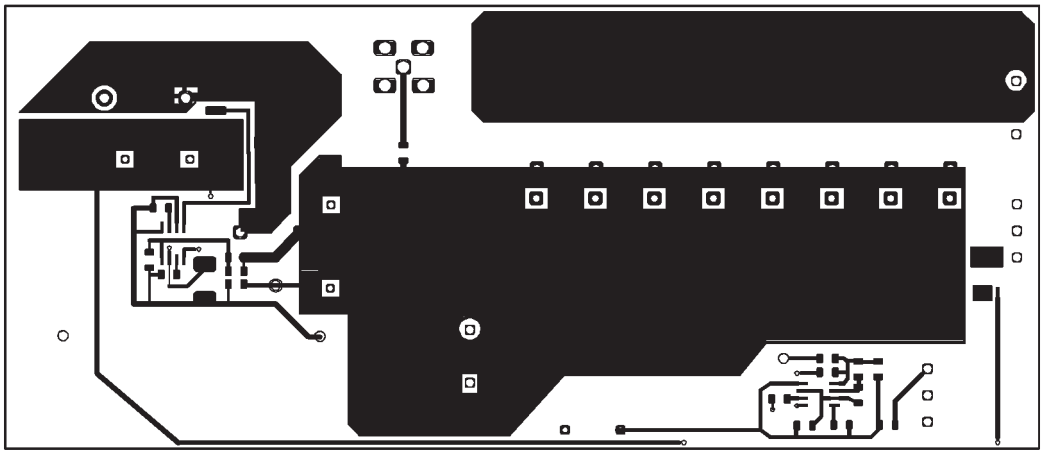


Figure 17. Top Layer

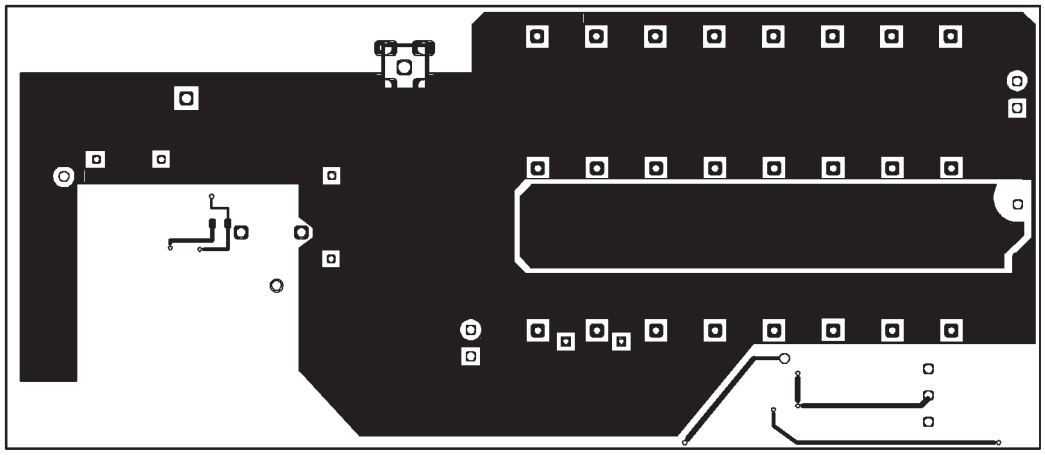


Figure 18. Bottom Layer

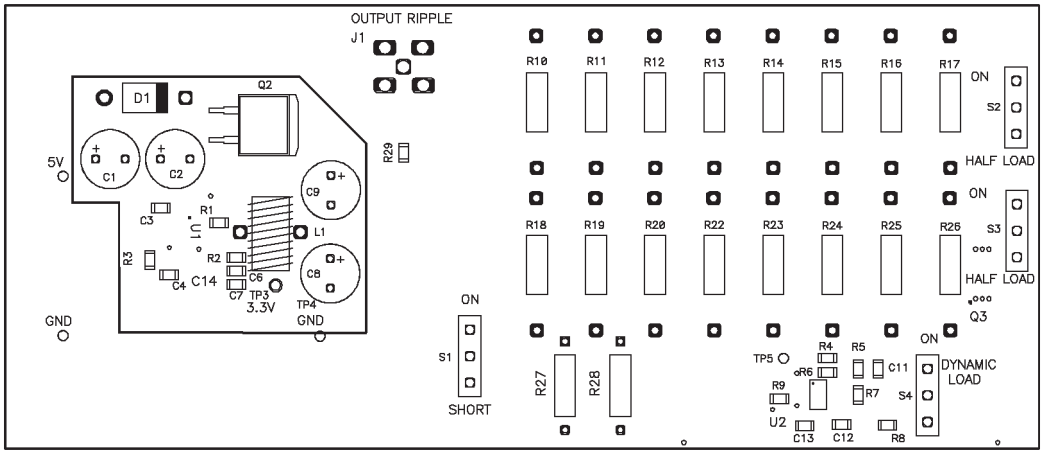


Figure 19. Silk Layer

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051
Phone: 81–3–5773–3850
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.