

# ON Semiconductor

## Is Now

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## Basic Power Topology

The principle of the Discontinuous Flyback converter is fairly simple (see Figure 2):

While the power MOSFET is in the ON state, the input voltage source is directly applied to the primary of the coupled inductor. Current ramps linearly in the primary since no current can flow in the secondary due to the blocking diode on the secondary. Under these conditions the transformer is really functioning as a coupled inductor. This results in accumulated energy in the core. During this time all of the current needed to supply the load is provided by the output capacitor since the blocking diode is reverse biased. The voltage stress on the output Diode during this time due to transformer action is:

$$V_{in} \frac{N_s}{N_p} + V_{out}$$

When the MOSFET turns OFF, the voltage on the secondary is forced to flip and conduction to the load commences. Since the output voltage is fixed with the output capacitance, current ramps down linearly flowing both to the load and the output capacitor. The voltage stress on the MOSFET Drain during this time due to transformer action is:

$$V_{in} + V_{out} \frac{N_p}{N_s}$$

Once the current reaches zero, the MOSFET Drain voltage falls toward  $V_{in}$ . Since the magnetizing inductance in series with the MOSFET parasitic Drain-to-Source capacitance forms a tuned circuit a resonance voltage waveform is typically created. That resonance is:

$$\frac{1}{2\pi\sqrt{L_{pri}C_{ds}}}$$

It is advantageous to select the capacitance, inductance and operating frequency to coincide with the lowest portion of this resonance just prior to start of a new switching cycle (See figure 3). This will minimize turn ON switching loss in the system.

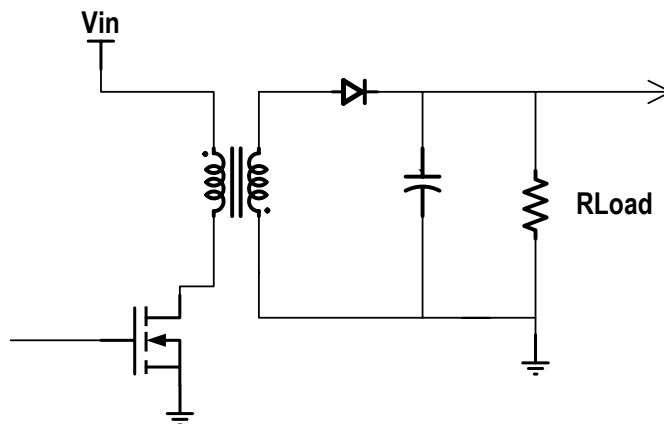
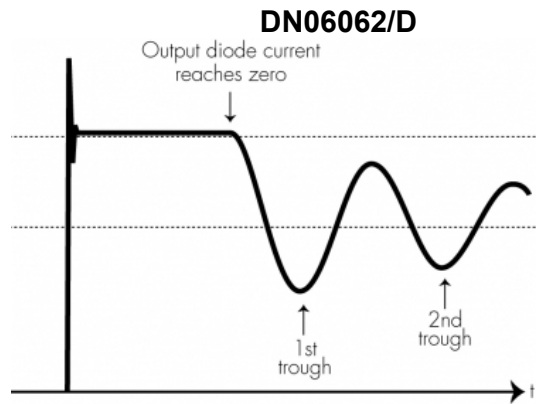


Figure 2 – Flyback Operation



**Figure 3 – MOSFET Drain Voltage**

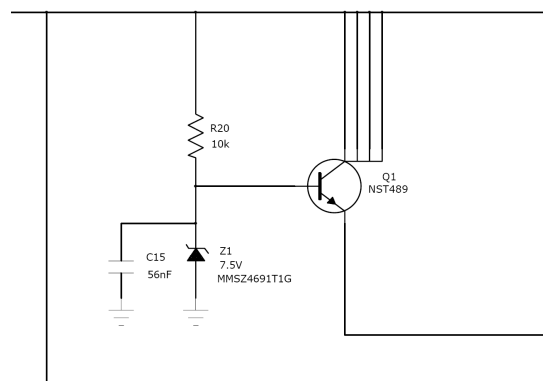
The initial spike seen on the Drain is a function of leakage inductance in series with the Drain-to-Source capacitance of the MOSFET. The resonance is:

$$\frac{1}{2\pi\sqrt{L_{leak}C_{ds}}}$$

C16 and R11 are installed in series across the transformer primary winding to snub this turn OFF waveform. Similar snubbers are installed across the output rectifiers to reduce local leakage inductance based ringing.

### Input Regulator Regulation

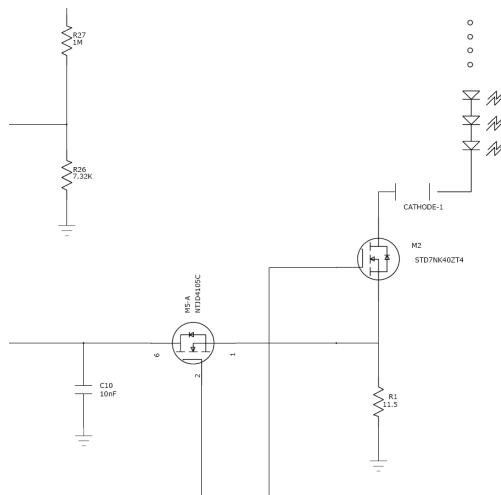
The Circuit in Figure 4 is used to create a regulated 7Volts for the NCP1294 to operate. The input regulator is a simple Emitter Follower with a Zener diode to set the base voltage. A three winding transformer could be used to back bias this supply, but care must be taken to understand the output variation on the winding voltage since the main output id current regulated.



**Figure 4 – Input Regulator**

### Current Loop

R11 is used to sense the inductor current and is fed to the FB pin of the NCP1294. When not in dimming mode, M2 and M5-A FETs are in the ON state allowing basic closed loop operation. Closing the voltage loop around R1 makes the output current  $1.26V/11.5\Omega = 109.5mA$ . C9 is the integrating capacitor that stabilizes the main current loop.



**Figure 5 – Current Sense**

### Input Voltage Feed-Forward Ramp

R23 and C3 form an RC network that sets the ramp voltage for the internal PWM loop. Deriving the voltage from  $V_{in}$  is beneficial to line rejection since perturbations on the input are directly offset in the modulator stage.

### Soft Start

Flyback power converters must be soft started to avoid saturation level currents from developing in the primary winding. This is achieved by feeding the soft start voltage into the Iset pin of the NCP1294. This allows for a variable current limit trip that increases as the Soft Start Capacitor charges at start up.

### PWM Dimming Circuit

The PWM dimming circuit is comprised of a number of MOSFET switches that alternate current in the LED load from a fixed regulation level (110mA Nominal) to zero current. Variation of the duty cycle of the switches results in reduction in current that is linear with respect to Duty Cycle. The nominal rate of dimming is between 500Hz and 1.5KHz.

Dimming is done by opening the LED current path as well as the feedback path. Also switching is halted to prevent additional energy during LED OFF periods.

The TTL level PWM dimming signal is passed through M6-A gate which feeds an inverting stage comprised of M4-B and M4-B driver transistors. R17 prevents shoot through currents in the driver stage. The inverted dimming signal turns off M2 which opens the LED current path. Simultaneously, M5-A is turned OFF which prevents discharge of C10 during the open current loop stage. This stores the feedback voltage level during the LED OFF period, thus preventing the error amplifier from railing.

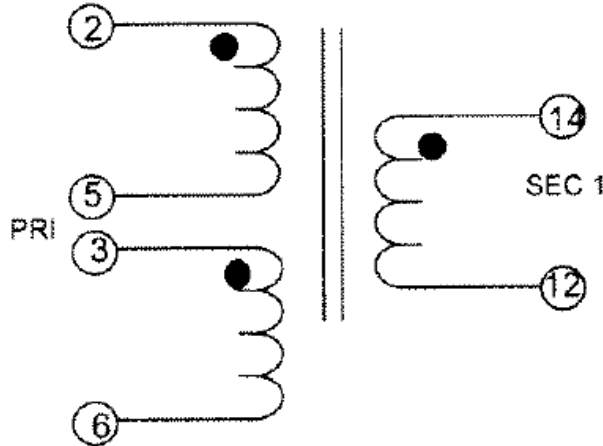
The dim signal is also sent to the gate of M6-B which pulls the FF pin to  $V_{ref}$  voltage. This disable switching while avoiding fault conditions during the LED OFF period.

**Transformer Design**

See Figure 6

**Electrical Specificaitons**

DC Resistance (25C)	2-6 (2+3,5+6) 12-14	0.018 Ohms Max 0.55 Ohms Max	
Inductance	2-6 (2+3,5+6) 12-14	5uH +/- 10% 320uH +/- 10%	100mVAC, 0 ADC 100mVAC, 0 ADC
Leakage Inductance	2-6 (2+3,5+6), short 12-14 12-14 2-6, short (2+3,5+6)	400nH Max 8uH Max	100KHz, 100mVAC 100KHz, 100mVAC
Primary Saturation Current	2-6 (2+3,5+6)	9 A Min	<20% drop in Lpri
Turns Ratio	(14-12):(2-5) (14-12):(3-6)	8:1 +/- 1% 8:1 +/- 1%	



**Figure 6 – Flyback Transformer Specifications**

**Protection Features -**

**Input UV Lockout**

R19 and R25 and C2 set the Input Under Voltage Lockout level. UVLO is calculated by:

$$V_{uvlo} = V_{uvref} \left( 1 + \frac{R19}{R25} \right)$$

**Pulse by Pulse Current Limit**

R12 is used to sense an limit primary peak current. R13 and C6 are used to filter leading edge current spike created by leakage inductance and gate driver currents. The Iset voltage is set with the R21 and R4 divider from Vref. The peak current trip point is calculated by:

$$I_{pk} = \frac{V_{ref}(R4)}{(R21 + R4)} \frac{1}{R12}$$

**LED Open Circuit Protection**

Since this is a current regulated loop, open circuit voltage could be a potential problem if it were not specifically limited. This design utilizes the OV pin of the NCP1294 and the R27 and R26 divider ratio. Vopen loop is calculated by:

$$V_{ov} = V_{ovref} \left( 1 + \frac{R27}{R26} \right)$$





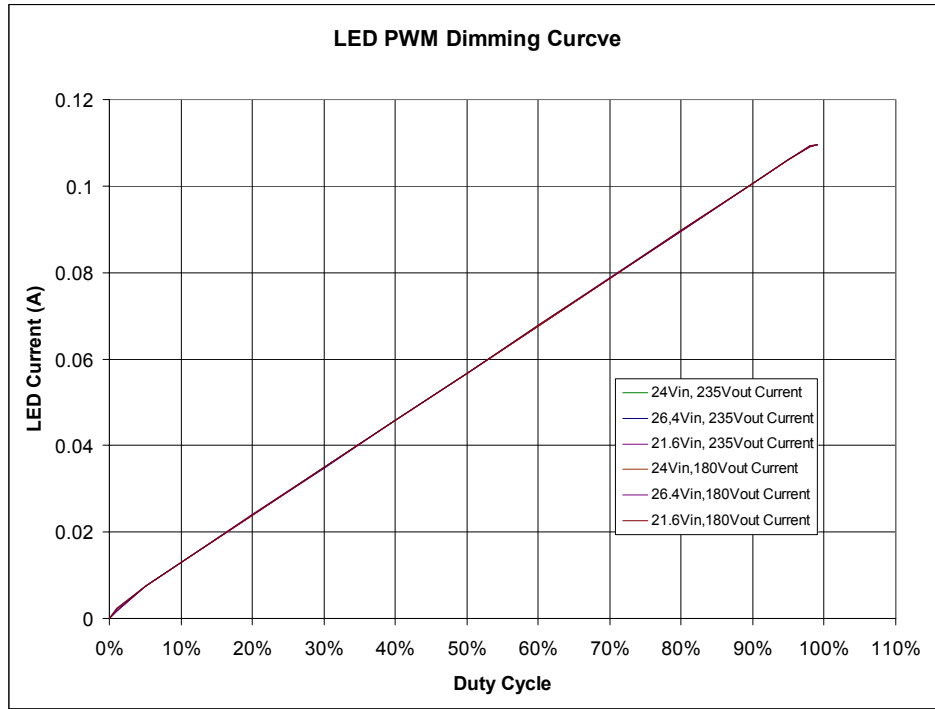
**DN06062/D**

Qty	Reference	Value	Part Number	Description	Manufacturer	PCB DECAL
1	T1		750311176	Flyback Transformer	Wurth	750311176-CUT
1	C5	0.1uF	ECJ-1VB1C104K	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C8	1.0uF	ECJ-1VF1E105Z	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C16	1.5nF	GRM188R72A152KA01D	Ceramic Chip Capacitor	Murata	0603CAP
1	C10	10nF	ECJ-1VB1C103K	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C6	1nF	GRM188F51H102ZA01D	Ceramic Chip Capacitor	Murata	0603CAP
1	C4	1uF	ECJ-1VF1E105Z	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C2	1uF	ECJ-1VF1E105Z	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C1	470pF	ECJ-1VC1H471J	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C9	56nF	ECJ-1VB1C563K	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C15	56nF	ECJ-1VB1C563K	Ceramic Chip Capacitor	Panasonic	0603CAP
1	C3	1.0nF	ECJ-1VC1H102J	Ceramic Chip Capacitor	Panasonic	0805CAP
1	C11	20pF	ECJ-2VC2D220J	Ceramic Chip Capacitor	Panasonic	0805CAP
1	C12	20pF	ECJ-2VC2D220J	Ceramic Chip Capacitor	Panasonic	0805CAP
1	C19	20pF	ECJ-2VC2D220J	Ceramic Chip Capacitor	Panasonic	0805CAP
1	C21	0.1uF	UVR2F010MED	Ceramic Chip Capacitor	Murata	1206CAP
1	C13	10uF	GMK316F106ZL-T	Ceramic Chip Capacitor	Panasonic	1210CAP
1	C7	1000uF	ECA-1VM102B	Electrolytic Capacitor	Panasonic	ECA 12.5D
1	C14	1uF	UPW2V010MPH	Electrolytic Capacitor	Nichicon	ECA 10D
1	D1		MBRS3200	DIODE, SCHOTTKY	ON Semiconductor	SMB
1	D3		MBRS3200	DIODE, SCHOTTKY	ON Semiconductor	SMB
1	D4		MBRS3200	DIODE, SCHOTTKY	ON Semiconductor	SMB
1	Z1	7.5V	MMSZ4691T1G	Zener Diode	ON Semiconductor	MMSZ11T1G_SOD123
1	U1		NCP1294	Enhanced Voltage Mode PWM Controller	ON Semiconductor	SOIC16
1	Q1	NPN	NST489	General Purpose Dual NPN Transistor	ON Semiconductor	TSOP-6
1	M1		NTD12N10T4G	Power MOSFET	On Semiconductor	NTD12N10_DPAK
1	M2		STD7NK40ZT4	Power MOSFET	On Semiconductor	NTD12N10_DPAK
1	M4		NTJD4105C		On Semiconductor	SOT-363
1	M5		NTJD4105C		On Semiconductor	SOT-363
1	M6		NTR4501		On Semiconductor	SOT-363
1	R8	0		Resistor	Vishay / Dale	0603RES
1	R6	1		Resistor	Vishay / Dale	0603RES
1	R20	10k		Resistor	Vishay / Dale	0603RES
1	R22	10k		Resistor	Vishay / Dale	0603RES
1	R19	120k		Resistor	Vishay / Dale	0603RES
1	R27	1M		Resistor	Vishay / Dale	0603RES
1	R17	1k		Resistor	Vishay / Dale	0603RES
1	R10	20K		Resistor	Vishay / Dale	0603RES
1	R5	220		Resistor	Vishay / Dale	0603RES
1	R21	28.7k		Resistor	Vishay / Dale	0603RES
1	R23	41.2k		Resistor	Vishay / Dale	0603RES
1	R4	6.8K		Resistor	Vishay / Dale	0603RES
1	R26	7.32K		Resistor	Vishay / Dale	0603RES
1	R13	80		Resistor	Vishay / Dale	0603RES
1	R25	8K		Resistor	Vishay / Dale	0603RES
1	R14	0		Resistor	Vishay / Dale	1206RES
1	R12	0R05		Resistor	Vishay / Dale	1206RES
1	R1	11.5		Resistor	Vishay / Dale	1206RES
1	R2	150		Resistor	Vishay / Dale	1206RES
1	R3	150		Resistor	Vishay / Dale	1206RES
1	R28	150		Resistor	Vishay / Dale	1206RES
1	R15	1R0		Resistor	Vishay / Dale	1206RES
1	R11	4.99		Resistor	Vishay / Dale	1206RES
1	R32	open		Resistor	Vishay / Dale	1206RES

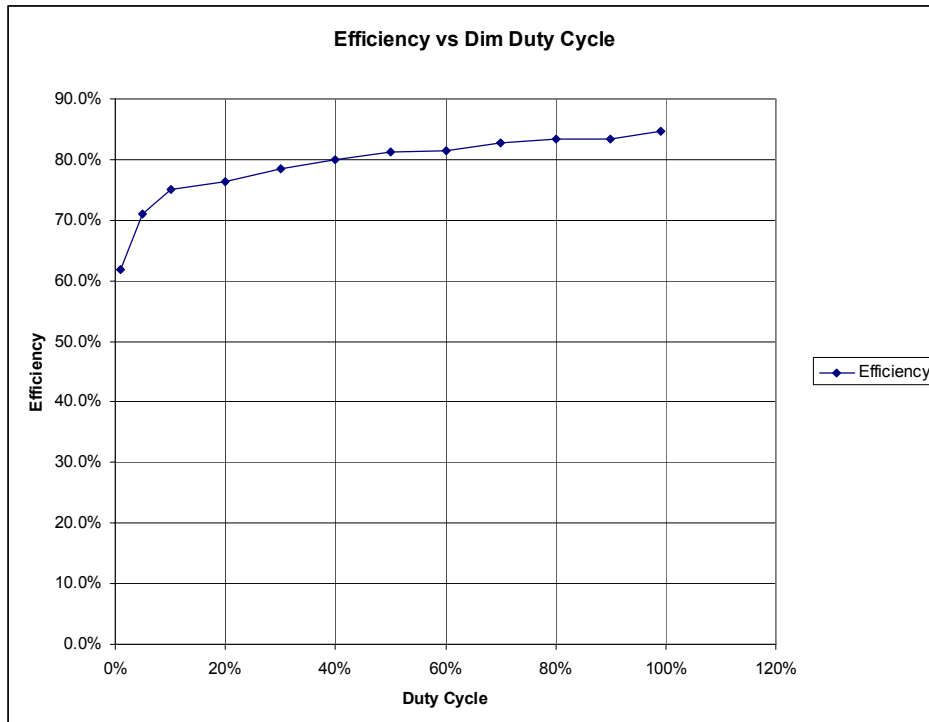
**Table 1 – Bill of materials**

Measurements –

Dimming Curve



Efficiency



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