NCL30081LEDGEVB

3.6 W Flyback 3 LED Step Dimmable Driver Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Overview

This documentation package covers an NCL30081 LED driver for use in a GU10 based LED lamp. The output is mains isolated by double insulation. Maximum input power is 5 W. The ECA (**E**lectronic **C**ircuit **A**ssembly) supports 2 versions; one step dimming and one non-dimming version. The version is controlled through minor bill-of-material changes. The LED current dims in 5 discrete levels sequentially by detecting the interruption of the AC mains briefly (about 1 s) to step the LED current down one level until it cycles back to full current.

Modifications

The value of R_{trim} sets the final output current value along with R_{sense}. R_{trim} is for fine adjustment. The nature of the open loop control makes the current adjustment somewhat iterative based on available standard resistor values and because of the circuit parameters that affect the output current setting.

Line regulation is optimized by the selection of R_{lff}. A line dependent current source creates a line dependent offset on the CS pin to account for propagation delay errors in the peak primary current. Changing the FET or gate driver resistor will also have some effect on the output current.

Since the input power is < 5 W maximum, this falls below the level where power factor or harmonic current requirements are applicable in many countries (e.g. US). In the EU, the harmonic current requirements for IEC61000-3-2 Class C are applicable even at this low power level. Compliance to the Class C requirements is simple with a change of the input capacitor from 4.7 μF to 1 μF. This change limits the input voltage operation to 200–265 V ac because there is insufficient energy storage for the full universal line range.

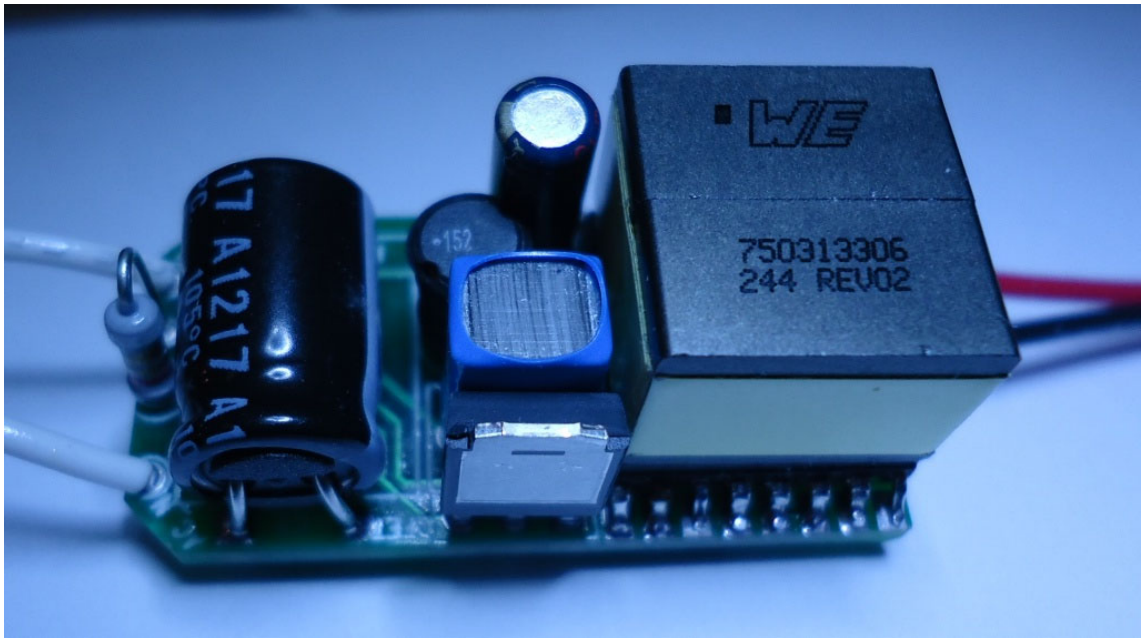


Figure 1. NCL30081LEDG Evaluation Board

THEORY OF OPERATION

Figure 3 portrays the primary and secondary current of a fly-back converter in discontinuous conduction mode (DCM). Figure 2 shows the basic circuit of a fly-back converter.

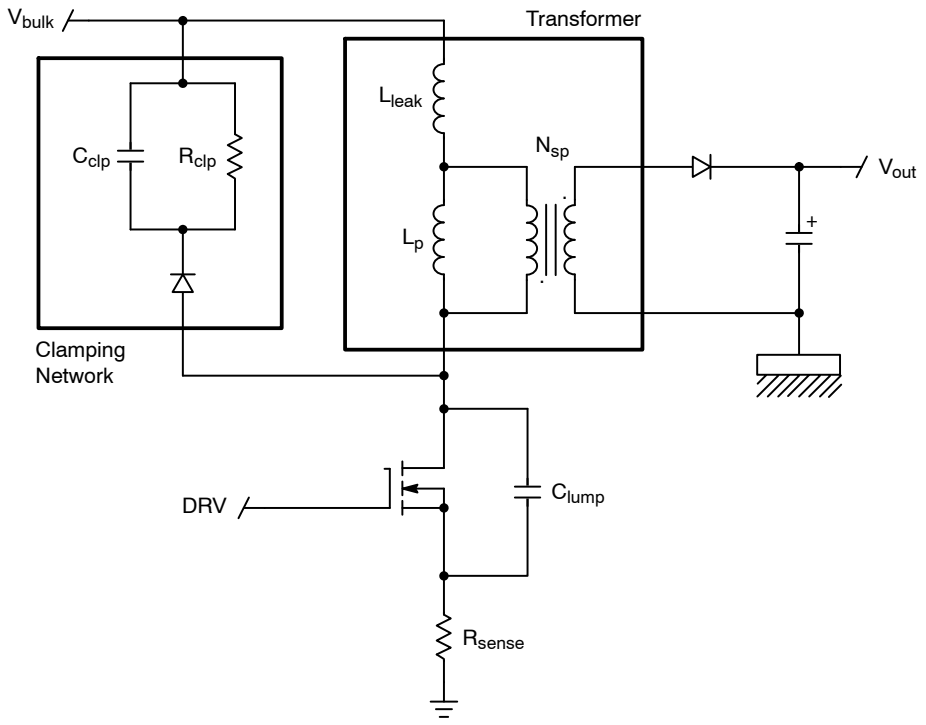


Figure 2. Basic Fly-back Converter Schematic

During the on-time of the MOSFET, the bulk voltage V_{bulk} is applied to the magnetizing and leakage inductors L_p and L_{leak}. The current ramps up.

When the MOSFET is turned-off, the inductor current first charges C_{lump}. The output diode is off until the voltage across L_p reverses and reaches

$$N_{sp}\left(V_{out} + V_f\right)$$

The output diode current increase is limited by the leakage inductor. As a consequence, the secondary peak current is reduced:

$$I_{D,pk} < \frac{I_{L,pk}}{N_{sp}}$$

The diode current reaches its peak when the leakage inductor is reset. Thus, in order to accurately regulate the output current, we need to take into account the leakage inductor current. This is accomplished by sensing the clamping network current. Practically, a node of the clamp capacitor is connected to R_{sense} instead of the bulk voltage V_{bulk}. Then, by reading the voltage on the CS pin, we have an image of the primary current (red curve in Figure 3).

When the diode conducts, the secondary current decreases linearly from $I_{D,pk}$ to zero. When the diode current has turned off, the drain voltage begins to oscillate because of the resonating network formed by the inductors ($L_p + L_{leak}$) and the lump capacitor. This voltage is reflected on the auxiliary winding wired in fly-back mode. Thus, by looking at the auxiliary winding voltage, we can detect the end of the conduction time of secondary diode. The constant current control block picks up the leakage inductor current, the end of conduction of the output rectifier and controls the drain current to maintain the output current constant. We have:

$$I_{out} = \frac{V_{REF}}{2N_{sp}\,R_{sense}} \qquad \textit{(eq. 1)}$$

The output current value is set by choosing the sense resistor:

$$R_{sense} = \frac{V_{ref}}{2N_{sp}\,I_{out}} \qquad \textit{(eq. 2)}$$

From (eq. 1), the first key point is that the output current is independent of the inductor value. Moreover, the leakage inductance does not influence the output current value as the reset time is taken into account by the controller.

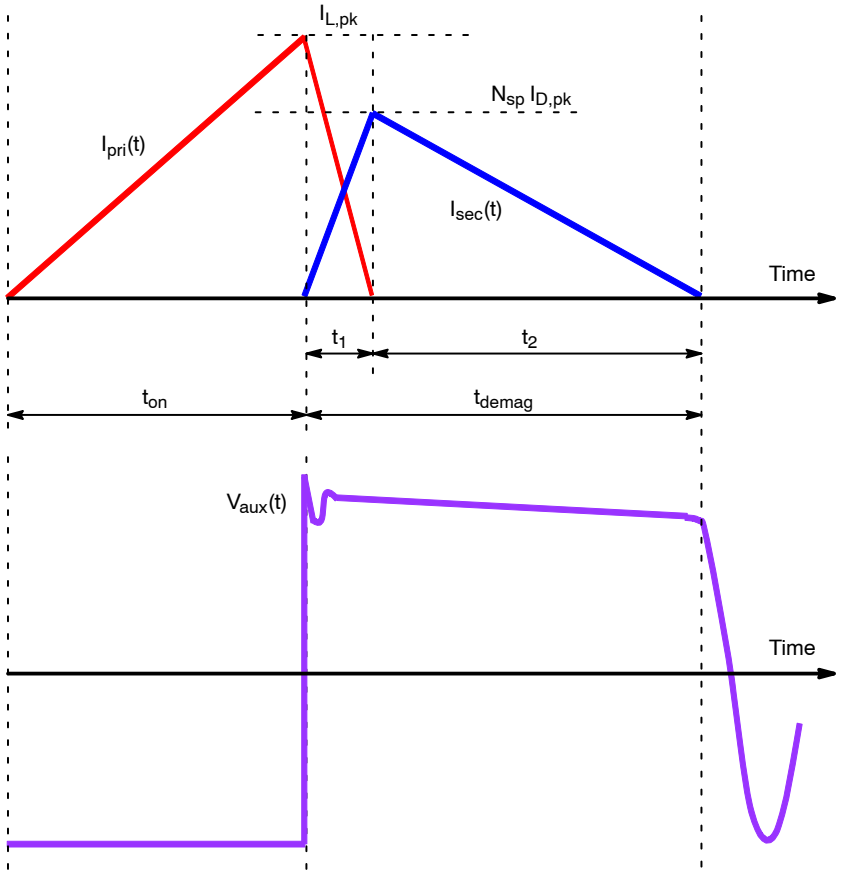


Figure 3. Flyback Currents and Auxiliary Winding Voltage in DCM

At this point the Excel® spreadsheet based design guide will help with many of the calculations.

A trim resistor allows for making fine adjustments to the current limit to set the output current precisely. The LFF circuit will create some error on the CS pin which is adjusted out by proper choice of R_{trim}

SPECIFICATIONS

Table 1. SPECIFICATIONS

Input voltage	90−265 V ac	
Line Frequency	50−60 Hz	
Power Factor	0.5	Typ.
Safety (Designed to meet)	IEC61347-2-13	EU
	UL8750	NA
Optimized Output Voltage Range	9−10.5 V dc	
Output Current	360 mA dc	
Output Ripple	200 mA P-P	
Efficiency	82 %	Typ.
Start Up Time	< 500 ms	
EMI (Conducted)	Class B	FCC/CISPR
Dimensions	34.1 × 17.3 × 16 mm	

SCHEMATIC

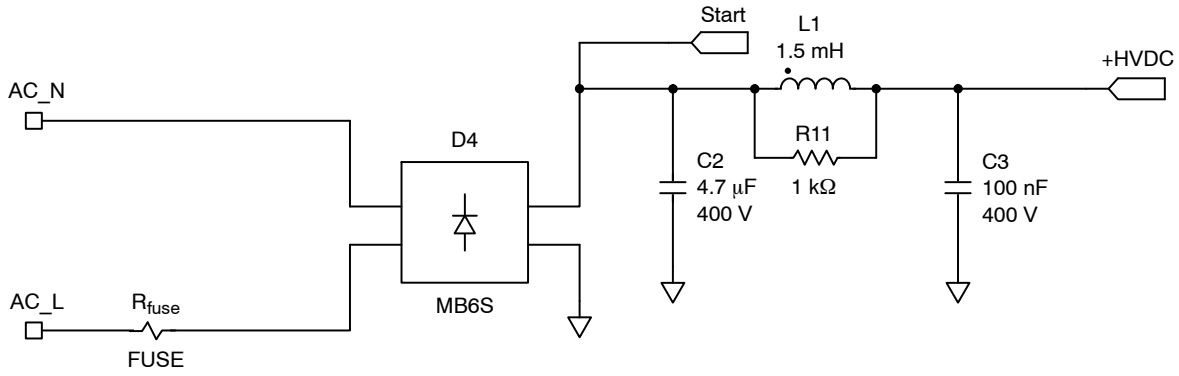


Figure 4. Input Circuit

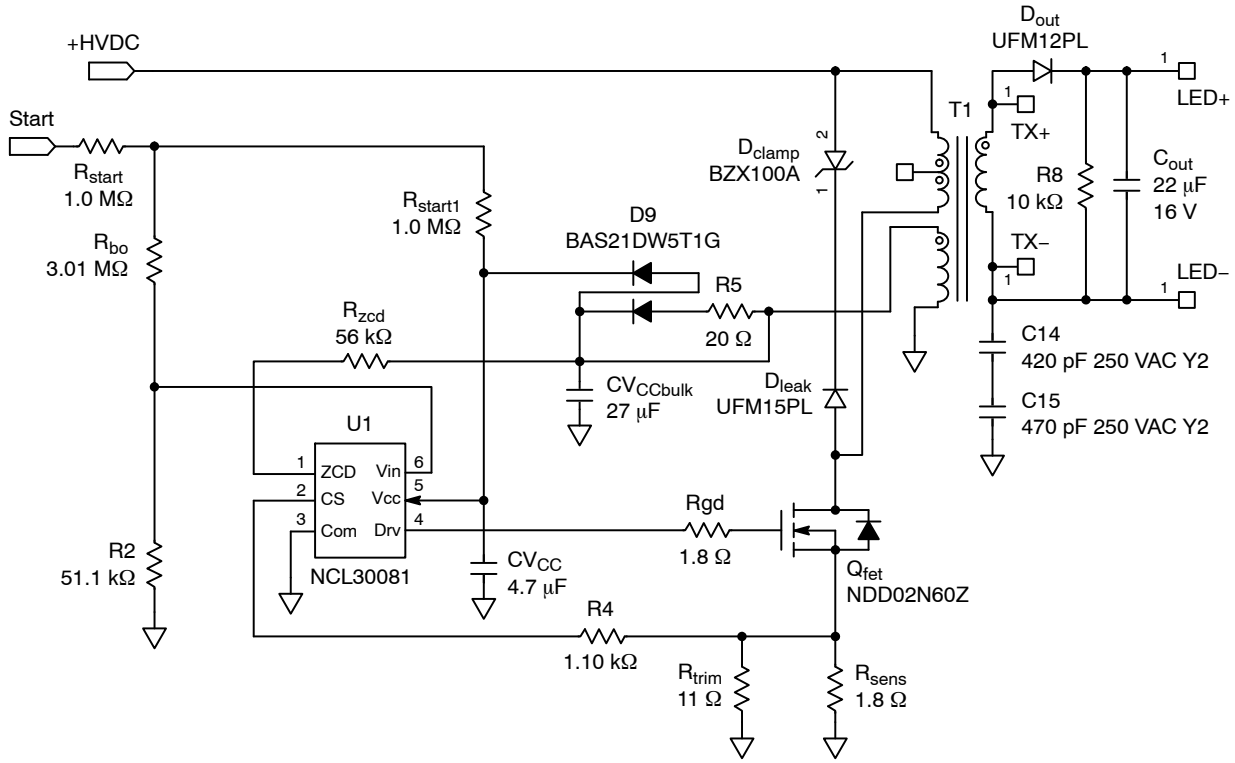


Figure 5. Main Schematic

Table 2. BILL OF MATERIALS

Qty	Reference	Part	PCB Footprint	Manufacturer	Mfr_PN	Can be Substituted	RoHS
1	CVcc	4.7 μF	0603	Taiyo Yuden	EMK107ABJ475KA-T	Yes	Yes
1	CVccbulk	27 μF	CAP-ALEL-4X11-HOR	Panasonic	EEU-FC1E270	Yes	Yes
1	Cout	22 μF 16 V	1206	Taiyo Yuden	EMK316BJ226ML-T	Yes	Yes
1	C2	4.7 μF 400 V	CAP_ALEL_D10XL13	Rubycon	400LLE4R7MEFC10X12.5	Yes	Yes
1	C3	100 nF 400 V	CAP-BOX-LS5-5M0X7M2	Epcos	B32559C6104+***	Yes	Yes
2	C14, C15	470 pF 250 VAC Y2	1808	Johanson-Dielectrics	502R29W471KV3E-****-SC	Yes	Yes
1	Dclamp	BZX100A	SOD323F	NXP	BZX100A,115	Yes	Yes
1	Dleak	UFM15PL	SOD123FL	MCC	UFM15PL	Yes	Yes
1	Dout	UFM12PL	SOD123FL	MCC	UFM12PL	Yes	Yes
1	D4	MB6S	MB6S	MCC	MB6S	Yes	Yes
1	D9	BAS21DW5T1G	SC-88A	ON Semiconductor	BAS21DW5T1G	No	Yes
1	L1	1.5 mH	IND-UPRIGHT-LS25	Wurth	7447462152	Yes	Yes
1	Qfet	NDD02N60Z	IPAK	ON Semiconductor	NDD02N60Z	No	Yes
1	Rbo	3.01 MΩ	0805	Yageo	RC0805FR-073M01L	Yes	Yes
1	Rfuse	FUSE	FUSE-HAIRPIN-LS250	Littelfuse	0263.500WRT1L	Yes	Yes
2	Rsens, Rgd	1.8 Ω	0603	Vishay	CRCW06031R80FKEA	Yes	Yes
2	Rstart1, Rstart	1.0 MΩ	0805	Yageo	RC0805FR-071ML	Yes	Yes
1	Rtrim	11 Ω	0402	Yageo	RT0402FRE0711RL	Yes	Yes
1	Rzcd	56 kΩ	0805	Yaego	RC0805FR-0756KL	Yes	Yes
1	R2	51.1 kΩ	0402	Yaego	RC0402FR-0751K1L	Yes	Yes
1	R4	1.10 kΩ	0402	Stackpole	RMCF0402FT1K10	Yes	Yes
1	R5	20 Ω	0402	Yaego	RC0402FR-0720RL	Yes	Yes
1	R8	10 kΩ	0402	Yaego	RC0402FR-0710KL	Yes	Yes
1	R11	1 kΩ	0805	Yaego	RC0805JR-071KL	Yes	Yes
1	T1	XFRM_LINEAR	EP13-SMD-16PIN-MOD1	Wurth	750313306	Yes	Yes
1	U1	NCL30080/1	TSOP6	ON Semiconductor	NCL30080	No	Yes
					NCL30081		
2	Wire 6”, Input, White		UL1430	Alpha Wire	#24 AWG, Stranded	Yes	Yes
1	Wire 6”, Output, Red		UL1430	Alpha Wire	#24 AWG, Stranded	Yes	Yes
1	Wire 6”, Output, Black		UL1430	Alpha Wire	#24 AWG, Stranded	Yes	Yes

GERBER VIEWS

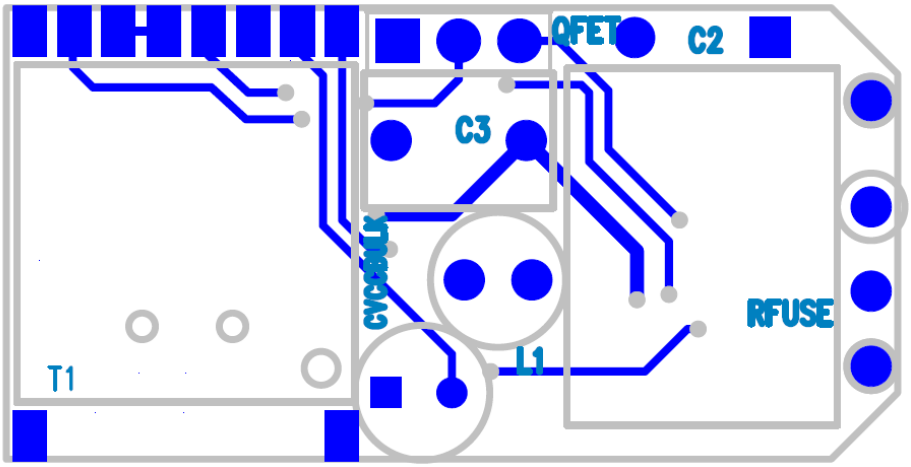


Figure 6. Component Side PCB

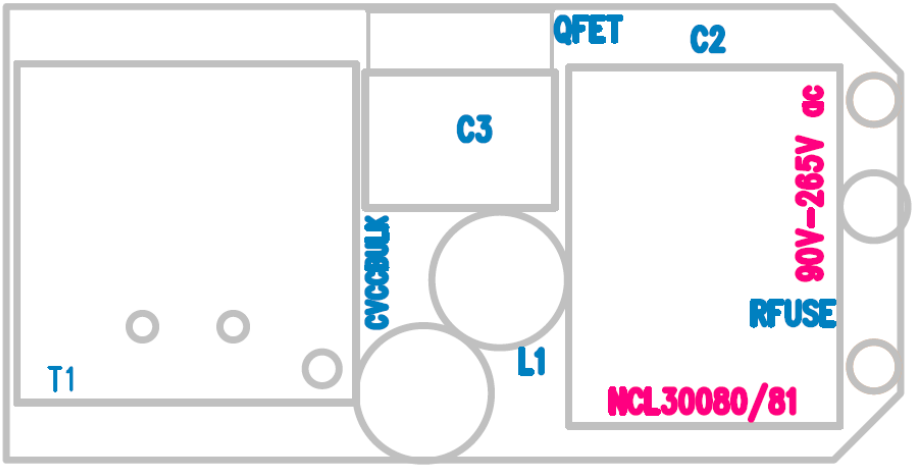


Figure 7. Component Side Silkscreen

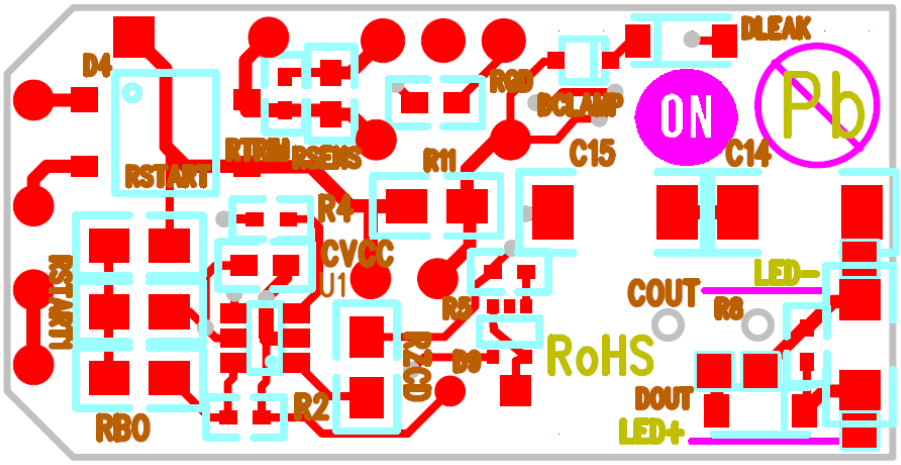


Figure 8. Solder Side PCB

GERBER VIEWS (CONTINUED)

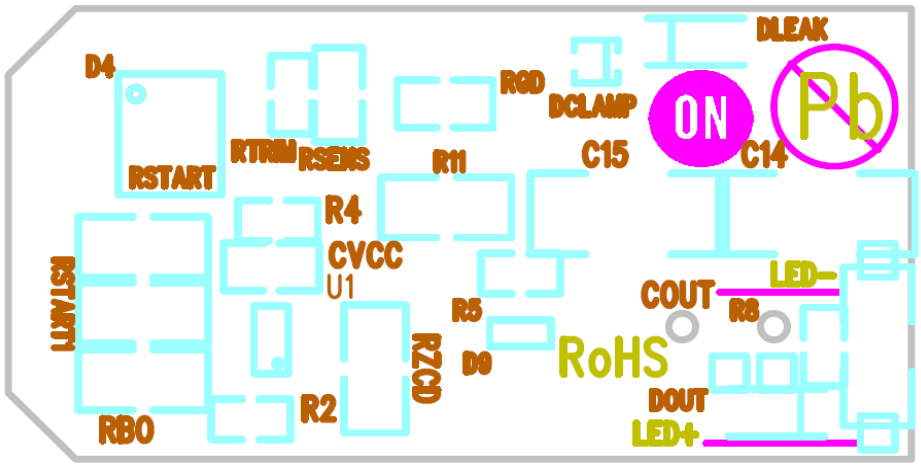


Figure 9. Solder Side Silkscreen

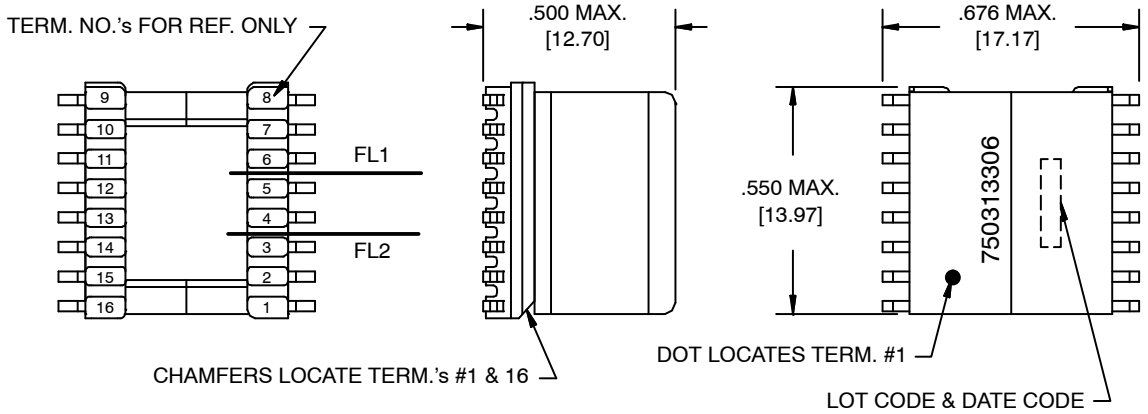
CIRCUIT BOARD FABRICATION NOTES

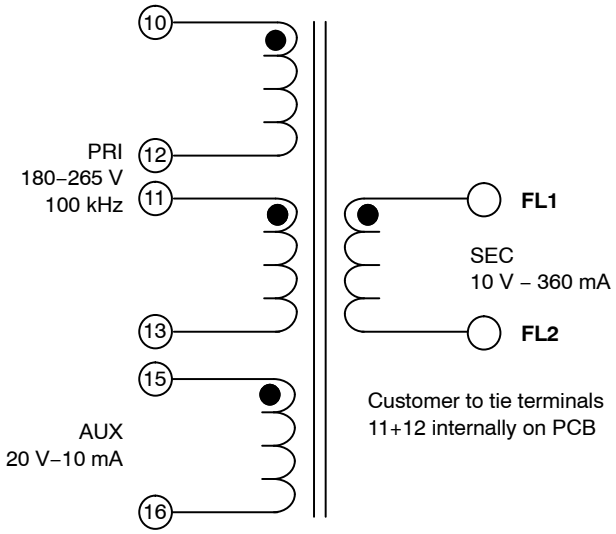
1. Fabricate per IPC-6011 and IPC6012. Inspect to IPA-A-600 Class 2 or updated standard.
2. Printed Circuit Board is defined by files listed in fileset.
3. Modification to copper within the PCB outline is not allowed without permission, except where noted otherwise. The manufacturer may make adjustments to compensate for manufacturing process, but the final PCB is required to reflect the associated gerber file design ±0.001 in. for etched features within the PCB outline.
4. Material in accordance with IPC-4101/21, FR4, Tg 125°C min.
5. Layer to layer registration shall not exceed ±0.004 in.
6. External finished copper conductor thickness shall be 0.0013 in. min.
7. Copper plating thickness for through holes shall be 0.0007 in. min.
8. All holes sizes are finished hole size.
9. Finished PCB thickness 0.031 in.
10. All un-dimensioned holes to be drilled using the NC drill data.
11. Size tolerance of plated holes: ±0.003 in.: non-plated holes ±0.002 in.
12. All holes shall be ±0.003 in. of their true position U.D.S.
13. Construction to be SMOBC, using liquid photo image (LPI) solder mask in accordance with IPC-SM-B40C, Type B, Class 2, and be green in color.
14. Solder mask mis-registration ±0.004 in. max.
15. Silkscreen shall be permanent non-conductive white ink.
16. The fabrication process shall be UL approved and the PCB shall have a flammability rating of UL94V0 to be marked on the solder side in silkscreen with date, manufactures approved logo, and type designation.
17. Warp and twist of the PCB shall not exceed 0.0075 in. per in.
18. 100% electrical verification required.
19. Surface finish: electroless nickel immersion gold (ENIG)
20. RoHS compliance required.

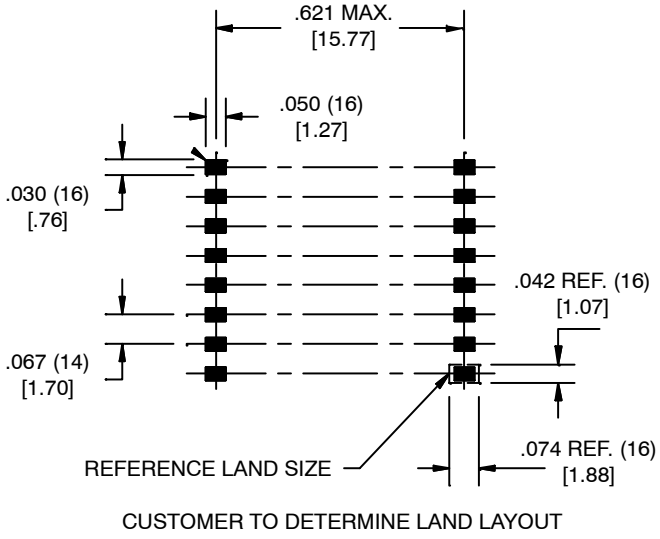
FLYBACK TRANSFORMER SPECIFICATION

CUSTOMER TERMINAL	RoHS	LEAD(Pb)-FREE
Sn 96%, Ag 4%	Yes	Yes

Update views to show flying leads and lead length dimension.
Leads are 2″ from outside bobbin rail and 1.8″ tinned.







ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

D.C. RESISTANCE (@ 20°C):	10−13 (tie 11+12), 2.50 Ω ±10%. 15−16, 1.28 Ω ±10%. FL1−FL2, 0.115 Ω ±20%.
DIELECTRICRATING:	4,000 VAC, 1 minute tested by applying 4,000 VAC for 1 second between pins 10−FL1 (tie 12+13+15). 500 VAC, 1 minute tested by applying 625 VAC for 1 second between pins 10−16.
INDUCTANCE:	1.50 mH ±10%, 10 kHz, 100 mVAC, 0 mADC, 10−13 (11+12), Ls.
SATURATION CURRENT:	420 mA saturating current that causes 20% rolloff from initial inductance.
LEAKAGE INDUCTANCE	7 μH typ, 15 μH max., 100 kHz, 100 mVAC, 10−13 (tie 11+12, 15+16, FL1+FL2), Ls.
TURNS RATIO:	(10−12):(11−13), (1):(1.00), ±1%. (10−13):(15−16), (2.5):(1.00), tie (11+12), ±1%. (10−13):(FL1−FL2), (5):(1.00), tie (11+12), ±1%.

OPERATING TEMPERATURE RANGE: −40°C TO 125°C including temp. rise.

Unless otherwise specified, tolerances are as follows: Angles: ±1° Fractions: ±1/64 Decimals: ±0.005 (.127 mm)
This drawing is dual dimensioned. Dimensions in brackets are in millimeters.

ECA PICTURES

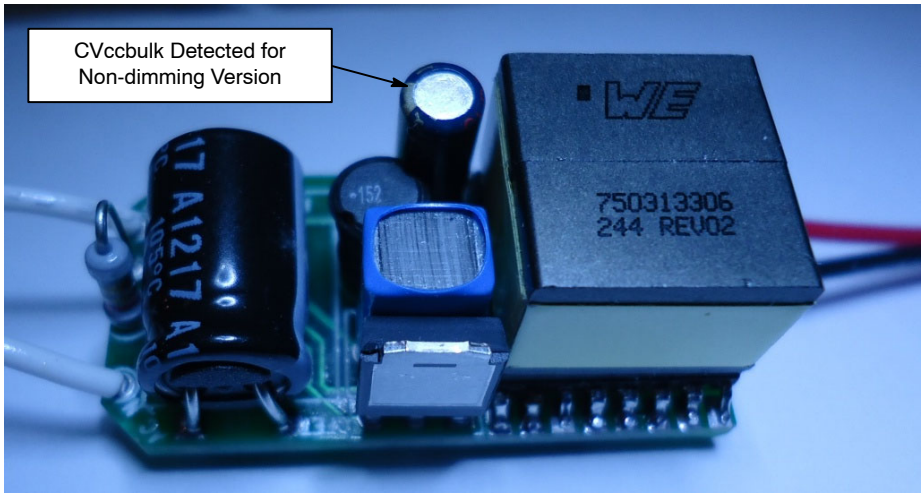


Figure 10. Top View

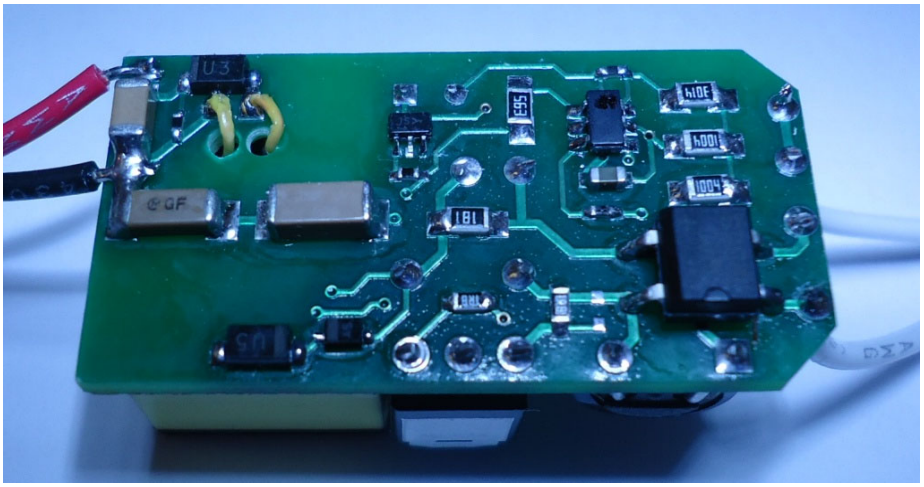


Figure 11. Bottom View

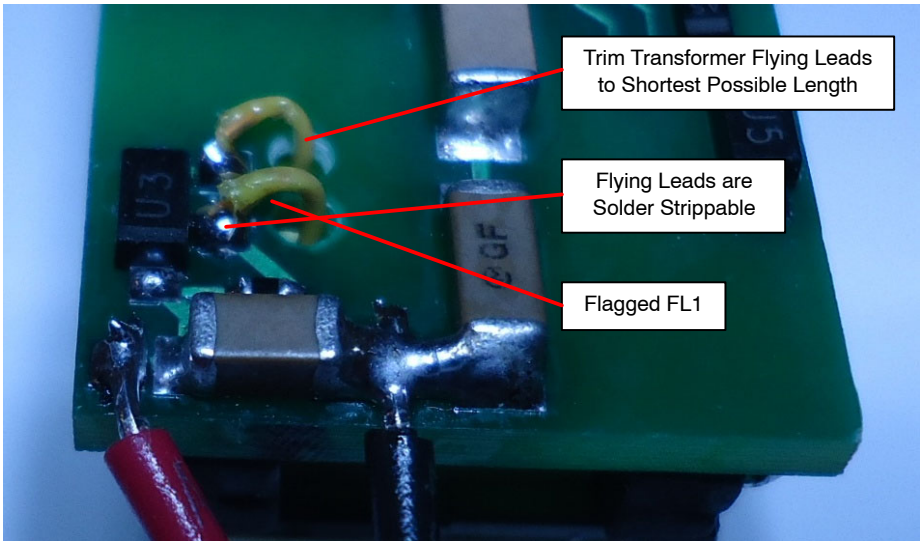


Figure 12. Transformer and Output Terminations

TEST PROCEDURE

Equipment Needed

- AC Source:
  90–265 V ac 50/60 Hz Minimum 1 A ac capability
- AC Wattmeter:
  30 W Minimum, True RMS Input Voltage and Current, Power Factor 0.2% accuracy or better
- DC Voltmeter:
  100 V dc minimum 0.1% accuracy or better
- DC Ammeter:
  1 A dc minimum 0.1% accuracy or better
- LED Load:
  9–10.5 V dc – 3 LED Load @ 360 mA

Test Connections

1. Connect the Unit Under Test (UUT) per the test set up in Figure 13
2. Set the AC source per the test procedure.

NOTE: Unless otherwise specified, all voltage measurements are taken at the terminals of the UUT.

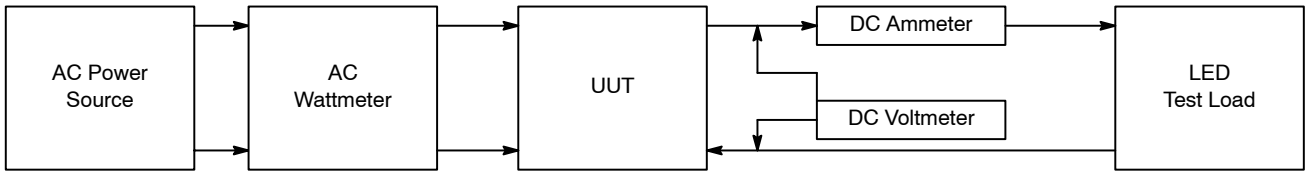


Figure 13. Test Set Up

Functional Test Procedure

Test Condition	Test Variable	Test Limits		Pass/Fail
		Min	Max	
V_{in} = 90 V ac	Output Current	350 mA	370 mA	–
V_{in} = 120 V ac	Output Current	350 mA	370 mA	–
V_{in} = 265 V ac	Output Current	350 mA	370 mA	–
V_{in} = 120 V ac	Power Factor	0.55	–	–
V_{in} = 120 V ac V_{out} = 10.5 V dc	Efficiency (use actual measured data)	80%	–	–

Efficiency = $100\% \times (V_{OUT} \times I_{OUT}) / Pin$

TEST DATA

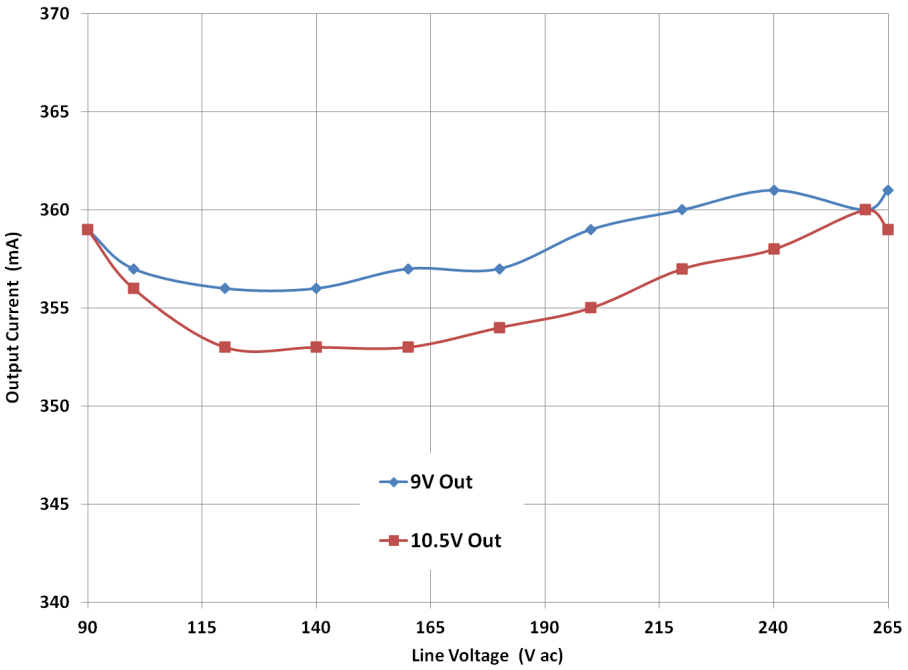


Figure 14. Regulation over Line Voltage

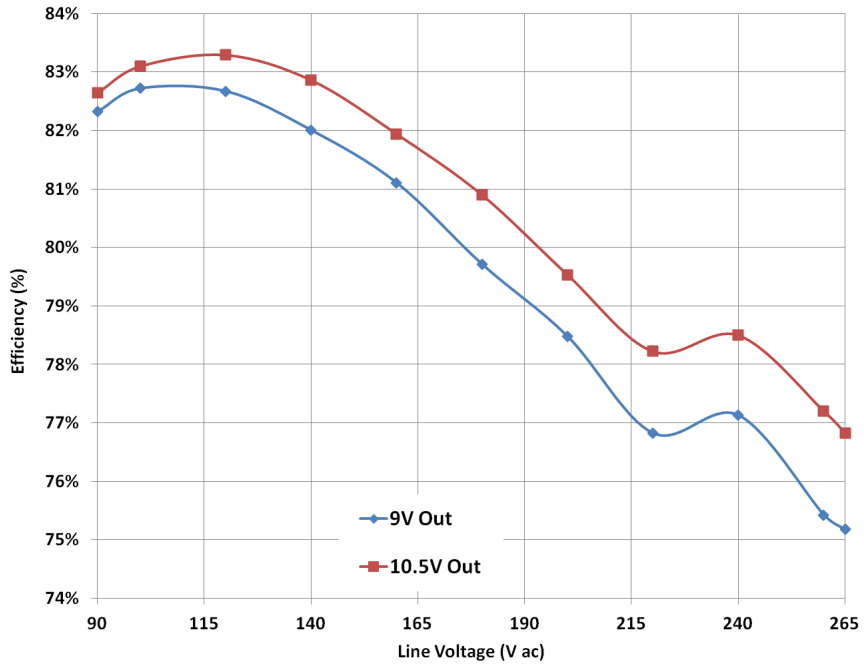


Figure 15. Efficiency over Line Voltage

TEST DATA (CONTINUED)

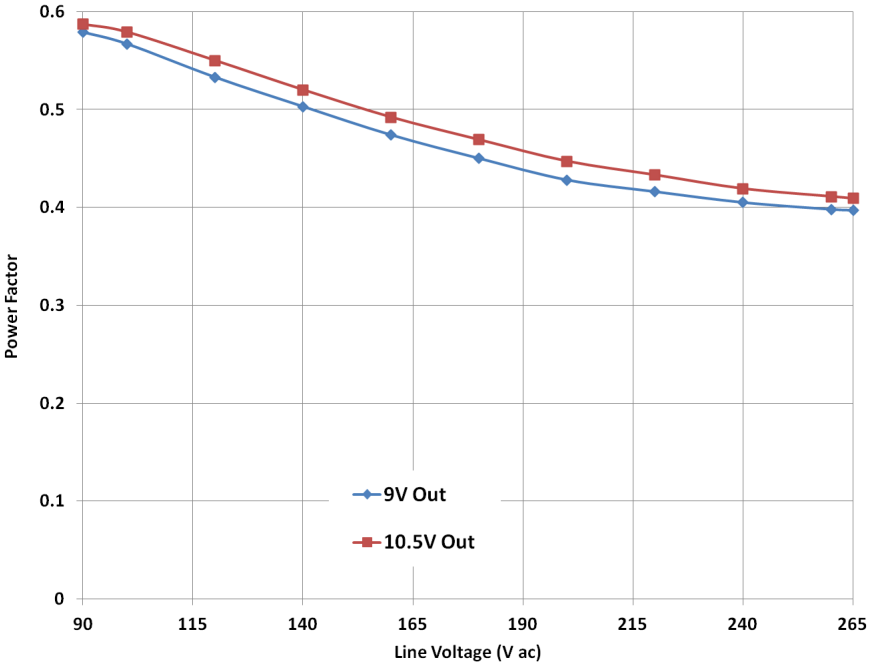


Figure 16. Power Factor over Line Voltage

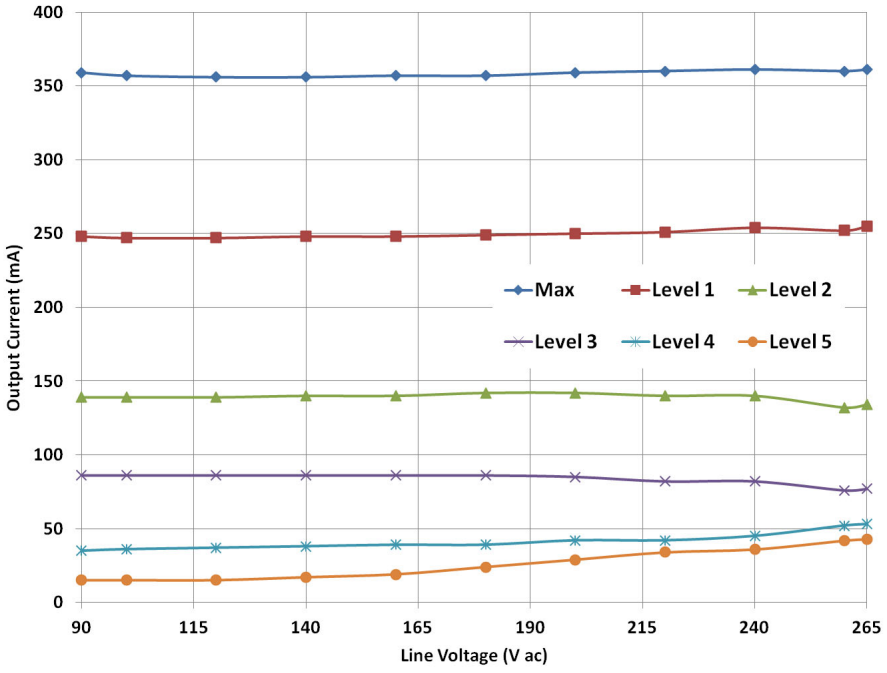


Figure 17. Dimming over Line Voltage

TEST DATA (CONTINUED)

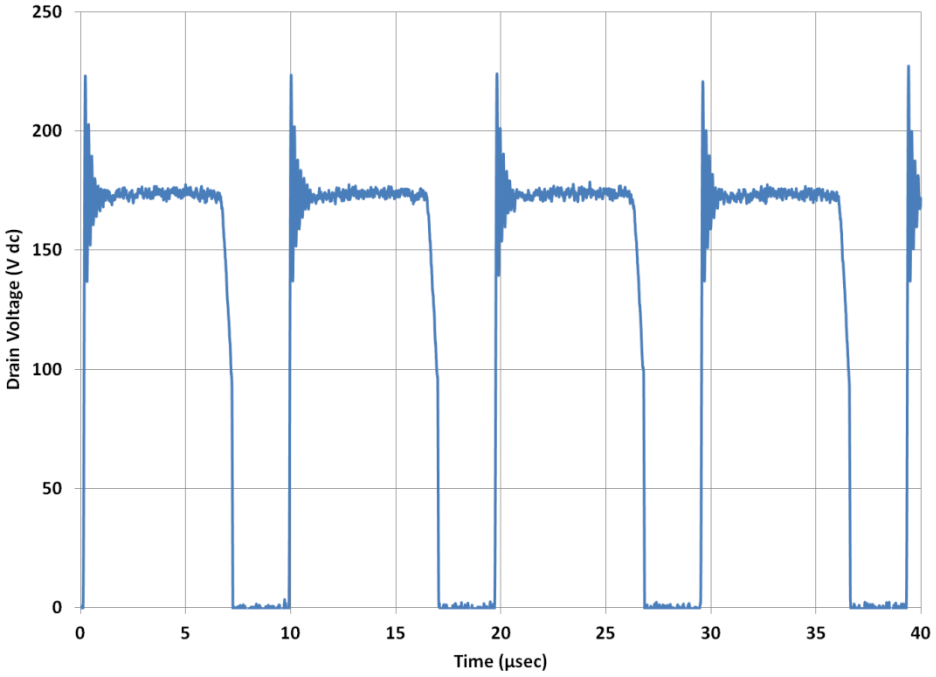


Figure 18. Drain Voltage @ 90 V ac

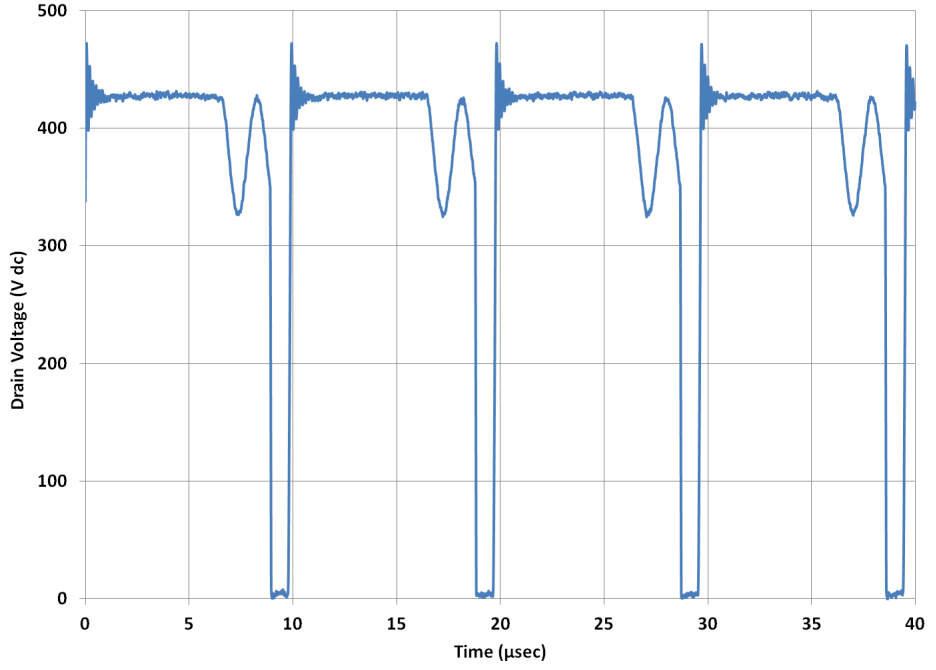


Figure 19. Drain Voltage @ 265 V ac

TEST DATA (CONTINUED)

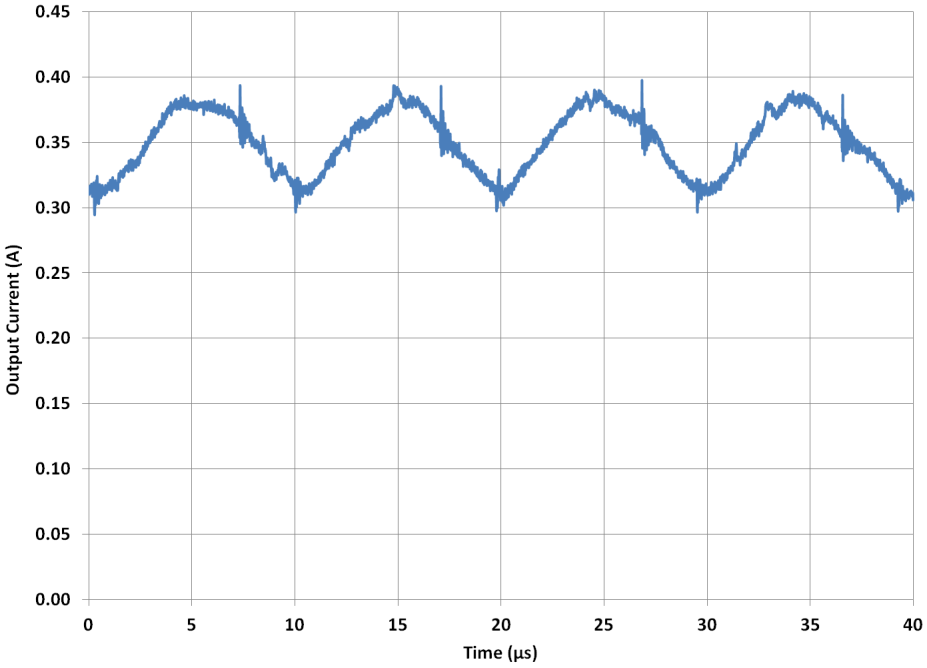


Figure 20. Output Ripple 90 V ac 50 Hz

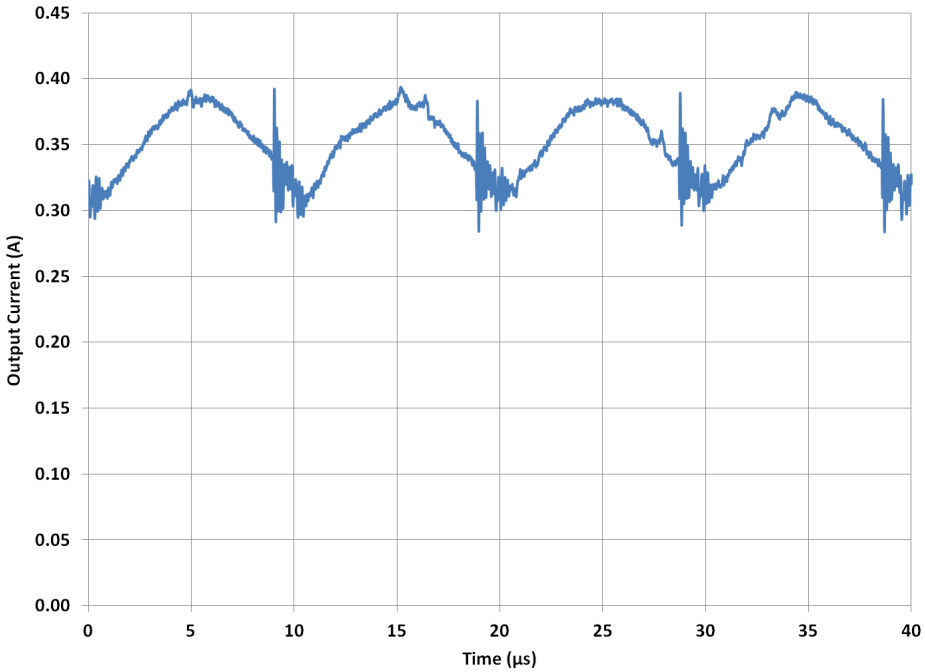


Figure 21. Output Ripple 265 V ac 50 Hz

TEST DATA (CONTINUED)

Figure 22. Conducted EMI Pre-compliance 150 kHz–2 MHz

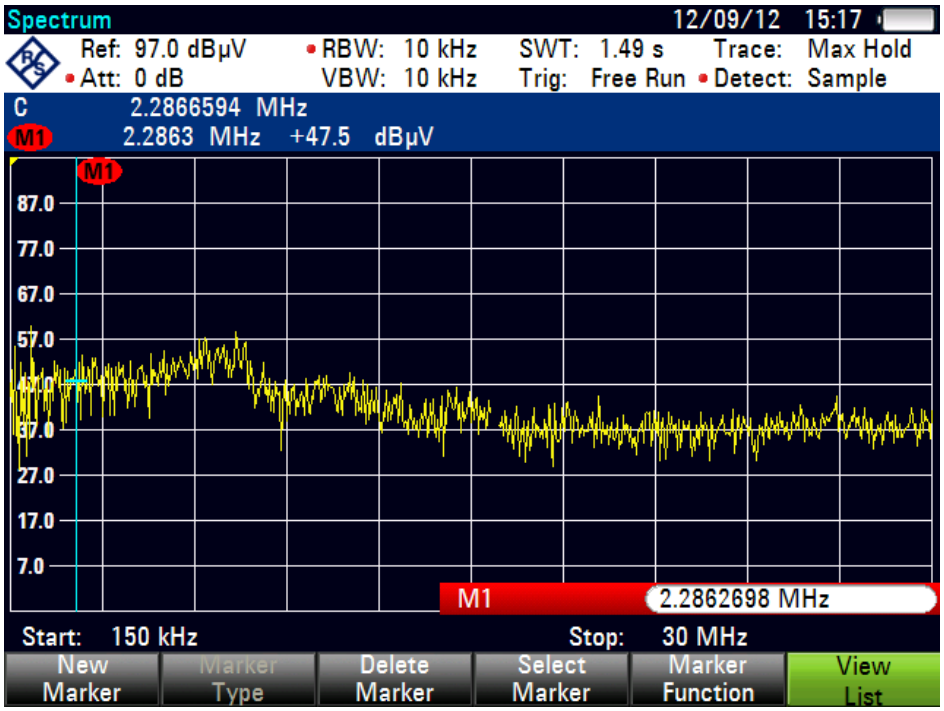


Figure 23. Conducted EMI Pre-compliance 150 kHz–30 MHz

APPENDIX

IEC61000-3-2 Class C Compliance

Compliance to IEC61000-3-2 Class C (under 25 W) is not possible with the universal front end architecture since input current does not comply with Class D requirements or the waveform definition requirements as stated in this excerpt.

Active Input Power ≤ 25 W:

Discharge lighting equipment having an active input power smaller than or equal to 25 W shall comply with one of the following two sets of requirements:

- The harmonic currents shall not exceed the power-related limits of Table 3, column 2, or:
- The third harmonic current, expressed as a percentage of the fundamental current, shall not exceed 86% and the fifth shall not exceed 61%; moreover, the waveform of the input current shall be such that it begins to flow before or at 60°, has its last peak (if there are several peaks per half period) before or at 65° and does not stop flowing before 90°, where the zero crossing of the fundamental supply voltage is assumed to be at 0°.

If the discharge lighting equipment has a built-in dimming device, measurement is made only in the full load condition.

It is possible to comply with the special waveform and harmonic requirements of the third paragraph with a standard peak charge front end if the bulk capacitance is properly sized. The bulk capacitor must be in the range of 200−300 nF/W for a 230 V ac line for Europe. Japan has a similar requirement; however, the bulk capacitance must be 800–1,200 nF/W because the nominal main is 100 V ac rather than 230 V ac. The recommended capacitance values are line specific. So there is no universal mains solution with a peak charge front end. It is possible to convert the Evaluation Board to IEC61000−3−2 Class C compliance by changing C2.

Table 3. C2 Capacitor Selection

Line	Minimum Capacitance	Maximum Capacitance	Voltage Rating
230 V ac 50 Hz	0.82 μF	1.2 μF	400 V dc
100 V ac 50/60 Hz	3.6 μF	4.7 μF	200 V dc

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