EVBUM2528/D

NCP51705 Mini Evaluation Board User's Manual

NCP51705 SiC Driver Evaluation Board for Existing or New PCB Designs

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EVAL BOARD USER'S MANUAL

INTRODUCTION

Purpose

This document describes the use and applications for the NCP51705 SiC driver mini EVB. The EVB is designed on a four layer PCB and includes the NCP51705 driver and all the necessary drive circuitry. The EVB also includes an on−board digital isolator and the ability to solder any MOSFET or SiC MOSFET in a T0247 high voltage package. The EVB does not include a power stage and is generic from the point of view that it is not dedicated to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these EVBs can be configured in a totem pole type drive configuration. The EVB can be considered as an isolator+driver+T0247 discrete module.

NCP51705 Description

The NCP51705 driver is designed to primarily drive SiC MOSFET transistors. To achieve the lowest possible conduction losses, the driver is capable of delivering the maximum allowable gate voltage to the SiC MOSFET device. By providing high peak current during turn−on and turn−off, switching losses are also minimized. For improved reliability, dV/dt immunity and even faster turn−off, the NCP51705 can utilize its on−board charge pump to generate a user selectable negative voltage rail.

For full compatibility and to minimize the complexity of the bias solution in isolated gate drive applications the NCP51705 also provides an externally accessible 5V rail to power the secondary side of digital or high speed opto isolators.

The NCP51705 offers important protection functions such as under−voltage lockout monitoring for the bias power and thermal shutdown based on the junction temperature of the driver circuit.

NCP51705 Block Diagram

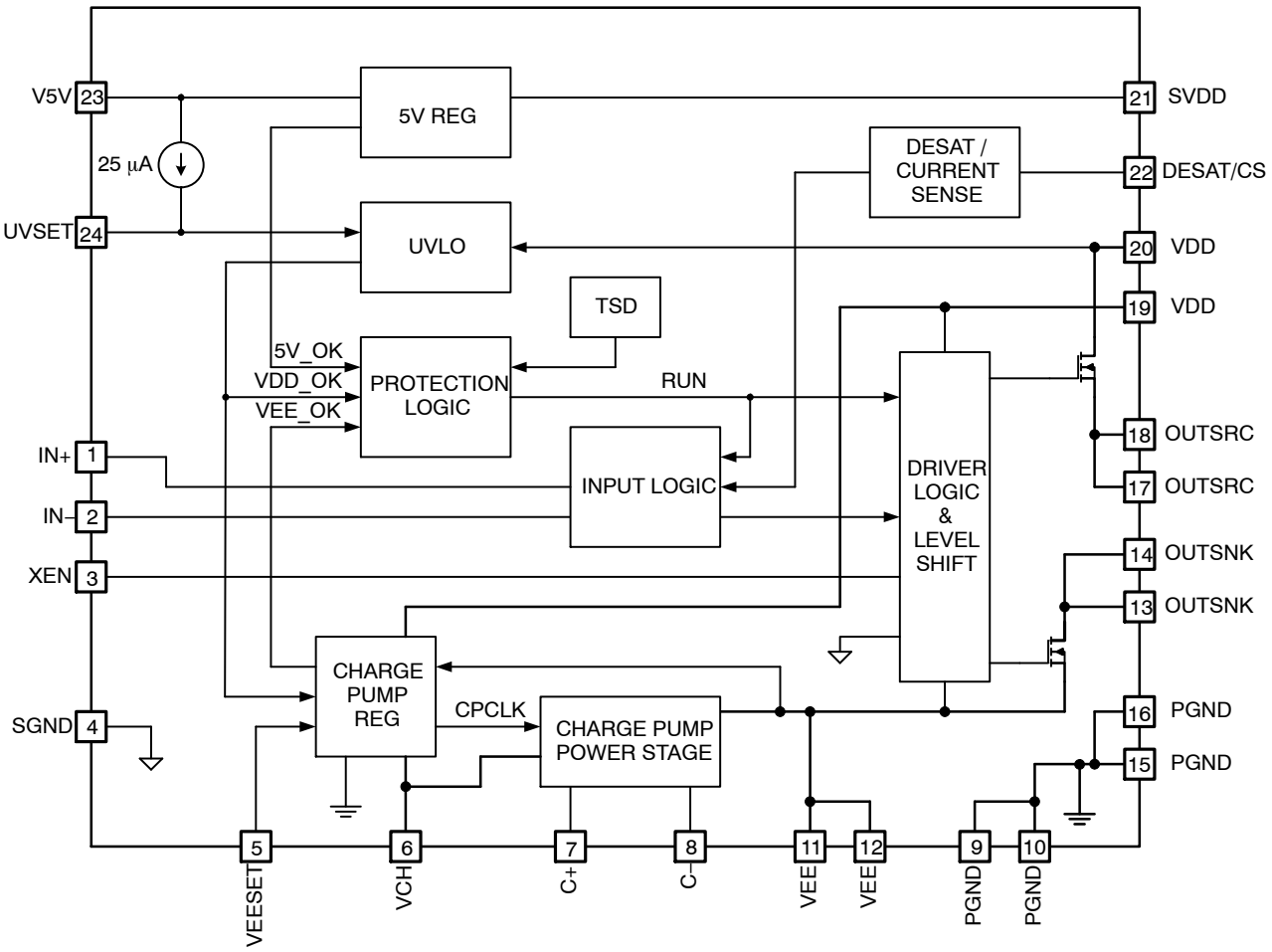

Figure 1. NCP51705 Functional Block Diagram

SUMMARY OF EVB

EVB Photos

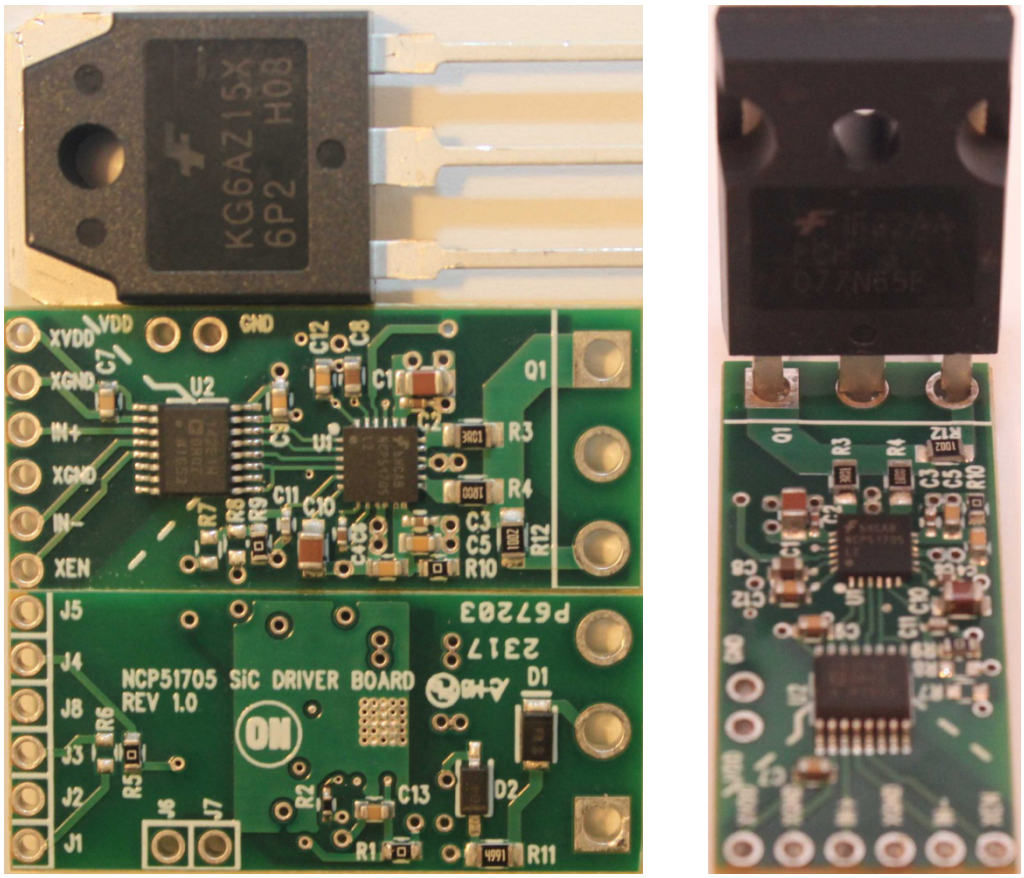

Figure 2. NCP51705 EVB (35 mm x 15 mm x 5 mm) − Top and Bottom View (T0−247 Shown for Scale)

EVB Schematic

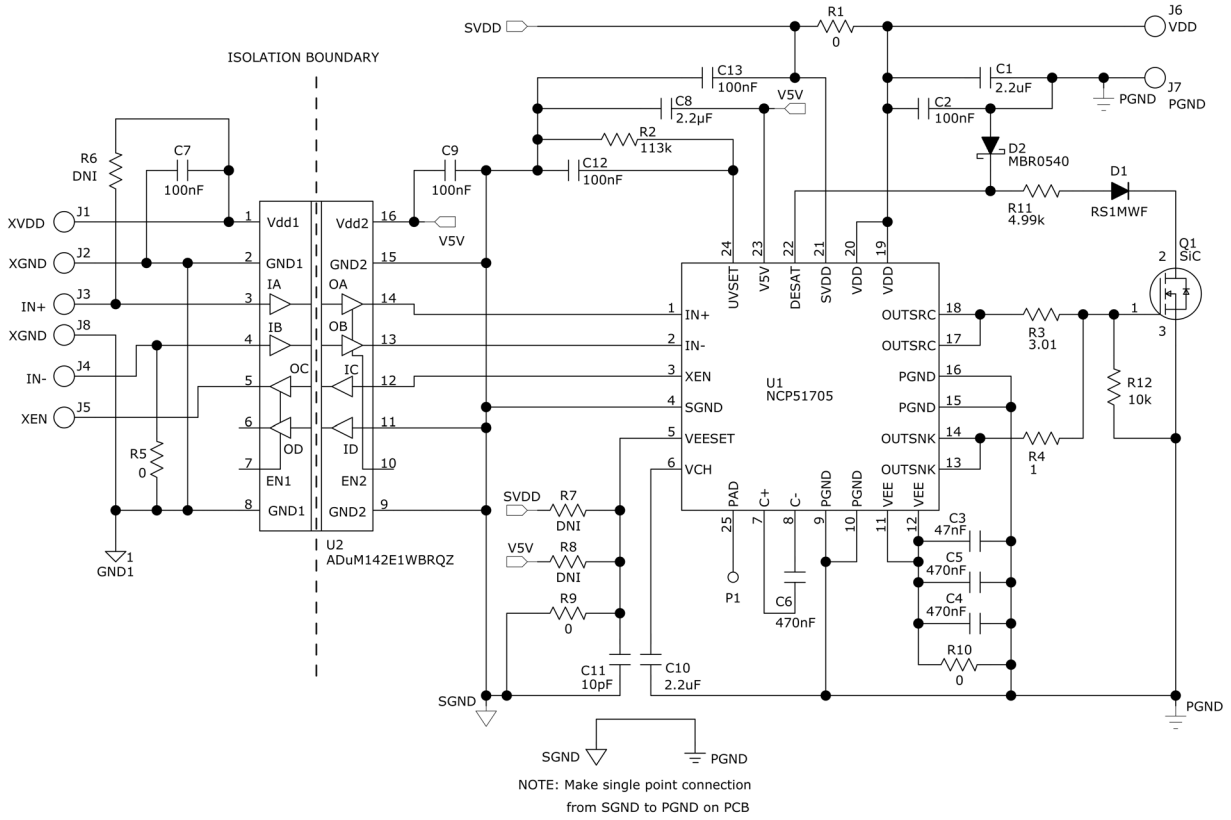

Figure 3. NCP51705 EVB Schematic

Table 1. BILL OF MATERIALS

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
1	2	C1 C10	2.2 µF	CGA4J3X7R1H225M125AE	CAP, SMD, CERAMIC, 50 V, X7R	STD	805
2	2	C2 C13	100 nF	C1005X7R1H104M050BE	CAP, SMD, CERAMIC, 50 V, X7R	STD	402
3	1	C3	47 nF	GRM155R71E473KA88D	CAP, SMD, CERAMIC, 25 V, X7R	STD	402
4	2	C4−5	470 nF	GRM188R71E474KA12D	CAP, SMD, CERAMIC, 25 V, X7R	STD	603
5	1	C6	470 nF	C1005X5R1E474K050BB	CAP, SMD, CERAMIC, 25 V, X5R	STD	402
6	3	C7 C9 C12	100 nF	C0603C104K8RACTU	CAP, SMD, CERAMIC, 10 V, X7R	STD	603
7	1	C8	2.2 µF	LMK107B7225KA−T	CAP, SMD, CERAMIC, 10 V, X7R	STD	603
8	1	C11	10 pF	GRM1555C1H100JA01D	CAP, SMD, CERAMIC, 50 V, NPO	STD	402
9	1	D1		RS1MWF	Diode, Fast, 1 A, 1000 V, Std. Rec.	Vishay	SOD123F
10	1	D2		MBR0540	Diode, Shottky, 40 V, 500 mA, 510 mV	ON Semiconductor	SOD−123
11	1	Q1		DNI	MOSFET, N−CH, 600 V, 20 A, 190 mΩ	ON Semiconductor	TO−247

Table 1. BILL OF MATERIALS

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
12	4	R1 R5 R9−10	0	RC0603JR−070RL	RES, SMD, 1/10 W	STD	603
13	1	R2	113k	RC0402FR−07200KL	RES, SMD, 1/16 W	STD	402
14	1	R3	3.01	RMCF0805FT3R01	RES, SMD, 1/8 W	STD	805
15	1	R4	1	RMCF0805FT1R00	RES, SMD, 1/8 W	STD	805
16	3	R6−8	DNI		RES, SMD, 1/10 W	STD	603
17	1	R11	4.99k	RC0805FR−074K99L	RES, SMD, 1/8 W	STD	805
18	1	R12	10k	RC0805FR−0710KL	RES, SMD, 1/8 W	STD	805
19	1	U1		NCP51705	SiC Driver, Single, 6 A, Single	ON Semiconductor	WQFN−24
20	1	U2		ADuM142E1WBRQZ	Digital Isolator, RF, 4−Channel	Analog Devices	QSOP−16

PCB Assembly and Layers

Figure 4 through Figure 9 shows the top and bottom assembly and the four−layers of the PCB. The PCB is 35 mm x 15 mm x 5 mm (length x width x height) where the width of the PCB is approximately the width of a T0−247 body.

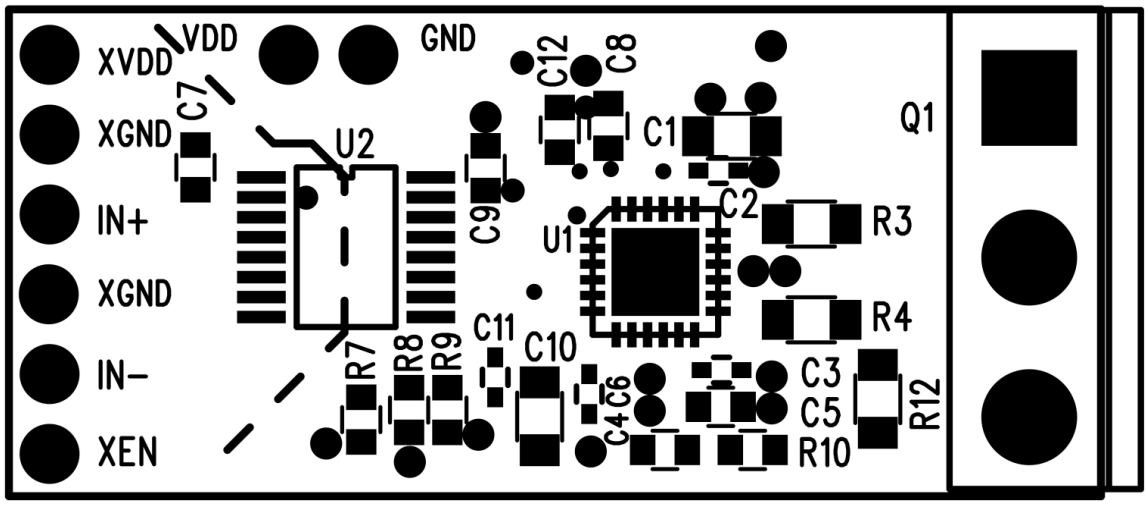

Figure 4. Top Assembly

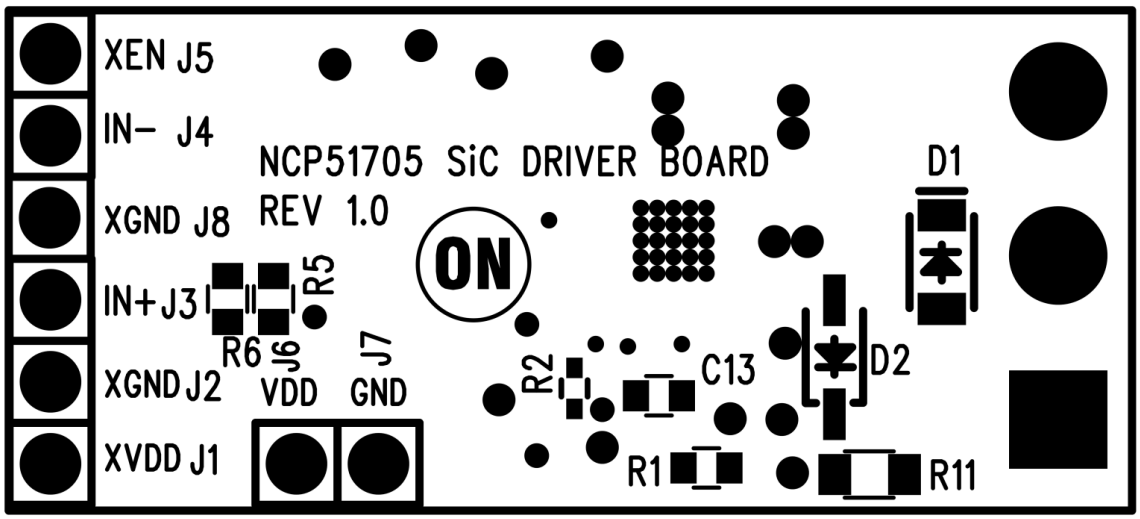

Figure 5. Bottom Assembly

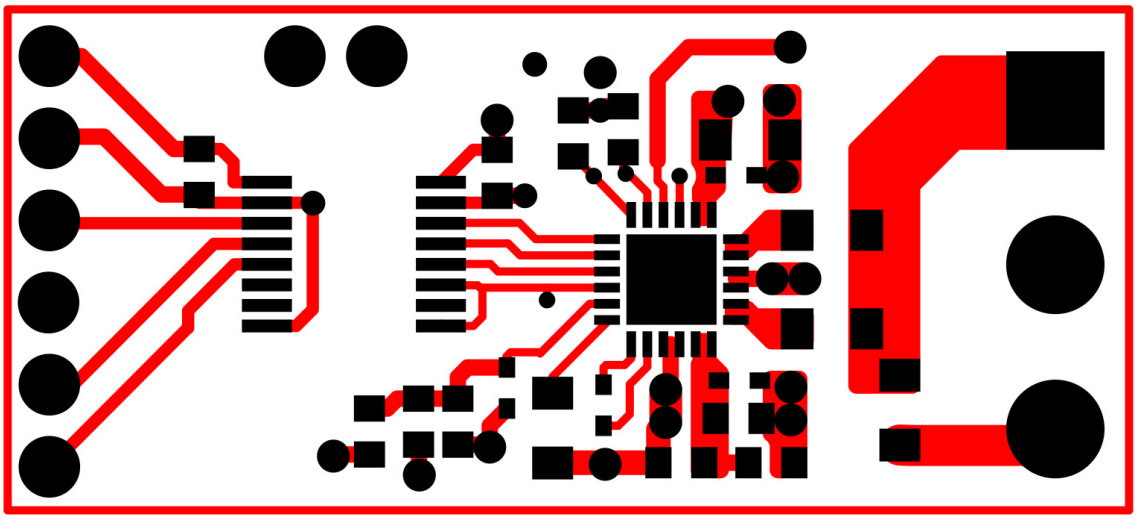

Figure 6. Top Layer

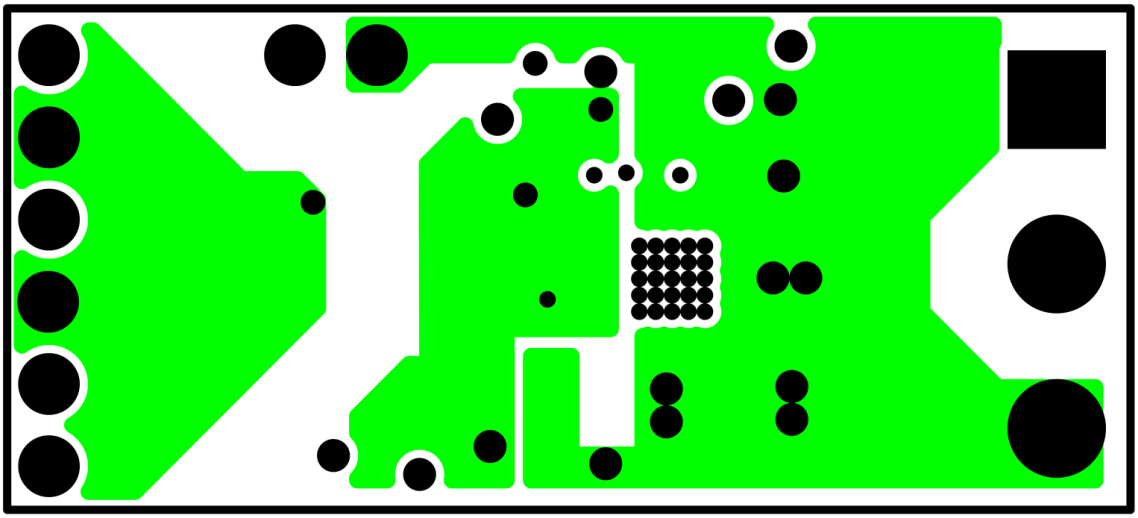

Figure 7. Layer 2

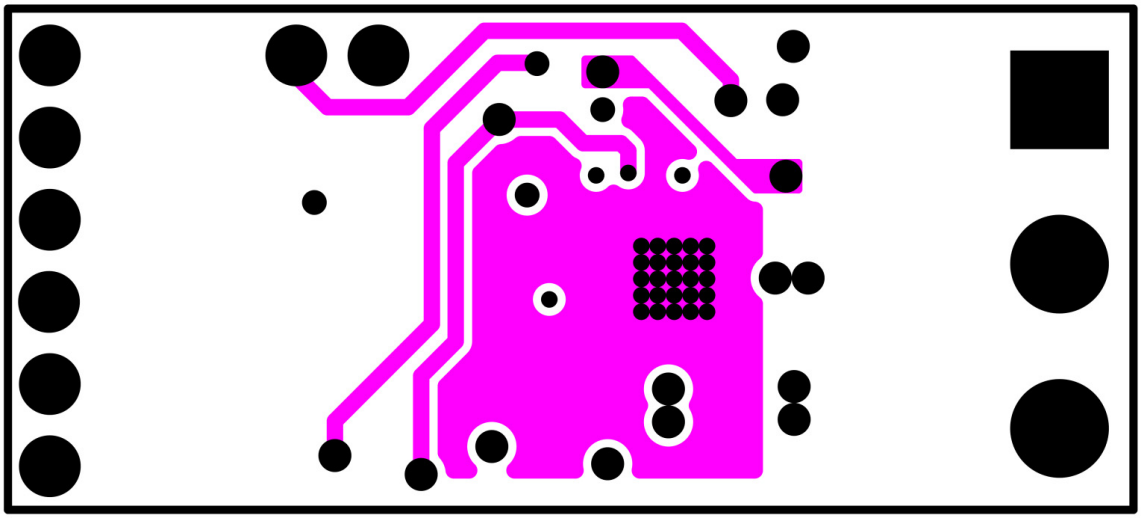

Figure 8. Layer 3

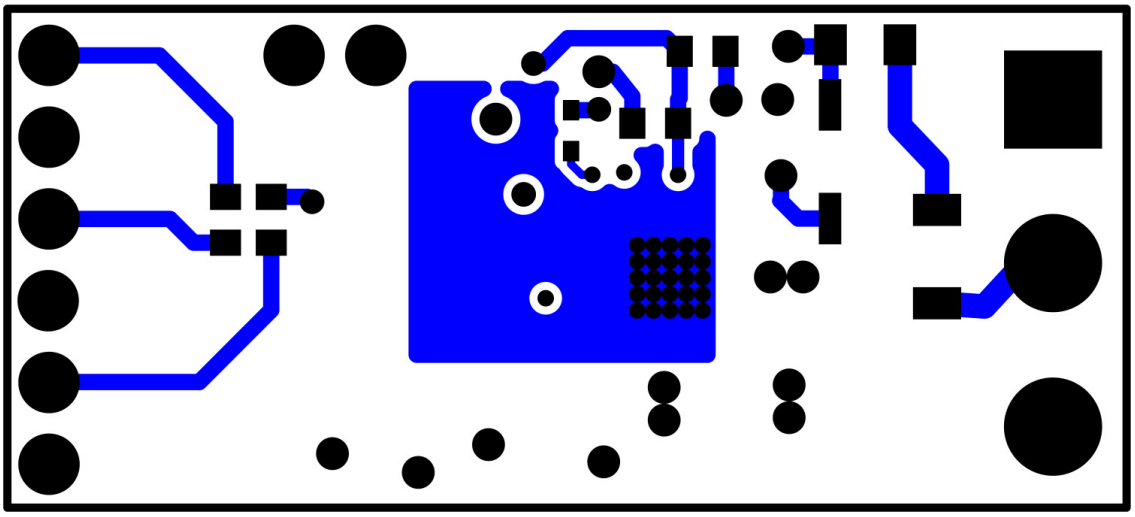

Figure 9. Bottom Layer

I/O Connectors

There are 7 I/O connectors described in Table 2 below. The μC (or, PWM control IC) output (J3, J4), the XVDD and XGND (J1, J2) and the XEN (J5) signals are noted as "primary" ground referenced. There is no true "primary" and "secondary" ground but there is 1.5 kV galvanic isolation across the isolation boundary. It is especially important to maintain isolation in high−side, high−voltage, switching applications where the "secondary" VDD (J6, J7) floats VDD volts above the power supply input voltage:

Table 2. I/O CONNECTOR DESCRIPTIONS

Ref Des	Name	I/O	GND Ref	Type	Description	Value (V)
J1	XGND	Input	Primary	Plated Hole	External primary ground from PWM side	0
J2	XVDD	Input	Primary	Plated Hole	External VDD from PWM side (isolator bias)	5 (Note 1)
J3	IN+	Input	Primary	Plated Hole	Non−inverting, PWM input	$3.3<V_{IN+}<5$ (Note 1)
J4	IN−	Input	Primary	Plated Hole	Inverting PWM input	$3.3<V_{IN-}<5$ (Note 1)
J5	XEN	Output	Primary	Plated Hole	XEN fault flag or sync signal from NCP51705	5
J6	VDD	Input	Secondary	Plated Hole	NCP51705 VDD	<20
J7	GND	Input	Secondary	Plated Hole	NCP51705 secondary ground	0
J8	XGND	Input	Primary	Plated Hole	External primary ground from PWM side	0

1. The digital isolator, U2, requires that the amplitude of the PWM input (IN+ or IN−) be equal to VDD (XVDD) and less than or equal to 5 V.

EVB INSTALL CONFIGURATIONS

Mounting into Existing PCB − Option 1

The NCP51705, SiC Driver Mini EVB can be mounted into an existing power board, shown as “Main PCB” in Figure 10. If there are no components or low profile surface mount components only, the mini EVB can be mounted parallel to the main PCB as shown in Figure 10. The T0−247, SiC MOSFET leads would pass through the mini EVB plated thru−holes and into the main PCB. Or, if necessary, the gate lead of the T0−247, SiC MOSFET can be soldered to the plated thru−hole on the mini EVB and cut so that it does not contact the main PCB, as shown in the dotted box in Figure 10. For mechanical strength, it is preferred that the T0−247 gate lead pass through both PCB’s.

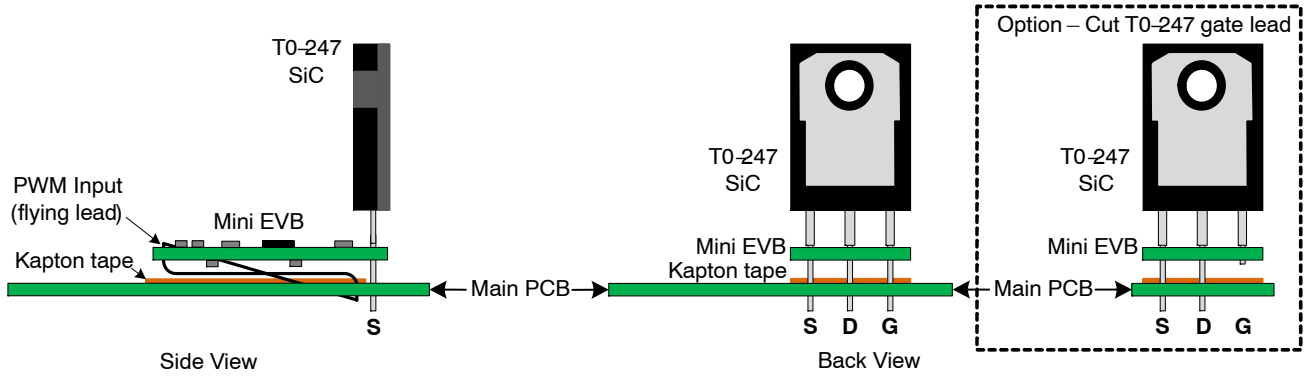

Figure 10. Mini EVB Installation − Option 1

Recommended Procedure for Option 1 Mounting into an Existing PCB

1. On the main PCB, isolate the gate drive to the T0−247 SiC MOSFET. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the T0−247. If there is no series component between the PWM signal source and the T0−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the T0−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a T0−247 discrete is installed in the main PCB, remove it now.
4. Place Kapton or non−conductive tape over the main PCB area directly beneath the mini EVB. This is to avoid the possibility of having any components on the bottom of the mini EVB touch components or conductive surfaces on the main PCB.
5. Solder a flying lead of bus wire to the main PCB, PWM signal. Make sure there is enough length of the PWM input (flying lead) to reach through the mini EVB plated thru−hole (J3 or J4)
6. For non−inverting PWM input logic, verify that R5 (0 Ω) is installed and R6 is removed. This is the correct configuration of the mini EVB for non−inverting PWM input logic.
7. For inverting PWM input logic, verify that R6 (0 Ω) is installed and R5 is removed. This is the correct configuration of the mini EVB for inverting PWM input logic.
8. Solder the T0−247 through just the mini EVB first
9. With the T0−247 installed into the mini EVB, install and solder the T0−247 leads into the main PCB
10. Solder the other end of the PWM input (flying lead) to IN+ (J3) for non−inverting PWM applications or IN− (J4) for inverting PWM applications.
11. Using the same size bus wire, solder the remaining connections between J1, J2, J5 and J8 of the mini EVB to the appropriate locations on the main PCB.
12. Solder flying leads from J6−7 for bias voltage to the NCP51705. Note that J6−7 are across the isolation boundary from J1−5 and J8.

Mounting into Existing PCB − Option 2

If components mounted on the main PCB interfere with mounting the mini EVB as described by Option 1 (Figure 10), the T0−247 leads can be formed (lead length may need to be added) with the mini EVB mounted perpendicular to the main PCB as shown in Figure 11, option 2. If required, both mounting options allow the application of a heat sink to the T0−247 package. If high dV/dt is present on the drain of the T0−247, the EVB should be angled, away from being parallel to the T0−247, as much as possible.

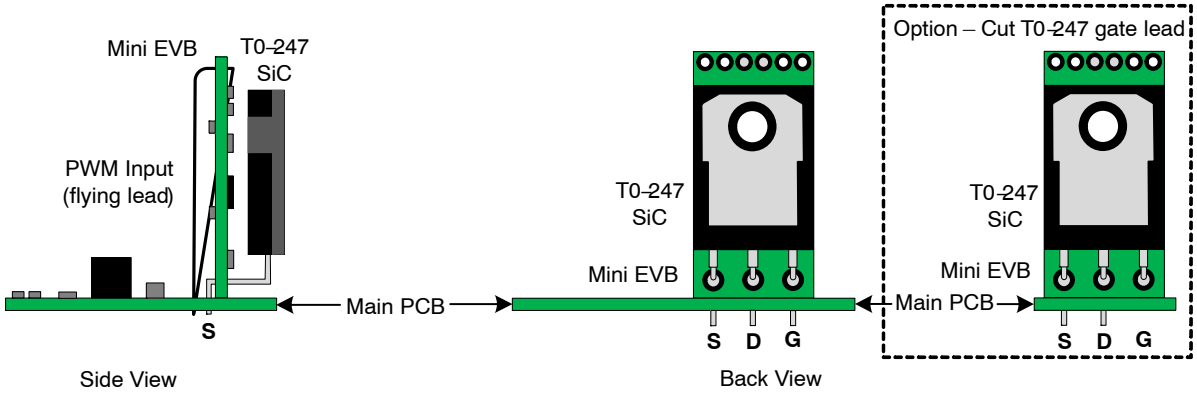

Figure 11. Mini EVB Installation − Option 2

Recommended Procedure for Option 2 Mounting into an Existing PCB

1. On the main PCB, isolate the gate drive to the T0−247 SiC MOSFET. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the T0−247. If there is no series component between the PWM signal source and the T0−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the T0−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a T0−247 discrete is installed in the main PCB, remove it now.
4. Solder a flying lead of bus wire to the main PCB, PWM signal. Make sure there is enough length of the PWM input (flying lead) to reach through the mini EVB plated thru−hole (J3 or J4)
5. For non−inverting PWM input logic, verify that R5 (0 Ω) is installed and R6 is removed. This is the correct configuration of the mini EVB for non−inverting PWM input logic.
6. For inverting PWM input logic, verify that R6 (0 Ω) is installed and R5 is removed. This is the correct configuration of the mini EVB for inverting PWM input logic.
7. Make appropriate modifications to lead form the T0−247 leads as shown in Figure 11. If the T0−247 leads are not long enough to provide sufficient clearance between the mini EVB and T0−247 case and allow the leads to pass through the mini EVB and down through the main PCB, then extending the lead length may be necessary.
8. After the T0−247 leads have been formed, check for fit through the mini EVB and down into the main PCB
9. Solder the T0−247 through just the mini EVB first
10. With the T0−247 installed into the mini EVB, install and solder the T0−247 leads into the main PCB
11. Solder the other end of the PWM input (flying lead) to IN+ (J3) for non−inverting PWM applications or IN− (J4) for inverting PWM applications.
12. Using the same size bus wire, solder the remaining connections between J1, J2, J5 and J8 of the mini EVB to the appropriate locations on the main PCB.
13. Solder flying leads from J6−7 for bias voltage to the NCP51705. Note that J6−7 are across the isolation boundary from J1−5 and J8.

Mounting into New PCB Design

The NCP51705, SiC Driver Mini EVB can also be used as an isolator+driver+T0−247 “driver module” that can be integrated into a new PCB design. The gate lead of the T0−247 between the mini EVB and the main PCB is for mechanical strength only. For main PCB layout, the gate lead extends down through the main PCB and can be soldered to an isolated plated thru−hole. As shown in Figure 12, shoulder pins with appropriate flange are one option that can be used as mounting pins between J1−8 of the mini EVB and the main PCB. Another option, shown in Figure 13, is to use a 100 mil center on center header which is a row of pins through a plastic header. The plastic header is used as a standoff for setting the mounting height between the mini EVB and the main PCB. The hole pattern for building a schematic library decal of the driver module is shown in Figure 14.

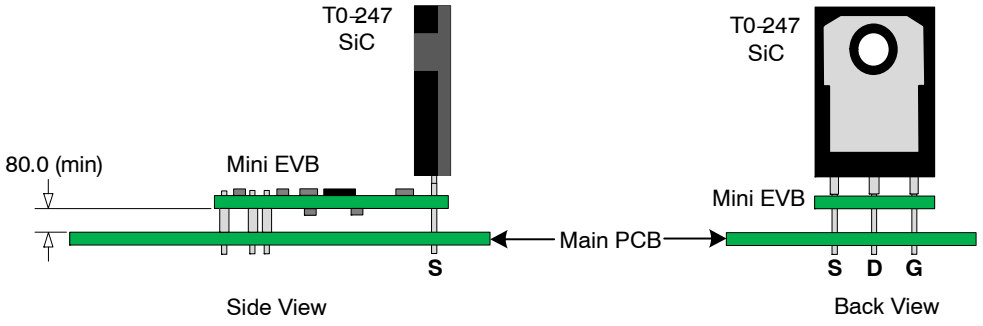

Figure 12. New PCB Design using Shoulder Pins (80 mil minimum mounting height)

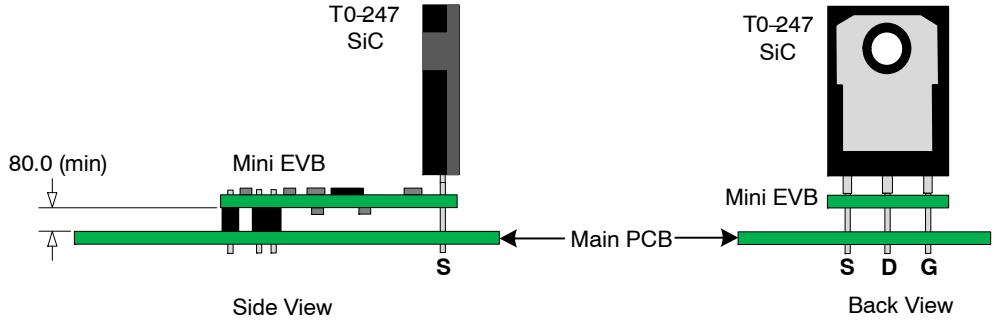

Figure 13. New PCB Design using 100 mil Interconnect Header Pins (80 mil minimum mounting height)

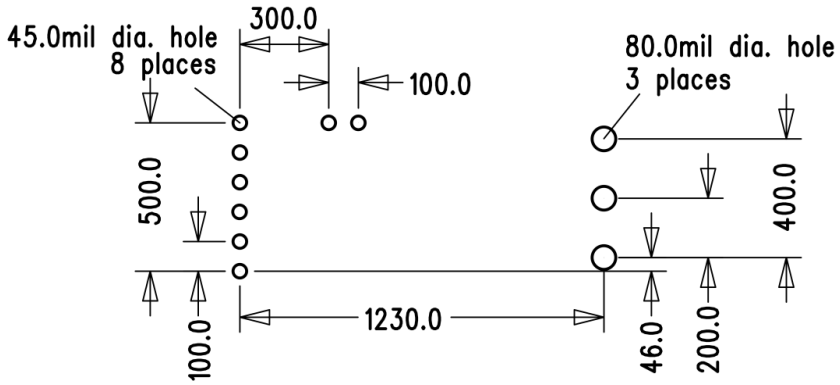

Figure 14. NCP51705 SiC Driver Mini EVB PCB Hole Pattern (All Dimensions in mils)

TESTING WITHOUT INSTALLING INTO A PCB

The NCP51705, SiC Driver Mini EVB can also be tested without installing into a main PCB. However, since this EVB was designed for small form factor there are no test points included for connecting voltage probes. The EVB should be hand probed carefully since the components are very fine pitch or flying leads connected to desired probe points can be attached. Note that the IN+/IN− PWM amplitude must be equal to the XVDD (5 V). The 20 V DC bias (VDD and GND) is on the secondary side of the digital isolator and therefore has a separate/isolated return ground from the 5 V DC bias (XVDD and XGND). The recommended series load of 470 pF and 4.99 Ω is close to what might be representative of a SiC gate drive input impedance. Leaded passive components can be soldered into the T0−247 holes as shown in Figure 15. Alternatively, a T0−247 SiC MOSFET can also be soldered in place for Q1 and used as a load for the NCP51705. Note that testing without installing into a power stage, leaves the DESAT pin open since there is no active drain signal. The effect of operating DESAT this way is explained in section ‘DESAT’.

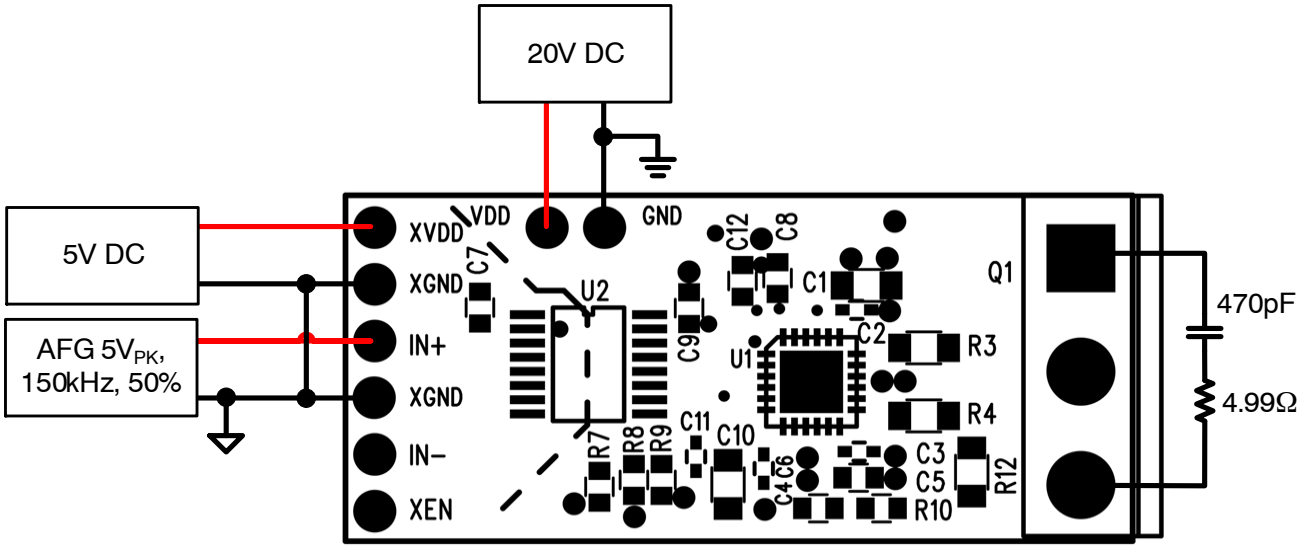

Figure 15. Test Configuration of EVB without Installing into Main PCB

Turn−on Procedure

1. Apply XVDD = 5 V (Voltage for primary side of the digital isolator, U2)
2. Apply VDD = 20 V (VDD bias voltage for the NCP5170, SiC driver, Note: $UVLO_{ON}$ = 17 V)
3. Apply IN+=5V_{PK}, 150 kHz, 50% (Reducing the frequency to less than ~90 kHz will show DESAT active as described in section ‘DESAT’)

VEE

The EVB is preconfigured for VEE=0V. Operating the EVB this way will result in switching between 0V < OUT < VDD. Several other options for negative VEE configuration are easily set by removing/installing resistors according to Table 3. Note that R10 must be removed for any VEE configuration other than 0 V. VDD_{UVLO} is programmable by the UVSET resistor as described in section ‘UVSET’ but VEE_{UVLO} is fixed at 80% of the VEE regulate value. If desired, the NCP5170 internal VEE charge pump can be disabled and an external negative voltage can be applied to VEE. When providing VEE from an external negative voltage supply, it is recommended to apply VEE prior to VDD. Any time the internal VEE charge pump is disabled (VEESET = 0 V), VEE_{UVLO} is disabled and is therefore shown as “NA” in Table 3.

Table 3. VEESET CONFIGURATION OPTIONS

VEESET	COMMENT	VEE	VEE_{UVLO}
VDD	Install R7 = 0 Ω, Remove R8, R9, R10 9V < VEESET < VDD	−8 V	−6.4 V
V5V	Install R7 = 0 Ω, Remove R7, R9, R10	−5 V	−4 V
OPEN	Remove R7, R8, R9, R10	−3 V	−2.4 V
GND	Install R9 = R10 = 0 Ω, Remove R7, R8	0 V	NA
GND	Remove R7, R8, R9, R10. Apply negative external voltage within the range of −8V < V_{EXT} < 0V	$-V_{EXT}$	NA

UVSET

The UVSET function is set by R2 and determines the UVLO turn−on threshold. The EVB is preconfigured with R2 = 113 kΩ which equates to UVLO turn−on (V_{ON}) of ~17 V. The UVLO turn−on threshold can be changed by selecting R2 according to a desired UVLO turn−on threshold, V_{ON}:

$$R_2 = \frac{V_{ON}}{6 \times 25\mu A} \quad \text{(eq. 1)}$$

DESAT

DESAT is a type of over−current protection dedicated to monitoring the $I_D x R_{DS}$ of the SiC MOSFET. The EVB is preconfigured with R11 = 4.99 kΩ (DESAT resistor). The internal DESAT threshold is fixed at $V_{DESAT(TH)}$=7.5V and the DESAT signal amplitude is adjustable by R11. R11 = 4.99 kΩ may not be the correct resistor value for some applications. If V_{DESAT} > 7.5 V during normal operation, decrease R11 to lower the signal amplitude. If DESAT is active, the trailing edge of the OUT pulse is terminated or reduced with respect to the input pulse (IN+). The waveforms shown in Figure 16, show VDESAT < 7.5 V during normal, 80 kHz, operation. Since DESAT is operating with no load, the amplitude is varied by varying the IN+ frequency. Figure 17 shows IN+ increased to 150 kHz and VDESAT = 7.5 V. The trailing edge of OUT is clearly terminated compared to IN+ indicating that DESAT is active.

WAVEFORMS

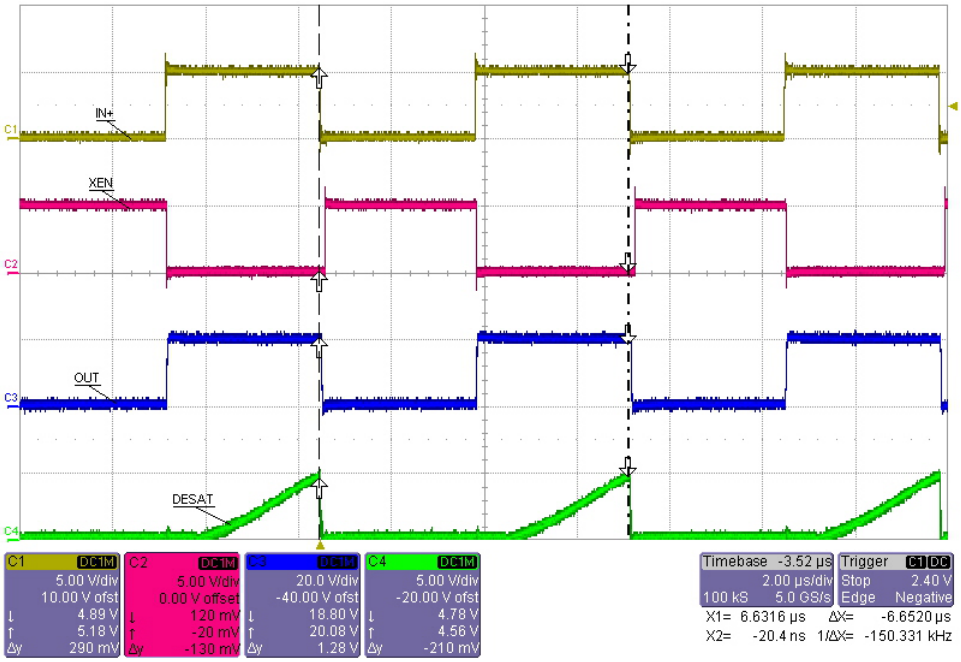

Figure 16. IN+ = 150 kHz, 50%, VDESAT = 5 V, DESAT Inactive

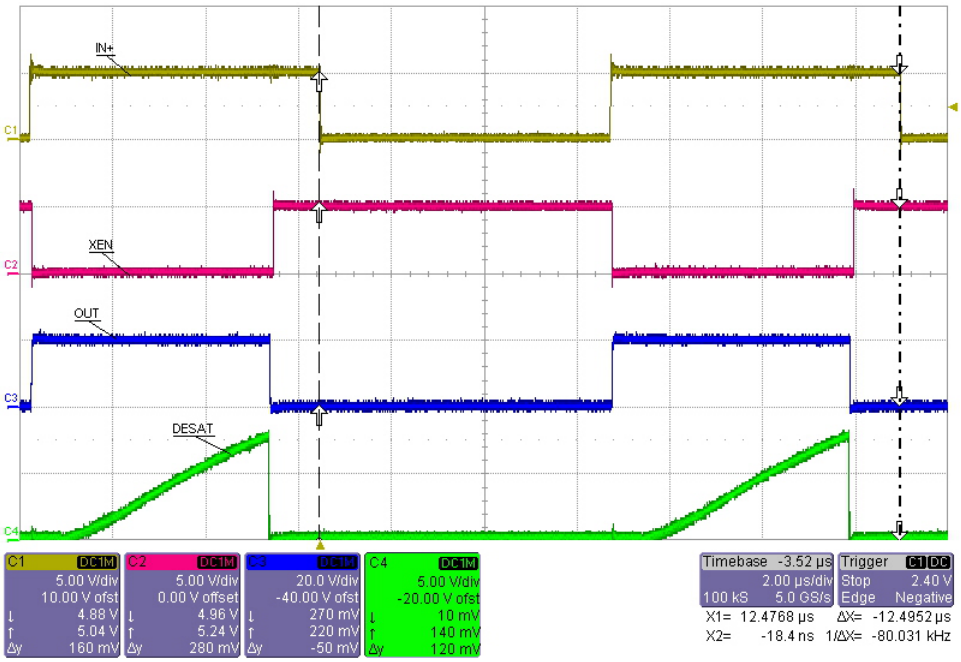

Figure 17. IN+ = 80 kHz, 50%, VDESAT = 7.5 V, DESAT Active

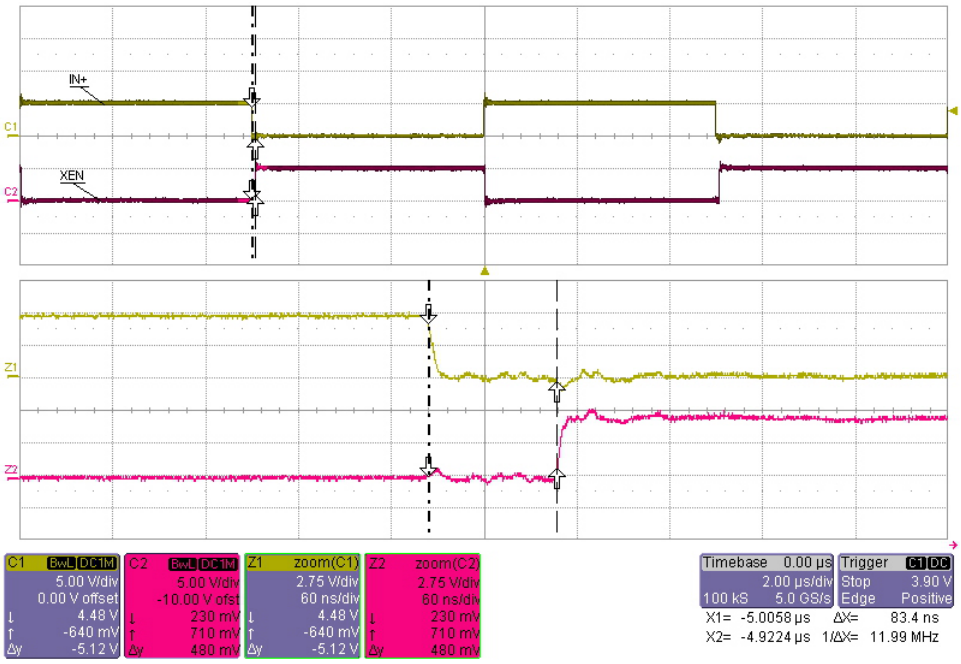

Figure 18. IN+ Falling to XEN Rising Delay, tD1 = 83 ns

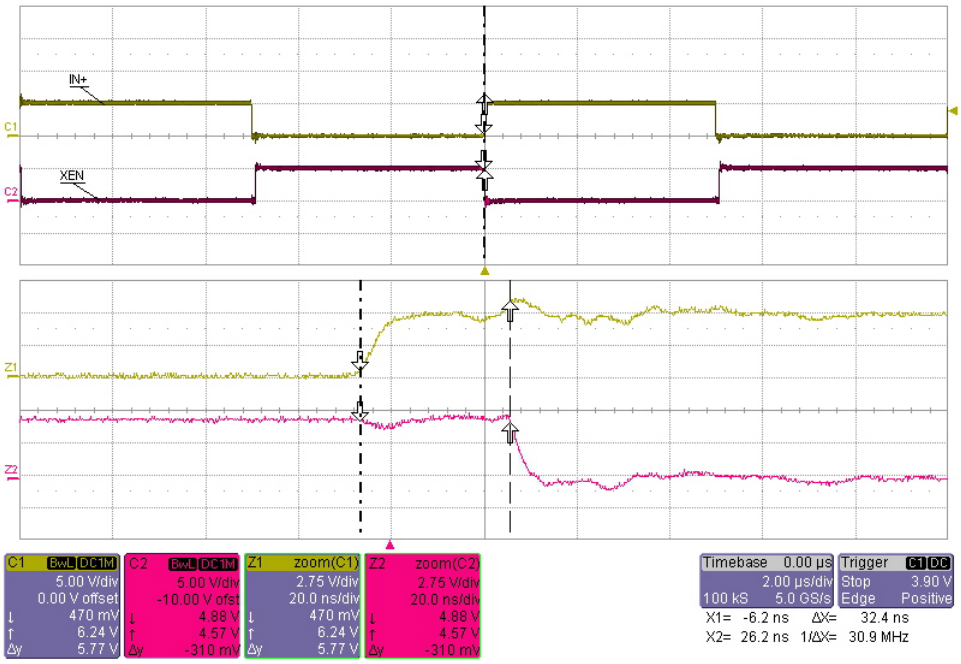

Figure 19. IN+ Rising to XEN Falling Delay, tD2 = 34 ns

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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