Synchronous Buck Regulator

3 MHz, 500 mA / 750 mA

FAN5362

Description

The FAN5362 is a 500 mA or 750 mA, step−down, switching voltage regulator that delivers a fixed output voltage from an input voltage supply of 2.7 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN5362 is capable of delivering a peak efficiency of 96%, while maintaining efficiency over 90% with load currents as low as 1 mA.

This regulator transitions seamlessly into and out of 100% duty cycle operation when the supply dips to or below the regulation setpoint and smoothly recovers full regulation without overshoot when the supply recovers.

The regulator operates at a nominal fixed frequency of 3 MHz, which reduces the value of the external components to 1 μH for the output inductor and 4.7 μF for the output capacitor. The PWM modulator can be synchronized to an external frequency source.

At moderate and light loads, pulse frequency modulation is used to operate the device in power−save mode with a typical quiescent current of 45 μA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed−frequency control, operating at 3 MHz. In shutdown mode, the supply current drops below 1 μA, reducing power consumption. For applications that require minimum ripple or fixed frequency, PFM mode can be disabled using the MODE pin.

The FAN5362 is available in 6−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP) and 6−Lead 2 x 2 mm Ultrathin Molded Leadless Package (UMLP).

Features

- 3 MHz Fixed−Frequency Operation
- 45 μA Typical Quiescent Current
- 1.80 V to 3.6 V Fixed Output Voltage
- 500 mA or 750 mA Output Current Capability
- 2.7 V to 5.5 V Input Voltage Range
- Smooth Transitions to/from 100% Duty Cycle when V_{IN} Drops
- PFM Mode for High Efficiency in Light Load
- Best−in−Class Load Transient Response
- Best−in−Class Efficiency
- Forced PWM and External Clock Synchronization
- Internal Soft−Start
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 6−Bump WLCSP, 0.4 mm Pitch or 6−Lead 2 x 2 mm Ultrathin Molded Leadless Package
- These Devices are Pb−Free and Halogen Free

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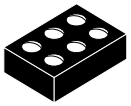
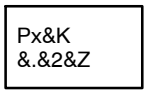


WLCSP6 1.31x0.96x0.586
CASE 567RS

MARKING DIAGRAMS



Px	= Device Code x = J, G, H
&K	= One Digit Date Code
&.	= Pin One Dot
&2	= 2 Digit Code
&Z	= Assembly Plant Code

UDFN6 2x2, 0.65P
CASE 517DR

&Z	= Assembly Plant Code
&2	= 2 Digit Code
&K	= One Digit Date Code
62x	= Device Code x = C, B

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

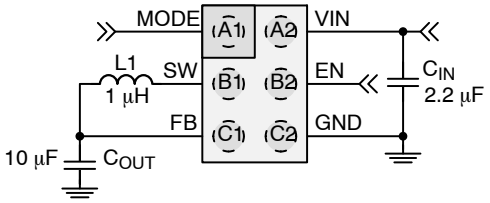


Figure 1. Typical Application

Applications

- SD Flash Memory Power Supply
- RF Transceiver Power
- Cell Phones, Smart Phones
- Tablets, Netbooks, Ultra−Mobile PCs
- 3G, LTE, WiMAX™, WiBro®, and WiFi® Data Cards
- Gaming Devices, Digital Cameras DC/DC Micro Modules

Table 1. ORDERING INFORMATION

Part Number	Output Voltage (Note 1)	Output Current (mA)	Operating Temperature Range	Package	Shipping†
FAN5362UC27X (Note 2)	2.7	500	−40 to 85°C	WLCSP−6, 0.4 mm Pitch	3000 / Tape & Reel
FAN5362UC29X (Note 2)	2.9				
FAN5362UC33X (Note 2)	3.3				
FAN5362UMP29X (Note 2)	2.9			6−Lead, 2x2 mm UMLP	3000 / Tape & Reel
FAN5362UMP33X	3.3				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. Other voltage options may be available upon request.
2. This device is End of Life. Please contact Sales for additional information and assistance with replacement devices.

Table 2. RECOMMENDED COMPONENTS FOR CIRCUIT IN FIGURE 1

Component	Description	Example Part	Typ.
L1	1 μH, 2012, 190 mΩ, 800 mA	Murata LQM21PN1R0MC0	1 μH
C_{IN}	2.2 μF, 6.3 V, X5R, 0402	Murata GRM155R60J225ME15	2.2 μF
	2.2 μF, 6.3 V, X5R, 0603	GRM188R60J225KE19D	
C_{OUT}	4.7 μF, X5R, 0603	Murata GRM188R60J475M	4.7 μF
	10 μF, X5R, 0603	Murata GRM188R60J106ME47D	10 μF

PIN CONFIGURATION

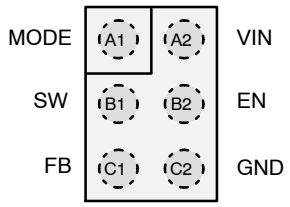


Figure 2. WLCSP, Bumps Facing Down

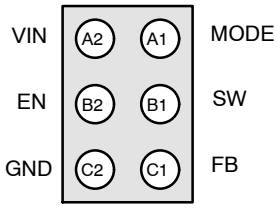


Figure 3. WLCSP, Bumps Facing Up

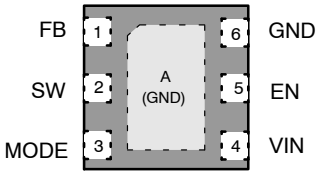


Figure 4. UMLP, Leads Facing Down

Table 3. PIN DEFINITIONS

WLCSP Bump #	UMLP Pin #	Name	Description
A1	3	MODE	Logic 1 on this pin forces the IC to stay in PWM mode. Logic 0 allows the IC to automatically switch to PFM during light loads. The regulator also synchronizes its switching frequency to two times the frequency provided on this pin. Do not leave this pin floating. When tying HIGH, use at least 1 kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
B1	2	SW	**Switching Node**. Connect to output inductor.
C1	1	FB	**Feedback** / **VOUT**. Connect to output voltage.
C2	6	GND	**Ground**. Power and IC ground. All signals are referenced to this pin.
B2	5	EN	**Enable**. The device is in shutdown mode when voltage to this pin is < 0.4 V and enabled when > 1.2 V. Do not leave this pin floating. When tying HIGH, use at least 1 kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
A2	4	VIN	**Input Voltage**. Connect to input power source.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	Input Voltage		−0.3	6.5	V
V_{SW}	Voltage on SW Pin		−0.3	V_{IN} + 0.3 (Note 3)	V
V_{CTRL}	EN and MODE Pin Voltage		−0.3	V_{IN} + 0.3 (Note 3)	V
V_{FB}	FB Pin		−0.3	4	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114	3.0		kV
		Charged Device Model per JESD22−C101	1.5		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
3. Lesser of 6.5 V or V_{IN} + 0.3 V.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range	2.7 (Note 4)		5.5	V
I_{OUT}	Output Current for 2.1 V	0		750	mA
	Output Current for 2.5 V, 2.7 V, 2.9 V, 3.3 V	0		500	
L	Inductor		1		μH
C_{IN}	Input Capacitor		2.2		μF
C_{OUT}	Output Capacitor		10	24	μF
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
4. Minimum V_{IN} = V_{OUT} + 200 mV or 2.7 V, whichever is greater.

Table 6. THERMAL PROPERTIES

Symbol	Parameter		Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance,	WLSCP	150	°C/W
		UMLP	49	

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer 1s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Table 7. ELECTRICAL CHARACTERISTICS

(Minimum and maximum values are at V_{IN} = V_{EN} = 2.7 V to 5.5 V, V_{MODE} = 0 V (AUTO Mode), T_A = −40°C to + 85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 V, C_{OUT} = 10 μF.)

Symbol	Parameter		Condition	Min	Typ	Max	Unit
POWER SUPPLIES							
I_Q	Quiescent Current		No Load, Not Switching, V_{IN} > 3 V		45	75	μA
			PWM Mode		5		mA
$I_{(SD)}$	Shutdown Supply Current		EN = GND		0.05	1.00	μA
V_{UVLO}	Under−Voltage Lockout Threshold		Rising V_{IN}		2.5	2.6	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis				175		mV
$V_{(ENH)}$	Enable HIGH−Level Input Voltage			1.05			V
$I_{(ENL)}$	Enable LOW−Level Input Voltage					0.4	V
$I_{(EN)}$	Enable Input Leakage Current		EN to V_{IN} or GND		0.01	1.00	μA
$V_{(MH)}$	MODE HIGH−Level Input Voltage			1.05			V
$V_{(ML)}$	MODE LOW−Level Input Voltage					0.4	V
$I_{(M)}$	MODE Input Leakage Current		MODE to V_{IN} or GND		0.01	1.00	μA
SWIITCHING AND SYNCHRONIZATION							
f_{SW}	Switching Frequency (Note 5)		V_{IN} = 3.6 V, T_A = 25°C	2.7	3.0	3.3	MHz
f_{SYNC}	MODE Synchronization Range (Note 5)		Square Wave at MODE Input	1.3	1.5	1.7	MHz
REGULATION							
V_O	Output Voltage Accuracy	2.10 V	I_{LOAD} = 0 to 750 mA	2.037 (−3%)	2.100	2.163 (+3%)	V
		2.50 V	I_{LOAD} = 0 to 400 mA, $V_{IN} \geq V_{OUT}$ + 200 mV	2.375 (−5%)	2.500	2.575 (+3%)	
			I_{LOAD} = 0 to 500 mA, $V_{IN} \geq V_{OUT}$ + 300 mV	2.425 (−3%)	2.500	2.575 (+3%)	
		2.70 V, 2.90 V 3.30 V	I_{LOAD} = 0 to 400 mA, $V_{IN} \geq V_{OUT}$ + 150 mV	−5%		+3%	
			I_{LOAD} = 0 to 500 mA, $V_{IN} \geq V_{OUT}$ + 300 mV	−3%		+3%	
t_{SS}	Soft−Start		From EN Rising Edge		180	300	μs
OUTPUT DRIVER							
$R_{DS(on)}$	PMOS On Resistance		V_{IN} = V_{GS} = 3.6 V		330		mΩ
	NMOS On Resistance		V_{IN} = V_{GS} = 3.6 V		300		
$I_{LIM(OL)}$	PMOS Peak Current Limit (Note 5)		V_{OUT} = 2.1 V		1375		mA
			V_{OUT} = 2.1 V, 2.7 V, 2.9 V, 3.3 V	800	1000	1150	
T_{TSD}	Under−Voltage Lockout Threshold				150		°C
T_{HYS}	Under−Voltage Lockout Hysteresis				15		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Limited by the effect of t_{OFF} minimum (see Figure 8 in Typical Performance Characteristics).
6. The Electrical Characteristics table reflects open−loop data. Refer to the Operation Description and Typical Characteristics for closed−loop data.

TYPICAL CHARACTERISTICS

(Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 (AUTO), V_{OUT} = 2.9 V, C_{OUT} = 10 μF, T_A = 25°C.)

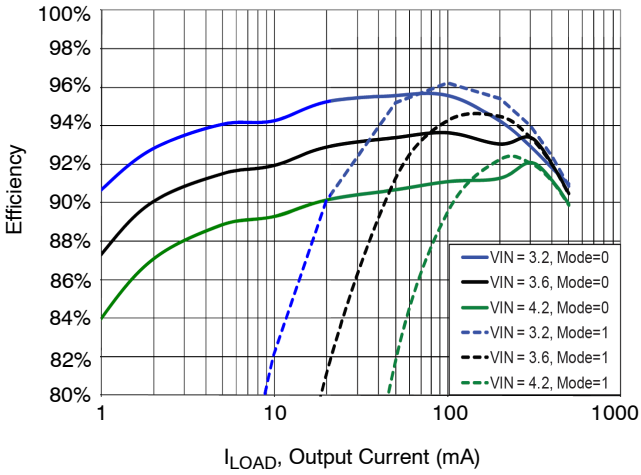


Figure 5. Efficiency vs. Load Current and Input Supply

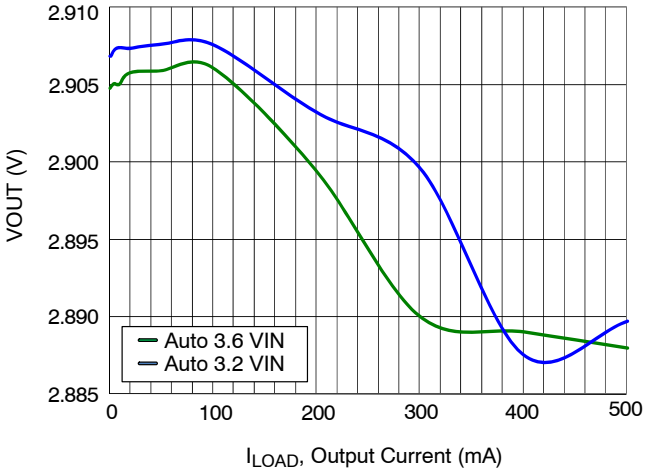


Figure 6. Load Regulation

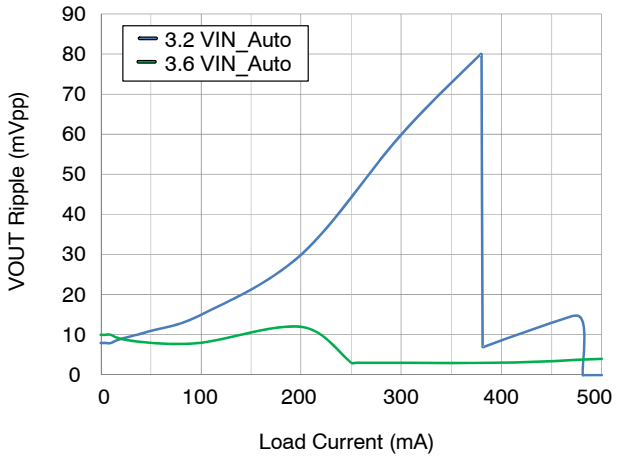


Figure 7. Ripple

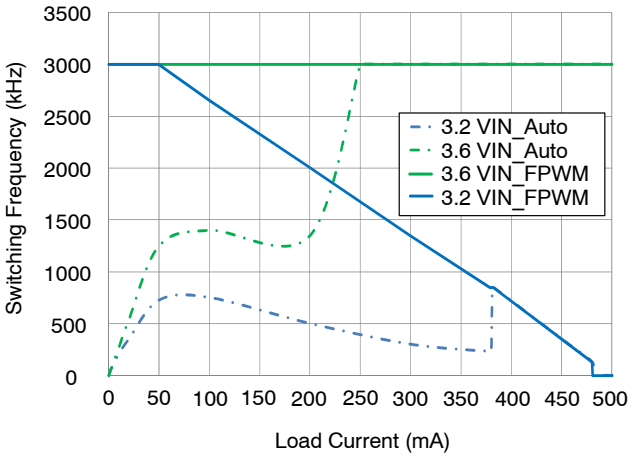


Figure 8. Effect of $t_{OFF(MIN)}$ on Reducing Switching Frequency

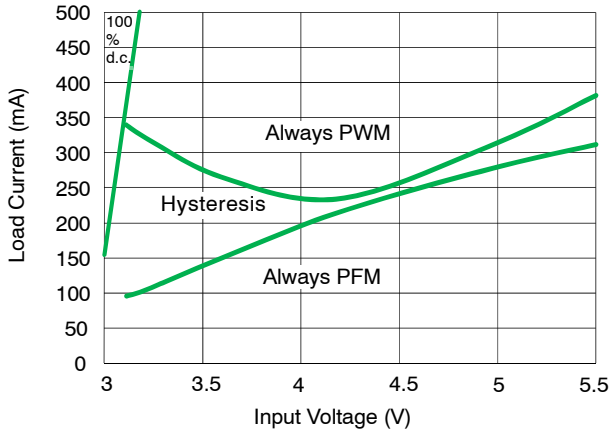


Figure 9. PFM / PWM Boundaries

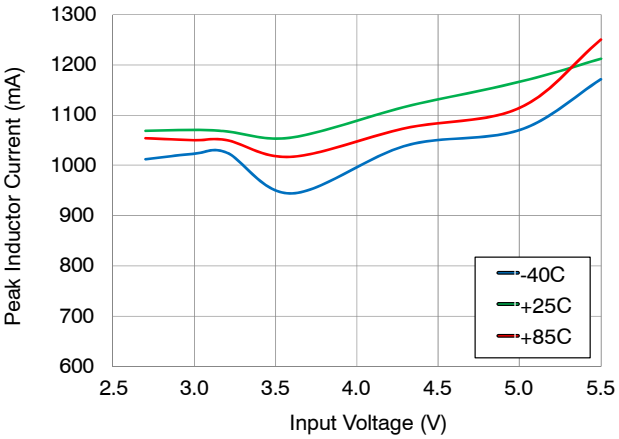


Figure 10. Peak Inductor Current

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 (AUTO), V_{OUT} = 2.9 V, C_{OUT} = 10 μF, T_A = 25°C.)

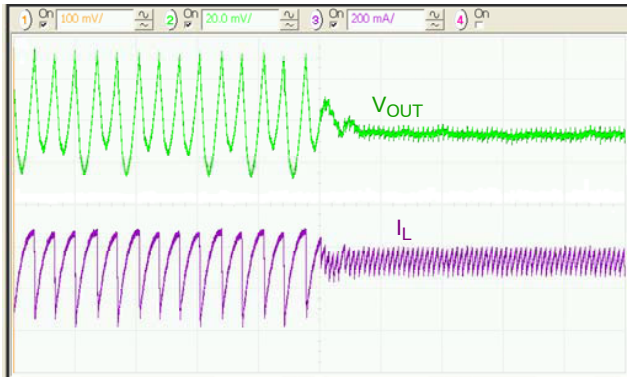


Figure 11. PFM to PWM Transition at V_{IN} = 3.2 V, 10 μs/div

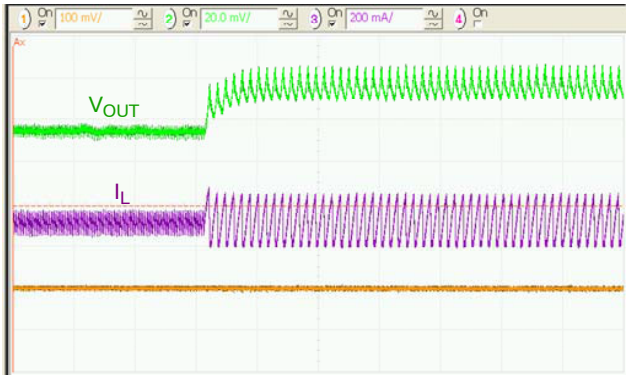


Figure 12. PWM to PFM Transition at V_{IN} = 3.2 V, 10 μs/div

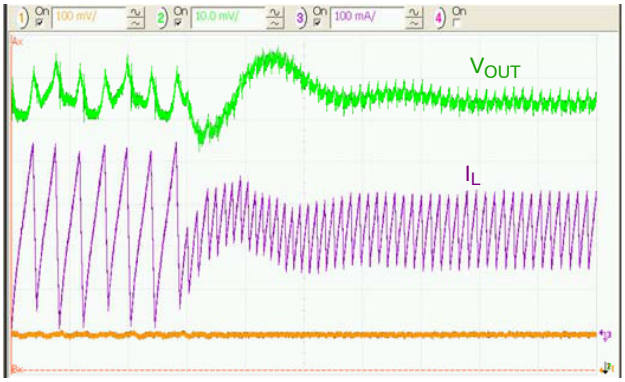


Figure 13. PFM to PWM Transition at V_{IN} = 3.6 V, 2 μs/div

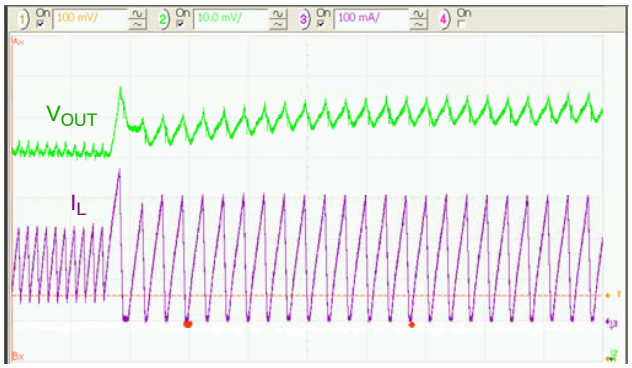


Figure 14. PWM to PFM Transition at V_{IN} = 3.6 V, 2 μs/div

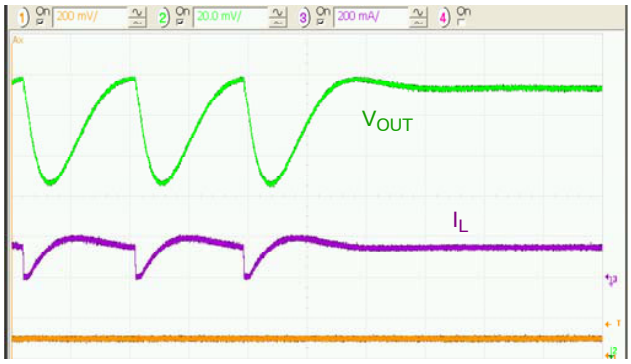


Figure 15. Regular Switching to 100% Duty Cycle Transition at V_{IN} = 3.2 V, 5 μs/div

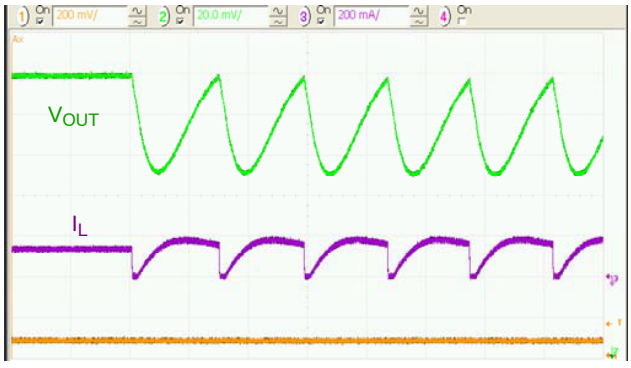


Figure 16. 100% Duty Cycle to Regular Switching Transition at V_{IN} = 3.2 V, 5 μs/div

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 (AUTO), V_{OUT} = 2.9 V, C_{OUT} = 10 μF, T_A = 25°C.)

Figure 17. Startup Ramping V_{IN} = V_{EN} with 500 mA Load, 1 ms/div.

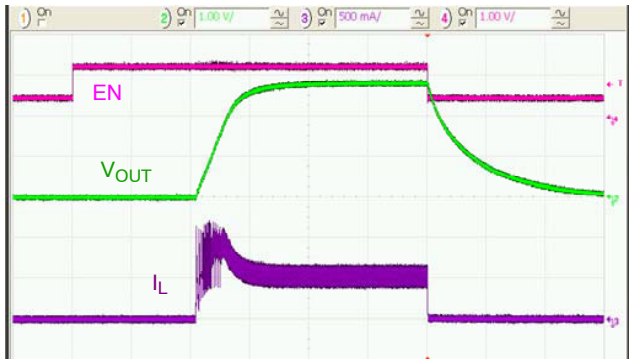


Figure 18. Startup and Shutdown through V_{EN} with 500 mA Load, 50 μs/div.

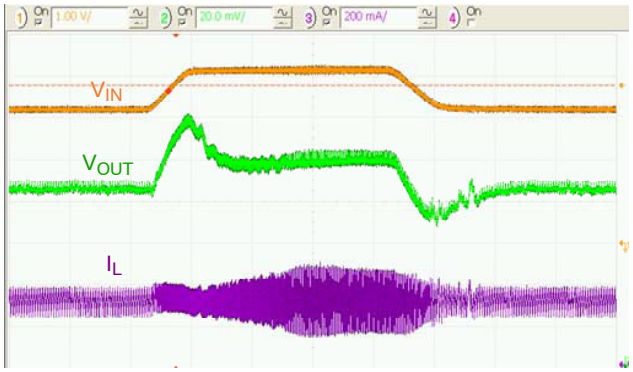


Figure 19. Line Transient at V_{IN} = 3.2 V to 4.2 V, 300 mA Load, t_{RISE} = t_{FALL} = 10 μs, 20 μs/div.

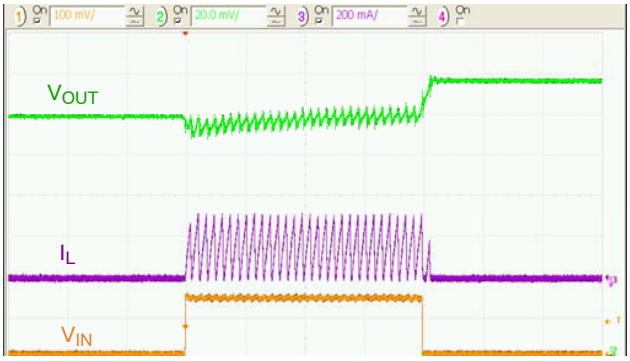


Figure 20. Load Transient 0 mA to 150 mA, V_{IN} = 3.6 V, t_{RISE} = t_{FALL} = 100 ns, 5 μs/div.

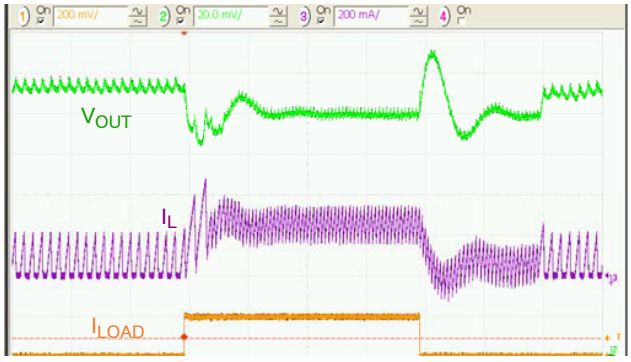


Figure 21. Load Transient 50 mA to 250 mA, V_{IN} = 3.6 V, t_{RISE} = t_{FAll} = 100 ns, 5 μs/div.

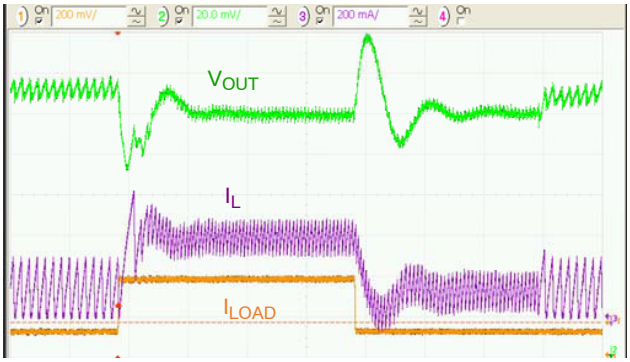


Figure 22. Load Transient 150 mA to 400 mA, V_{IN} = 3.6 V, t_{RISE} = t_{FALL} = 100 ns, 5 μs/div.

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 (AUTO), V_{OUT} = 2.9 V, C_{OUT} = 10 μF, T_A = 25°C.)

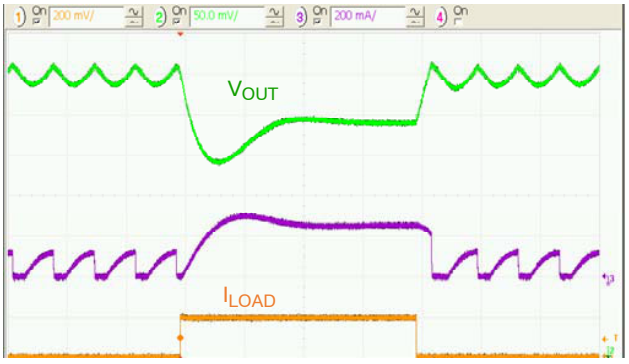


Figure 23. Load Transient 50 mA to 250 mA, V_{IN} = 3 V, t_{RISE} = t_{FALL} = 100 ns, 5 μs/div.

Figure 24. Load Transient 150 mA to 400 mA, V_{IN} = 3 V, t_{RISE} = t_{FALL} = 100 ns, 5 μs/div.

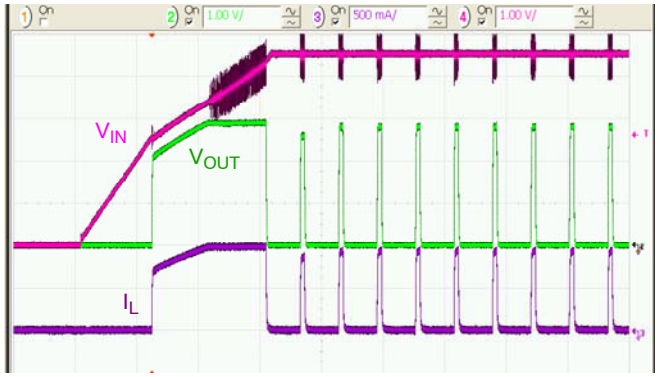


Figure 25. Startup Ramping V_{IN} = V_{EN}, into Overload, Load = 3 Ω, 5 ms/div.

OPERATION DESCRIPTION

FAN5362 is a 500 mA or 750 mA, step−down switching voltage regulator that delivers a fixed output voltage from an input voltage supply up to 5.5 V. Using a proprietary architecture with synchronous rectification, FAN5362 is capable of delivering a peak efficiency above 96%, while maintaining efficiency above 90% at load currents as low as 1 mA. The regulator operates at a nominal frequency of 3 MHz at full load, which reduces the value of the external components to 1 μH for the inductor and 4.7 μF for the output capacitor. High efficiency is maintained at light load with single−pulse PFM mode.

Control Scheme

The FAN5362 uses a proprietary, non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN5362 operates in discontinuous current (DCM) single−pulse PFM mode, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 18 mV at V_{OUT} during the transition between DCM and CCM modes.

Combined with exceptional transient response characteristics, the very low quiescent current of the controller (45 μA) maintains high efficiency, even at very light loads, while preserving fast transient response for applications requiring tight output regulation.

100% Duty Cycle Operation

When V_{IN} approaches V_{OUT}, the regulator increases its duty cycle until 100% duty cycle is reached. As the duty cycle approaches 100%, the switching frequency declines due to the minimum off−time ($t_{OFF(MIN)}$) of about 35 ns imposed by the control circuit. When 100% duty cycle is reached, V_{OUT} follows V_{IN} with a drop−out voltage ($V_{DROPOUT}$) determined by the total resistance between V_{IN} and V_{OUT}:

$$V_{DROPOUT} = I_{LOAD} \cdot \left(PMOSR_{DS(ON)} + DCR_L\right) \quad \text{(eq. 1)}$$

To calculate the worst−case $V_{DROPOUT}$, use the maximum PMOS $R_{DS(ON)}$ at high temperature from Figure 6.

Enable and Soft Start

When the EN pin is LOW, the IC is shut down and the part draws very little current. In addition, during shutdown, FB is actively discharged to ground through a 230 Ω path. Raising EN above its threshold voltage activates the part and starts the soft−start cycle. During soft−start, the internal reference is ramped using an exponential RC shape to prevent any overshoot of the output voltage. Current limiting minimizes inrush during soft−start.

Synchronous rectification is inhibited during soft−start, allowing the IC to start into a pre−charged load.

The IC may fail to start if heavy load is applied during startup and/or if excessive C_{OUT} is used. This is due to the current−limit fault response, which protects the IC in the event of an over−current condition present during soft−start.

The current required to charge COUT during soft−start is commonly referred to as “displacement current” and given as:

$$I_{DISP} = C_{OUT} \cdot \frac{dV}{dt} \quad \text{(eq. 2)}$$

where $\frac{dV}{dt}$ refers to the soft−start slew rate.

To prevent shutdown during soft−start, the following condition must be met:

$$I_{DISP} + I_{LOAD} < I_{MAX(DC)} \quad \text{(eq. 3)}$$

where $I_{MAX(DC)}$ is the maximum load current the IC is guaranteed to support (500 mA or 750 mA).

MODE Pin

Logic 1 on this pin forces the IC to stay in PWM mode. A logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled, the converter synchronizes its switching frequency to four times the frequency on the mode pin (f_{MODE}).

At startup, the mode pin must be held LOW or HIGH for at least 10 μs to ensure that the converter does not attempt to synchronize to this pin.

Under−Voltage Lockout

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. 16 consecutive PWM cycles in current limit causes the regulator to shut down and stay off for about 2900 μs before attempting a restart.

In the event of a short circuit, the soft−start circuit attempts to restart at 240 μs, which results in a duty cycle of less than 10%, providing current into a short.

The closed−loop peak−current limit, $I_{LIM(PK)}$, is not the same as the open−loop tested current limit, $I_{LIM(OL)}$, in the Electrical Characteristics table. This is primarily due to the effect of propagation delays of the IC current limit comparator.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 20°C hysteresis.

Minimum Off−Time Effect on Switching Frequency

$t_{OFF(MIN)}$ is 35 ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN5362 can provide, or the maximum output voltage it can provide at low V_{OUT} while maintaining a fixed switching frequency in PWM mode.

When V_{IN} is high, fixed switching is maintained as long as $\frac{V_{OUT}}{V_{IN}} \le 1 - t_{OFF(MIN)} \cdot f_{SW} \approx 0.7$.

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 3 MHz to maintain regulation. This occurs when V_{IN} is below 3.3 V at nominal load currents.

The calculation for switching frequency is given by:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, 3MHz\right) \quad \text{(eq. 4)}$$

where:

$$t_{SW(MAX)} = 35ns \cdot \left(1 + \frac{V_{OUT} + I_{OUT} \cdot R_{OFF}}{V_{IN} - I_{OUT} \cdot R_{ON} - V_{OUT}}\right) \quad \text{(eq. 5)}$$

where:

$R_{OFF} = R_{DSON\_N} + DCR_L$

$R_{ON} = R_{DSON\_P} + DCR_L$

APPLICATION INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application.

The inductor value affects the average current limit, the PWM−to−PFM transition point, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}}\right) \quad \text{(eq. 6)}$$

The maximum average load current, $I_{MAX(LOAD)}$ is related to the peak current limit, $I_{LIM(PK)}$ by the ripple current:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad \text{(eq. 7)}$$

The FAN5362 is optimized for operation with L = 1 μH, but is stable with inductances up to 1.5 μH (nominal) and down to 470 nH. The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current that the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}} \quad \text{(eq. 8)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Inductor Current Rating

The FAN5362's current limit circuit can allow a peak current of 1.25 A to flow through L1 under worst−case conditions. If it is possible for the load to draw that much continuous current, the inductor should be capable of sustaining that current or failing in a safe manner.

Output Capacitor

While 4.7 μF capacitors are available in 0402 package size, 0603 capacitors are recommended due to the severe DC voltage bias degradation in capacitance value that the 0402 exhibits.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I \cdot \left(\frac{1}{8 \cdot C_{OUT} \cdot f_{SW}} + ESR\right) \quad \text{(eq. 9)}$$

If values greater than 24 μF of C_{OUT} are used, the regulator may fail to start. See the sections on Enable and Soft Start for more information.

Input Capacitor

The 2.2 μF ceramic input capacitor should be placed as close as possible to the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

PCB LAYOUT GUIDELINES

There are only three external components: the inductor, input capacitor, and the output capacitor. For any buck switcher IC, including the FAN5362, it is important to place a low−ESR input capacitor very close to the IC, as shown in Figure 26. The input capacitor ensures good input decoupling, which helps reduce noise appearing at the output terminals and ensures that the control sections of the IC do not behave erratically due to excessive noise. This reduces switching cycle jitter and ensures good overall performance. It is important to place the common GND of C_{IN} and C_{OUT} as close as possible to the C2 terminal. There is some flexibility in moving the inductor further away from the IC; in that case, V_{OUT} should be considered at the C_{OUT} terminal.

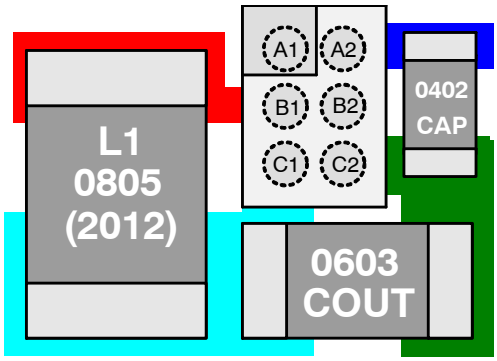
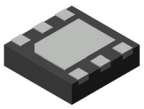


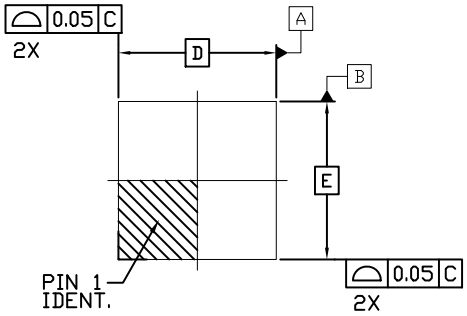
Figure 26. PCB Layout Recommendation

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

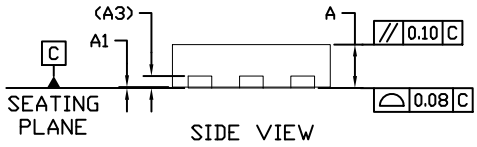


UDFN6 2x2, 0.65P
CASE 517DR
ISSUE A

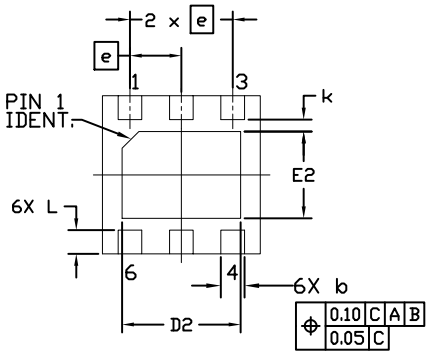
DATE 25 JAN 2022



TOP VIEW



SIDE VIEW

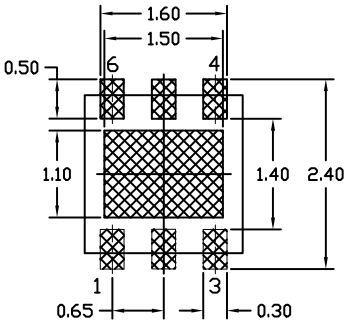


BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	-	-	0.55
A1	0.00	-	0.05
A3	0.15 REF.		
b	0.25	0.30	0.35
D	2.00 BSC		
D2	-	-	1.50
E	2.00 BSC		
E2	-	-	1.10
e	0.65 BSC		
k	0.15		
L	0.25	-	0.35

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2018
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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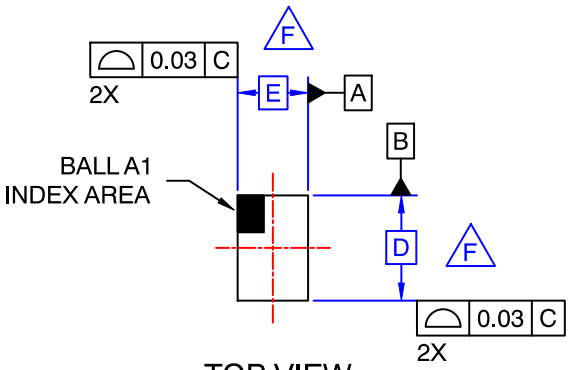
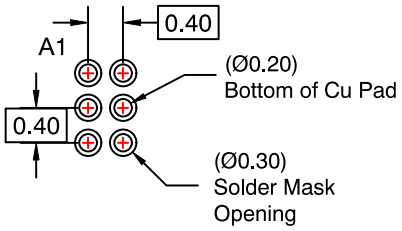
WLCSP6 1.31x0.96x0.586
CASE 567RS
ISSUE O

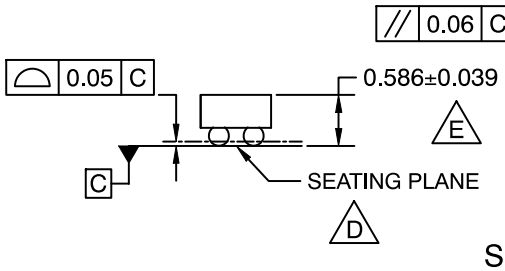
DATE 30 NOV 2016

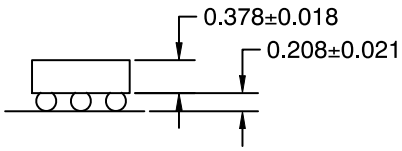


TOP VIEW

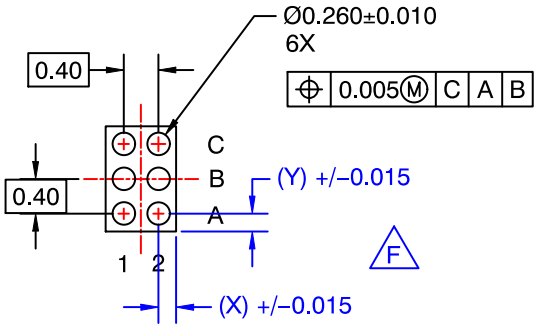


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 2009.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547−625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y, SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP6 1.31x0.96x0.586**		**PAGE 1 OF 1**

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