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High-Voltage Switcher for Low Power Offline SMPS

NCP1060, NCP1063

The NCP106X products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a PDIP−7, SOIC−10 or SOIC−16 package, the NCP106X offer a high level of integration, including soft−start, frequency−jittering, short−circuit protection, skip−cycle, adjustable peak current set point, ramp compensation, and a Dynamic Self−Supply (eliminating the need for an auxiliary winding).

Unlike other monolithic solutions, the NCP106X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (60 kHz or 100 kHz). When the output power demand diminishes, the IC automatically enters frequency foldback mode and provides excellent efficiency at light loads. When the power demand reduces further, it enters into a skip mode to reduce the standby consumption down to a no load condition.

Protection features include: a timer to detect an overload or a short−circuit event, Overvoltage Protection with auto−recovery and AC input line voltage detection (A version).

The **onsemi** proprietary integrated Over Power Protection (OPP) lets you harness the maximum delivered power without affecting your standby performance simply via external resistors.

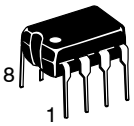
For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to reduce input power consumption below 50 mW at high line.

NCP106x can be seamlessly used both in non−isolated and in isolated topologies.

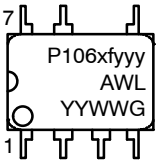
Features

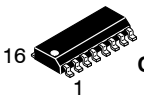
- Built−in 700 V MOSFET with $R_{DS(on)}$ of 34 Ω (NCP1060) and 11.4 Ω (NCP1063)
- Large Creepage Distance Between High−voltage Pins
- Current−Mode Fixed Frequency Operation – 60 kHz or 100 kHz (130 kHz on demand)
- Adjustable Peak Current: see below table
- Fixed Ramp Compensation
- Direct Feedback Connection for Non−isolated Converter
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Skip−Cycle Operation at Low Peak Currents Only
- Dynamic Self−Supply: No Need for an Auxiliary Winding
- Internal 4 ms Soft−Start
- Auto−Recovery Output Short Circuit Protection with Timer−Based Detection
- Auto−Recovery Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 50 mW
- Frequency Foldback to Improve Efficiency at Light Load
- These Devices are Pb−Free and are RoHS Compliant

MARKING DIAGRAMS



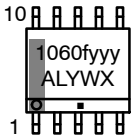
PDIP−7
CASE 626A
AP SUFFIX





SOIC−16
CASE 751B−05
D SUFFIX

SOIC−10
CASE 751BQ
AD or BD SUFFIX



x	= Power Switch Circuit On−state Resistance (0 = 34 Ω, 3 = 11.4 Ω)
f	= Brown In (A = Yes, B = No)
yyy	= Oscillator Frequency (060 = 60 kHz, 100 = 100 kHz)
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 28.

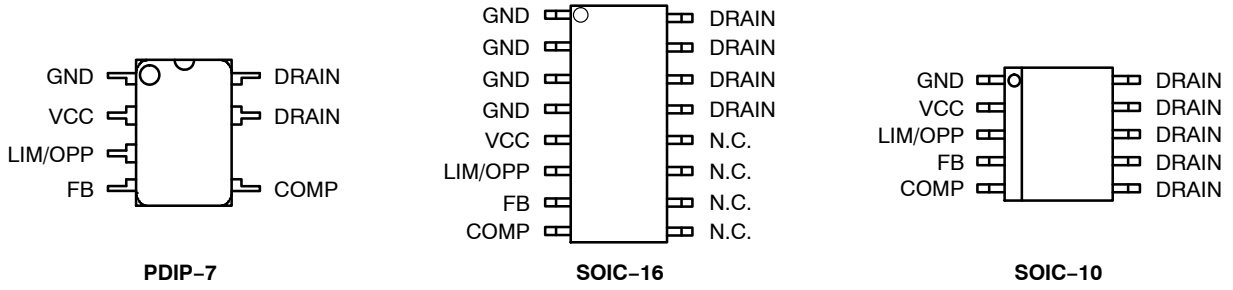
Typical Applications

- Auxiliary / Standby Isolated and Non−isolated Power Supplies
- Power Meter SMPS
- Wide Vin Low Power Industrial SMPS

Table 1. PRODUCT INFORMATION & INDICATIVE MAXIMUM OUTPUT POWER

Product	$R_{DS(on)}$	$I_{IPK(0)}$	230 Vac ± 15%		85 – 265 Vac	
			Adapter	Open Frame	Adapter	Open Frame
NCP1060 60 kHz	34 Ω	300 mA	3.3 W	8.3 W	1.9 W	4.7 W
NCP1063 100 kHz	11.4 Ω	780 mA	6.2 W	15.5 W	3.3 W	7.8 W

NOTE: Informative values only, with T_{amb} = 25°C, T_{case} = 100°C, PDIP−7 package, Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.



PDIP−7 **SOIC−16** **SOIC−10**

Figure 1. Pin Connections

Table 2. PIN FUNCTION DESCRIPTION

Pin No			Pin Name	Function	Pin Description
PDIP 7	SOIC 10	SOIC 16			
1	1	1−4	GND	The IC Ground	
2	2	5	V_{CC}	Powers the internal circuitry	This pin is connected to an external capacitor. The V_{DD} includes an auto−recovery over voltage protection.
3	3	6	LIM/OPP	Ipeak set / Over power limitation	The current drown from the pin decreases Ipeak of the primary winding. If resistive divider from the auxiliary winding is connected to this pin it sets the OPP compensation level (it diminishes the peak current.)
4	4	7	FB	Feedback signal input	This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider.
5	5	8	Comp	Compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto−coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
6		9−12			This un−connected pin ensures adequate creepage distance
7,8	6−10	13−16	Drain	Drain connection	The internal drain MOSFET connection

Table 3. TYPICAL APPLICATIONS

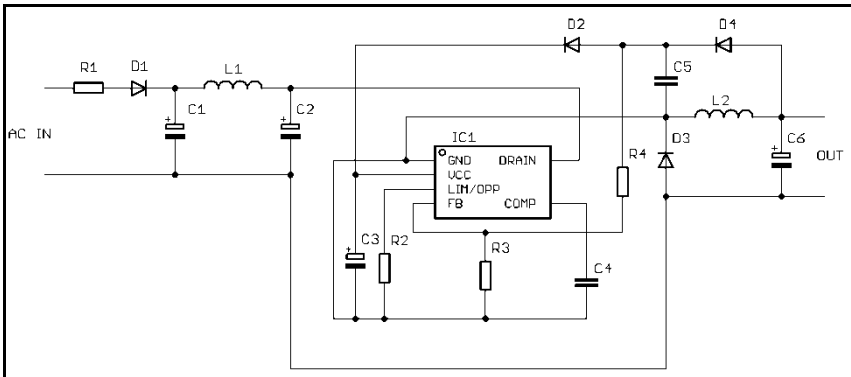
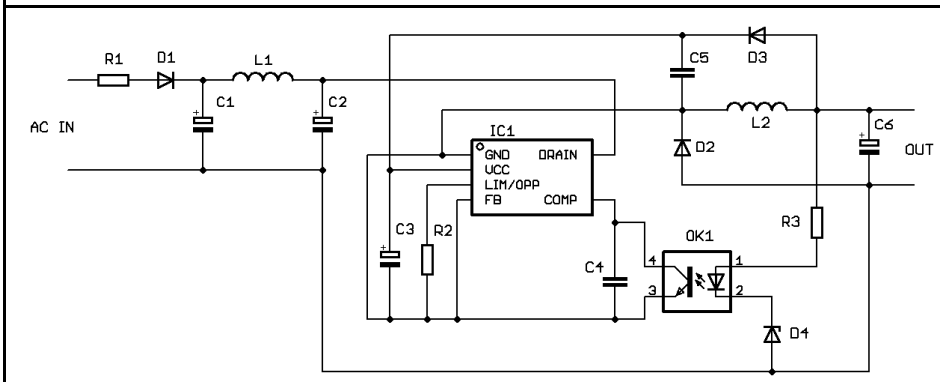
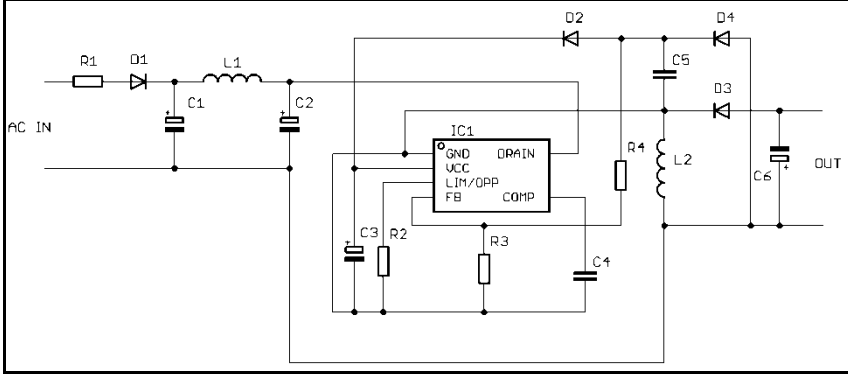
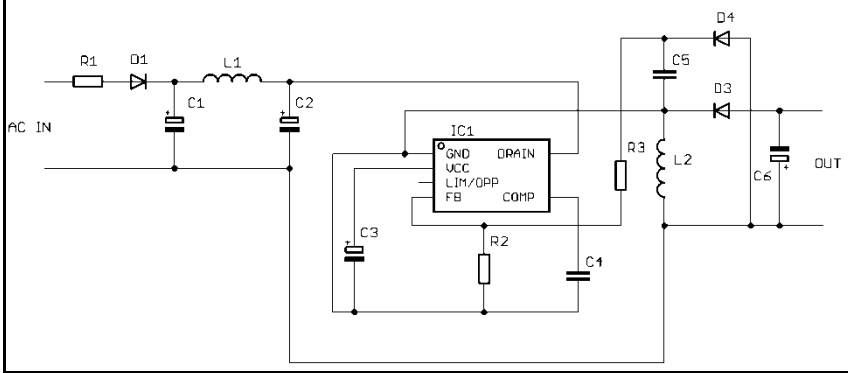
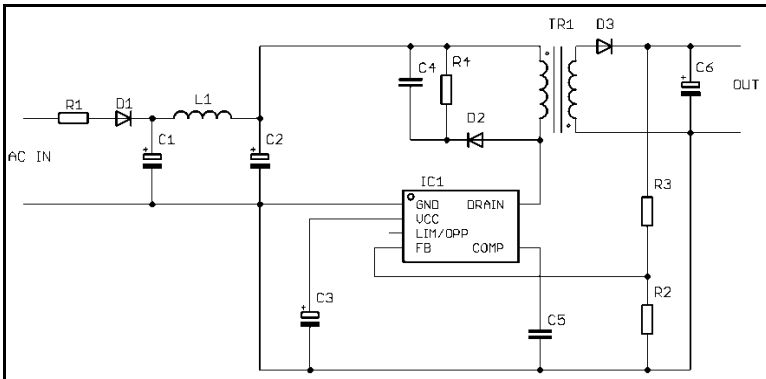
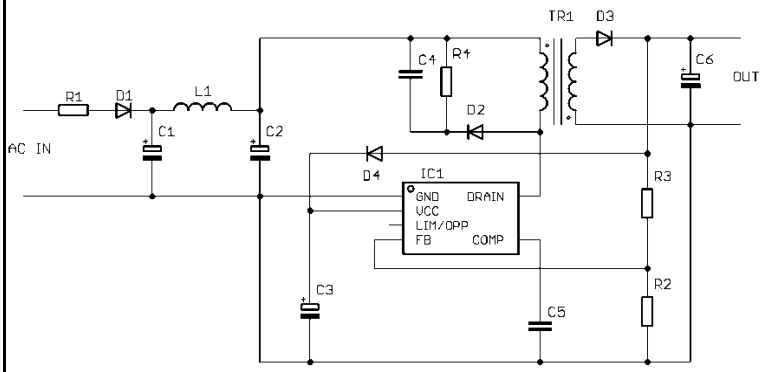
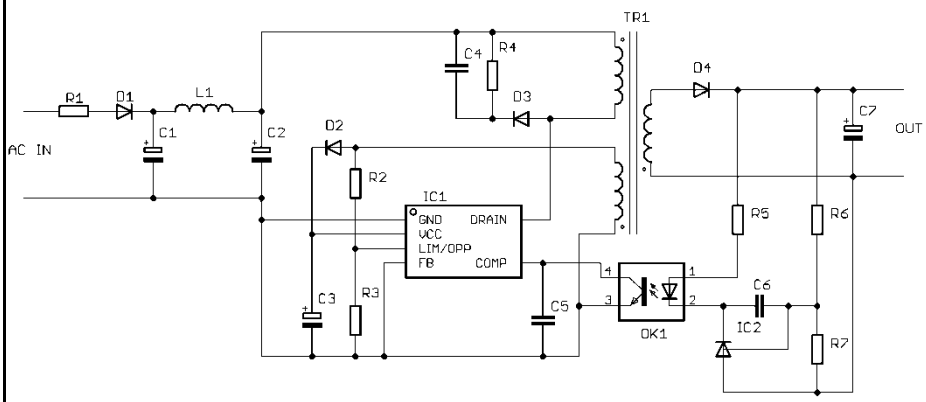
	• If the output voltage is above 9.0 V typ. (between Vcc(on) level and Vovp level) Vcc is supplied from output via D2 • If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS • R2 limits maximum output power (can be omitted if not required) • Direct feedback, resistive divider formed by R3, R4 sets output voltage
	• If the output voltage is above 9.0 V typ. (between Vcc(on) level and Vovp level) Vcc is supplied from output via D3 • If the output voltage is below 9.0 V, D3 and C5 are redundant, the IC is supplied from DSS • R2 limits maximum output power (can be omitted if not required) • Optocoupler feedback
Typical Non−isolated Application – Buck Converter	
	• If the output voltage is above 9.0 V typ. between $V_{CC(ON)}$ level and V_{OVP} level − VCC supplied from output via D2 • R2 limits maximal output power • Direct feedback, resistive divider formed by R3, R4 sets output voltage
	• VCC supplied from DSS • Output voltage is below 9.0 V typ. • LIM/OPP pin floating − no limit output power • Direct feedback, resistive divider formed by R2, R3 sets output voltage
Typical Non−isolated Application – Buck−Boost Converter	

Table 3. TYPICAL APPLICATIONS (continued)

	• VCC supplied from DSS • Output voltage is below 9.0 V typ. • LIM/OPP pin floating – no limit output power • Resistive divider formed by R2, R3 sets output voltage
	• If the output voltage is above 9.0 V typ. between $V_{CC(ON)}$ level and V_{OVP} level – VCC supplied from output via D4 • LIM/OPP pin floating – no limit output power • Resistive divider formed by R2, R3 sets output voltage
Typical Non−isolated Application – Flyback Converter	
	• VCC supplied from auxiliary winding • Resistive divider formed by R2, R3 sets output power limit and over power protection • Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage
Typical Isolated Application – Flyback Converter	

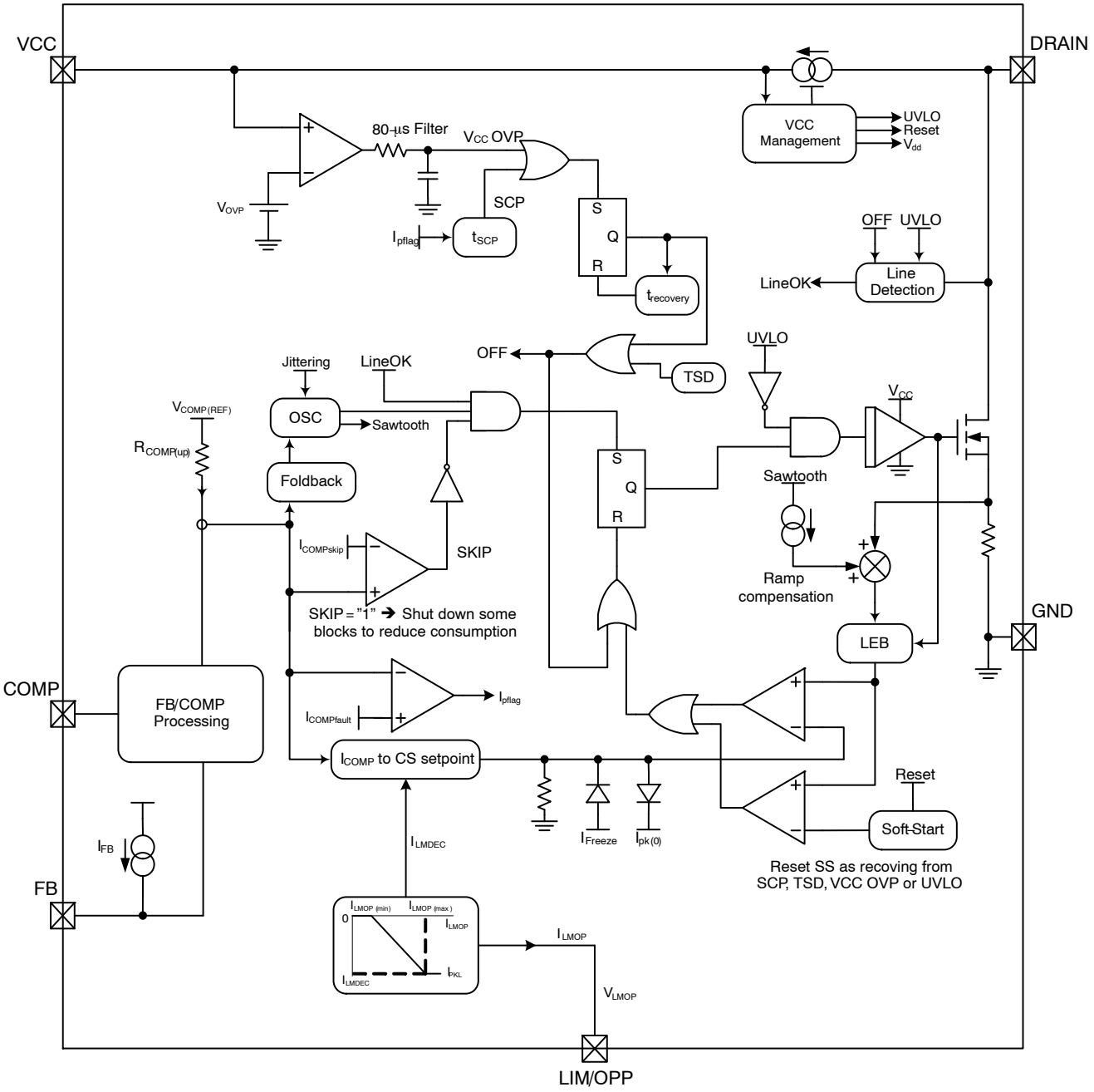


Figure 2. Simplified Internal Circuit Architecture

Table 4. MAXIMUM RATING TABLE (All voltages related to GND terminal)

Rating	Symbol	Value	Unit
Power supply voltage, V_{CC} pin, continuous voltage	V_{CC}	−0.3 to 20	V
Voltage on all pins, except Drain and V_{CC} pin	Vinmax	−0.3 to 10	V
Drain voltage	BVdss	−0.3 to 700	V
Maximum Current into V_{CC} pin	I_{CC}	10	mA
Drain Current Peak during Transformer Saturation (T_J = 150°C, Note 2): NCP1060 NCP1063 Drain Current Peak during Transformer Saturation (T_J = 125°C, Note 2): NCP1060 NCP1063 Drain Current Peak during Transformer Saturation (T_J = 25°C, Note 2): NCP1060 NCP1063	$I_{DS(PK)}$	 300 850 335 950 520 1500	mA
Thermal Resistance, Junction−to−Air − PDIP7 with 200 mm² of 35−μ copper area	$R_{\theta JA}$	115	°C/W
Thermal Resistance, Junction−to−Air − SOIC10 with 200 mm² of 35−μ copper area	$R_{\theta JA}$	132	°C/W
Thermal Resistance, Junction−to−Air − SOIC16 with 200 mm² of 35−μ copper area	$R_{\theta JA}$	104	°C/W
Junction−to−Top Thermal Characterization Parameter − PDIP7	Ψ_{JT}	7.3	°C/W
Junction−to−Top Thermal Characterization Parameter − SOIC10	Ψ_{JT}	2.3	°C/W
Junction−to−Top Thermal Characterization Parameter − SOIC16	Ψ_{JT}	2.5	°C/W
Junction Temperature Range	T_J	−40 to +150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Human Body Model ESD Capability (All pins except HV pin) per JEDEC JESD22−A114F	HBM	2	kV
Charged−Device Model ESD Capability per JEDEC JESD22−C101E	CDM	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. Maximum drain current $I_{DS(PK)}$ is obtained when the transformer saturates. It should not be mixed with short pulses that can be seen at turn on. Figure 3 below provides spike limits the device can tolerate.

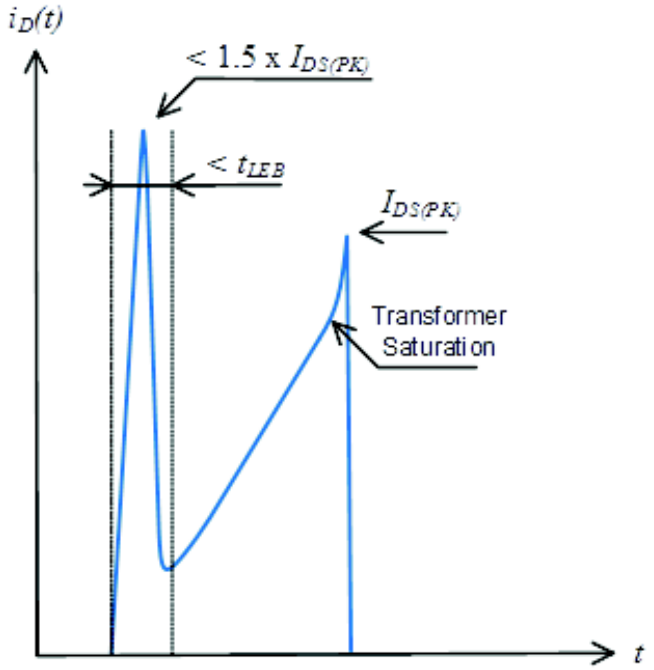


Figure 3. Spike Limits

Table 5. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
$V_{CC(on)}$	V_{CC} increasing level at which the switcher starts operation	2 (5)	8.4	9.0	9.5	V
$V_{CC(min)}$	V_{CC} decreasing level at which the HV current source restarts	2 (5)	7.0	7.5	7.8	V
$V_{CC(off)}$	V_{CC} decreasing level at which the switcher stops operation (UVLO)	2 (5)	6.7	7.0	7.2	V
I_{CC1}	Internal IC consumption, NCP1060 switching at 60 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1060 switching at 100 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1063 switching at 60 kHz, LIM/OPP = 0 A Internal IC consumption, NCP1063 switching at 100 kHz, LIM/OPP = 0 A	2 (5)	– – – –	0.92 0.97 0.99 1.07	– – – –	mA
I_{CCskip}	Internal IC consumption, COMP is 0 V (No switching on MOSFET)	2 (5)	–	340	–	μA
POWER SWITCH CIRCUIT						
$R_{DS(on)}$	Power Switch Circuit on−state resistance NCP1060 (Id = 50 mA) Tj = 25°C Tj = 125°C NCP1063 (Id = 50 mA) Tj = 25°C Tj = 125°C	7, 8 (6−10) (13−16)	 – – – –	 34 65 11.4 22	 41 72 14.0 24	Ω
BV_{DSS}	Power Switch Circuit & Startup breakdown voltage ($ID_{(off)}$ = 120 μA, Tj = 25°C)	7, 8 (6−10) (13−16)	700	–	–	V
$I_{DSS(off)}$	Power Switch & Startup breakdown voltage off−state leakage current Tj = 125°C (Vds = 700 V)	7, 8 (6−10) (13−16)	–	84	–	μA
t_r t_f	Switching characteristics (R_L = 50 Ω, V_{DS} set for I_{drain} = 0.7 x Ilim) Turn−on time (90% − 10%) Turn−off time (10% − 90%)	7, 8 (6−10) (13−16)	 – –	 20 10	 – –	ns
$t_{on(min)}$	Minimum on time NCP1060 NCP1063	7, 8 (6−10) (13−16)	 – –	 200 230	 – –	ns
INTERNAL START−UP CURRENT SOURCE						
I_{start1}	High−voltage current source, V_{CC} = $V_{CC(on)}$ − 200 mV	7, 8 (6−10) (13−16)	5	8	12	mA
I_{start2}	High−voltage current source, V_{CC} = 0 V	7, 8 (6−10) (13−16)	–	0.5	–	mA
V_{CCTH}	V_{CC} Transient level for I_{start1} to I_{start2} toggling point	2 (5)	–	1.4	–	V
$V_{start(min)}$	Minimum startup voltage, V_{CC} = 0 V	7, 8 (6−10) (13−16)			21	V
CURRENT COMPARATOR						
I_{IPK}	Maximum internal current setpoint at 50% duty cycle FB = 2 V, LIM/OPP = 0 μA, Tj = 25°C NCP1060 NCP1063	 – –	 – –	 250 650	 – –	mA
$I_{IPK(0)}$	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, LIM/OPP pin open Tj = 25°C NCP1060 NCP1063	 – –	 268 702	 300 780	 332 858	mA

3. The final switch current is: $I_{IPK(0)}$ / (V_{in}/L_P + S_a) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} = 60 kHz (Note 3), LIM/OPP pin open NCP1060 NCP1063	 – –	 – –	 330 740	 – –	mA
I_{IPKSW}	Final switch current with a primary slope of 200 mA/μs, F_{SW} = 100 kHz (Note 3), LIM/OPP pin open NCP1060 NCP1063	 – –	 – –	 320 710	 – –	mA
I_{LMDEC}	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, LIM/OPP = −285 μA, Tj = 25°C NCP1060 NCP1063	 – –	 – –	 128 312	 – –	mA
t_{SS}	Soft−start duration (guaranteed by design)	–	–	4	–	ms
t_{prop}	Propagation delay from current detection to drain OFF state	–	–	70	–	ns
t_{LEB}	Leading Edge Blanking Duration NCP1060 NCP1063	 – –	 – –	 130 160	 – –	ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency, 60 kHz version, Tj = 25°C (Note 4)	–	54	60	66	kHz
f_{OSC}	Oscillation frequency, 100 kHz version, Tj = 25°C (Note 4)	–	90	100	110	kHz
f_{jitter}	Frequency jittering in percentage of f_{OSC}	–	–	±6	–	%
f_{swing}	Jittering swing frequency	–	–	300	–	Hz
D_{max}	Maximum duty−cycle	–	62	66	72	%
ERROR AMPLIFIER SECTION						
V_{REF}	Voltage Feedback Input (V_{COMP} = 2.5 V)	4 (7)	3.2	3.3	3.4	V
I_{FB}	Input Bias Current (V_{FB} = 3.3 V)	4 (7)	–	1	–	μA
G_M	Transconductance	5 (8)		2		mS
I_{OTAlim}	OTA maximum current capability (V_{FB} > V_{OTAen})	5 (8)		±150		μA
V_{OTAen}	FB voltage to disable OTA	4 (7)	0.7	1.3	1.7	V
COMPENSATION SECTION						
$I_{COMPfault}$	COMP current for which Fault is detected	5 (8)	–	−40	–	μA
$I_{COMP100\%}$	COMP current for which internal current set−point is 100% ($I_{IPK(0)}$)	5 (8)	–	−44	–	μA
$I_{COMPfreeze}$	COMP current for which internal current setpoint is: $I_{Freeze1\ or\ 2}$ (NCP1060/3)	5 (8)	–	−80	–	μA
$V_{COMP(REF)}$	Equivalent pull−up voltage in linear regulation range (Guaranteed by design)	5 (8)	–	2.7	–	V
$R_{COMP(up)}$	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	5 (8)	–	17.7	–	kΩ
V_{LMOP}	Voltage on LIM/OPP pin @ I_{LMOP} = −35 μA Voltage on LIM/OPP pin @ I_{LMOP} = −250 μA, Tj = 25°C	3 (6)	1.40 1.28	1.50 1.35	1.60 1.42	V
I_{LMOP}	Maximum current from LIM/OPP pin	3 (6)		−330	−420	μA
$I_{LMOP(min)}$	Current at which LIM/OPP starts to decrease I_{PEAK}	3 (6)	−20	−26	−32	μA
$I_{LMOP(max)}$	Current at which LIM/OPP stops to decrease I_{PEAK}	3 (6)		−285		μA
$I_{LMOP(neg)}$	Negative Active Clamp Voltage (I_{LMOP} = −2.5 mA)	3 (6)		−0.7		V

3. The final switch current is: $I_{IPK(0)}$ / ($V_{in}/L_P + S_a$) x V_{in}/L_P + V_{in}/L_P x t_{prop}, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
COMPENSATION SECTION						
$I_{LMOP(pos)}$	Positive Active Clamp (Guaranteed by design)	3 (6)		2.5		mA
FREQUENCY FOLDBACK & SKIP						
$I_{COMPfold}$	Start of frequency foldback COMP pin current level	5 (8)	–	−68	–	μA
$I_{COMPfold(end)}$	End of frequency foldback COMP pin current level, $f_{sw} = f_{min}$	5 (8)	–	−100	–	μA
f_{min}	The frequency below which skip−cycle occurs	–	21	25	29	kHz
$I_{COMPskip}$	The COMP pin current level to enter skip mode	5 (8)	–	−120	–	μA
$I_{Freeze1}$	Internal minimum current setpoint ($I_{COMP} = I_{COMPFreeze}$) in NCP1060		–	110	–	mA
$I_{Freeze2}$	Internal minimum current setpoint ($I_{COMP} = I_{COMPFreeze}$) in NCP1063		–	270	–	mA
RAMP COMPENSATION						
$S_{a(60)}$	The internal ramp compensation @ 60 kHz: NCP1060 NCP1063	 – –	 – –	 8.4 15.6	 – –	mA/μs
$S_{a(100)}$	The internal ramp compensation @ 100 kHz: NCP1060 NCP1063	 – –	 – –	 14 26	 – –	mA/μs
PROTECTIONS						
t_{SCP}	Fault validation further to error flag assertion	–	35	48	–	ms
$t_{recovery}$	OFF phase in fault mode	–	–	400	–	ms
V_{OVP}	V_{CC} voltage at which the switcher stops pulsing	2 (5)	17.0	18.0	18.8	V
t_{OVP}	The filter of V_{CC} OVP comparator	–	–	80	–	μs
$V_{HV(EN)}$	The drain pin voltage above which allows MOSFET operate, which is detected after TSD, UVLO, SCP, or V_{CC} OVP mode. (A version only)	7,8 (6−10) (13−16)	67	87	110	V
TEMPERATURE MANAGEMENT						
TSD	Temperature shutdown (Guaranteed by design)	–	150	163	–	°C
TSD_{hyst}	Hysteresis in shutdown (Guaranteed by design)	–	–	20	–	°C

3. The final switch current is: $I_{IPK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$, with S_a the built−in slope compensation, Vin the input voltage, L_P the primary inductor in a flyback, and t_{prop} the propagation delay.
4. Oscillator frequency is measured with disabled jittering.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

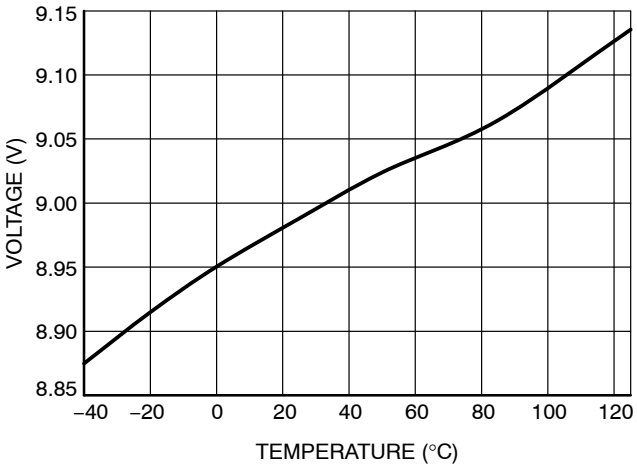


Figure 4. $V_{CC(on)}$ vs. Temperature

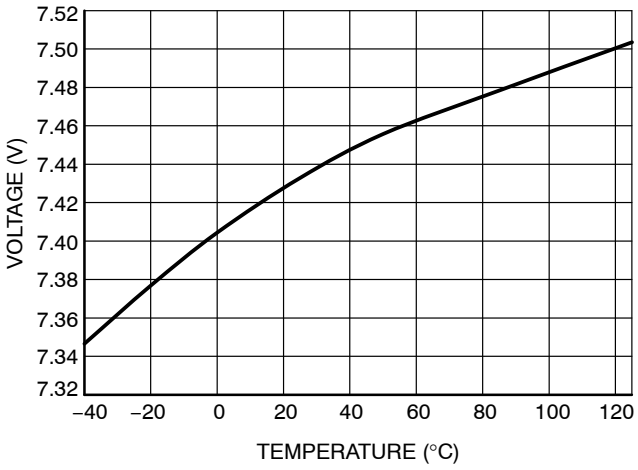


Figure 5. $V_{CC(min)}$ vs. Temperature

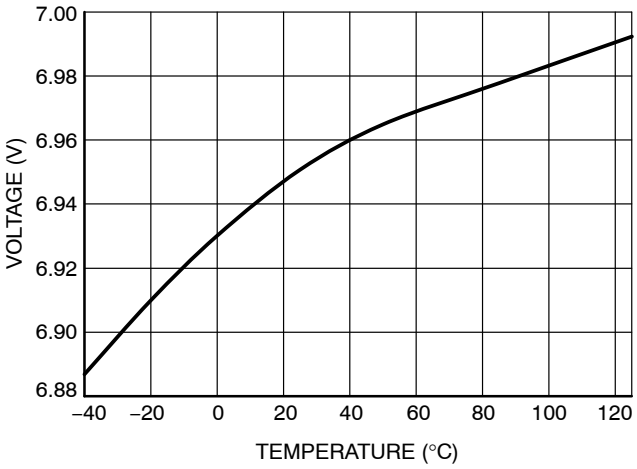


Figure 6. $V_{CC(off)}$ vs. Temperature

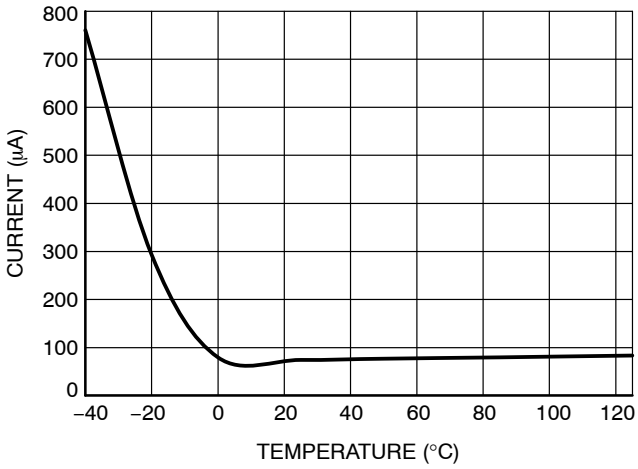


Figure 7. $I_{DSS(off)}$ vs. Temperature

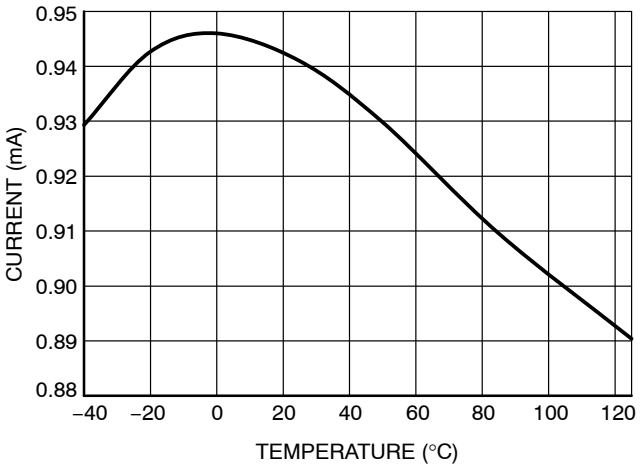


Figure 8. $I_{CC1\ 60\ kHz}$ vs. Temperature

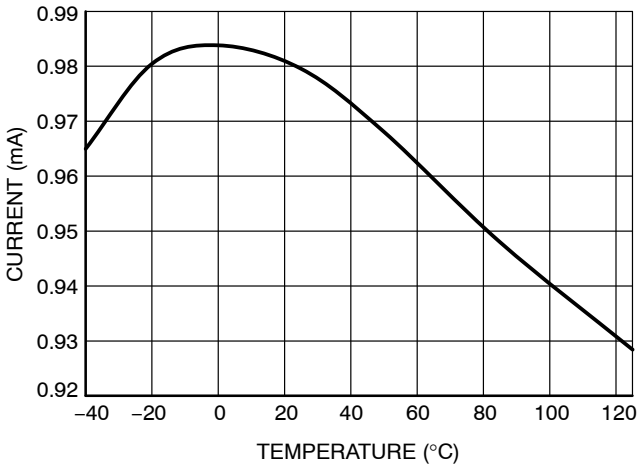


Figure 9. $I_{CC1\ 100\ kHz}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

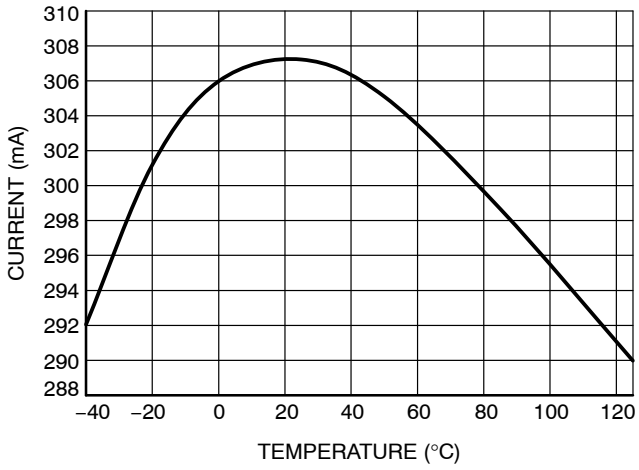


Figure 10. $I_{IPK(0)1060}$ vs. Temperature

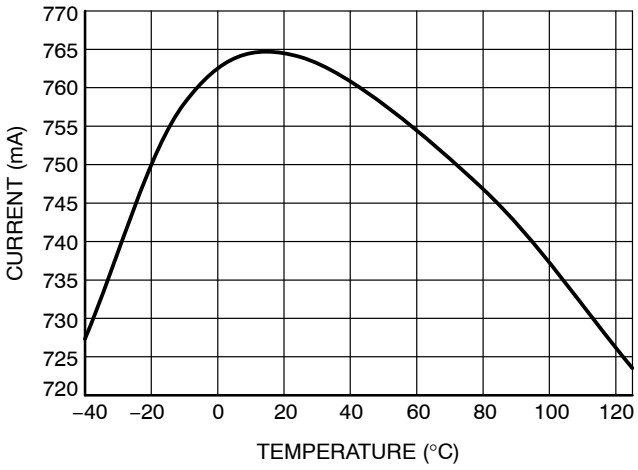


Figure 11. $I_{IPK(0)1063}$ vs. Temperature

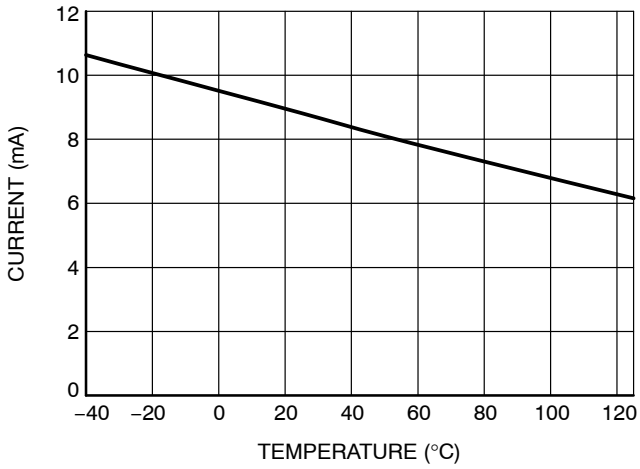


Figure 12. I_{start1} vs. Temperature

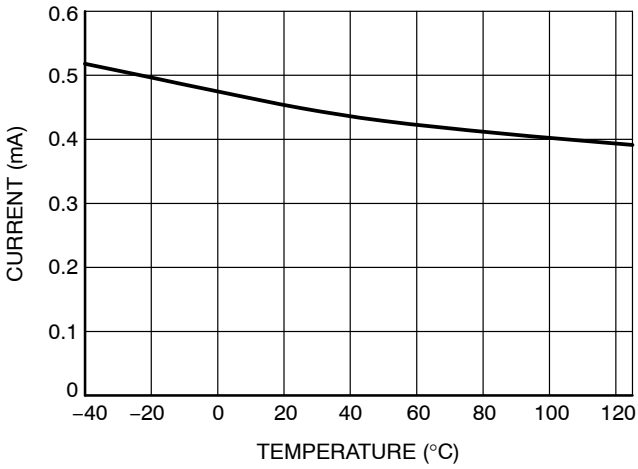


Figure 13. I_{start2} vs. Temperature

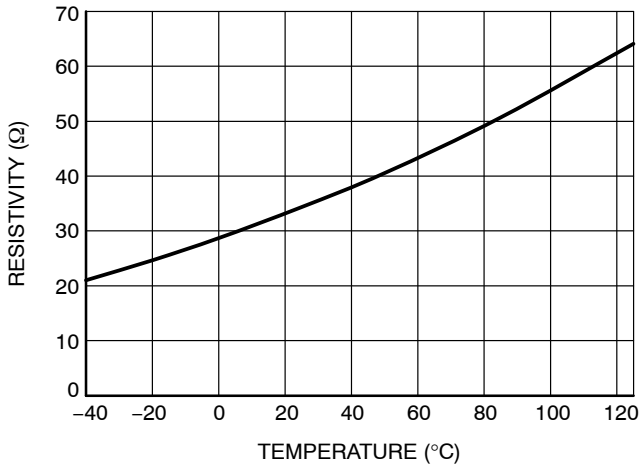


Figure 14. $R_{DS(on)1060}$ vs. Temperature

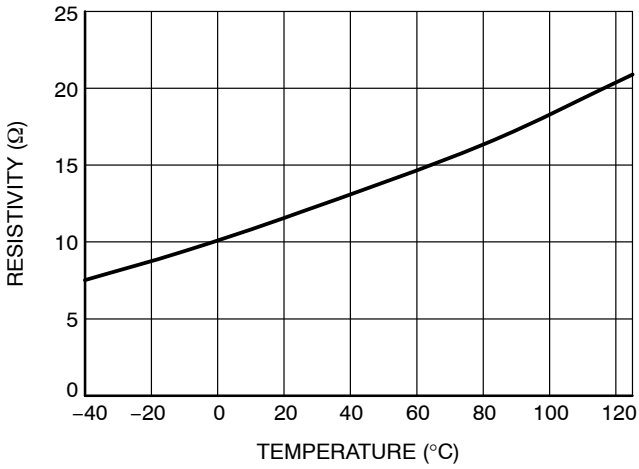


Figure 15. $R_{DS(on)1063}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

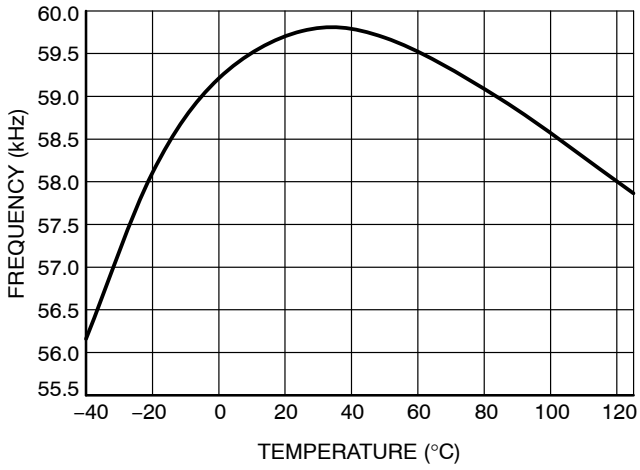


Figure 16. f_{OSC60} vs. Temperature

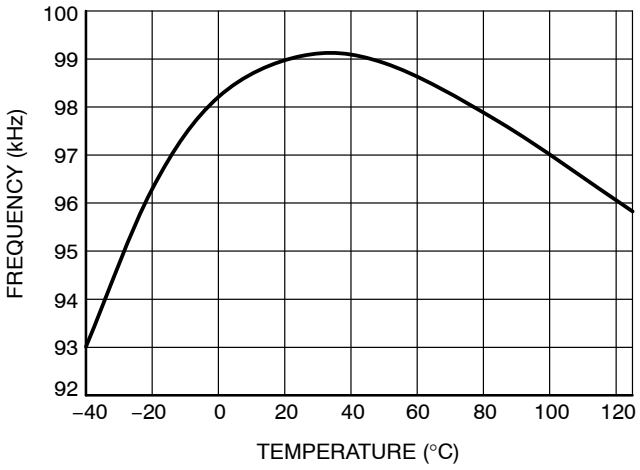


Figure 17. f_{OSC100} vs. Temperature

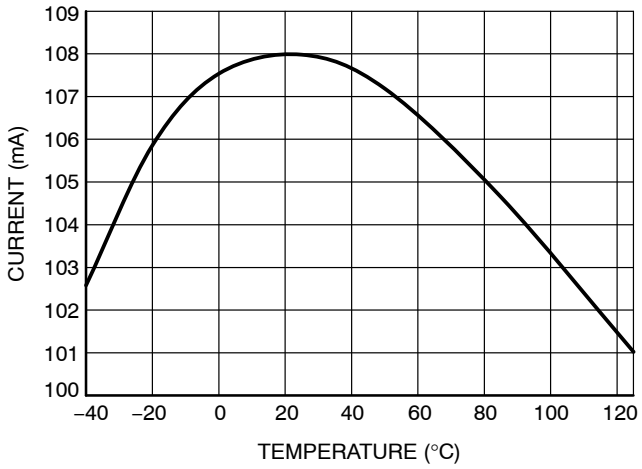


Figure 18. $I_{freeze1060}$ vs. Temperature

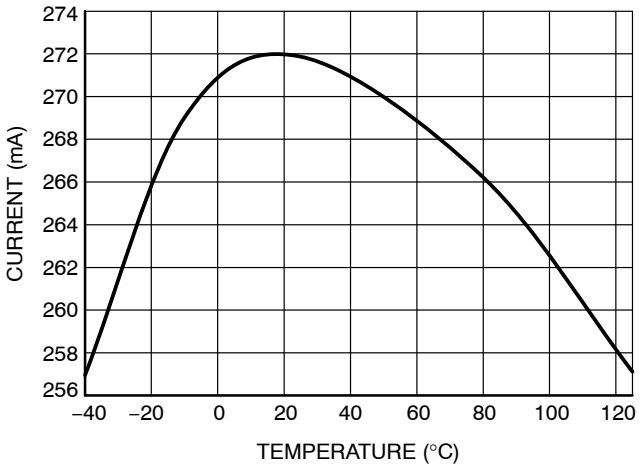


Figure 19. $I_{freeze1063}$ vs. Temperature

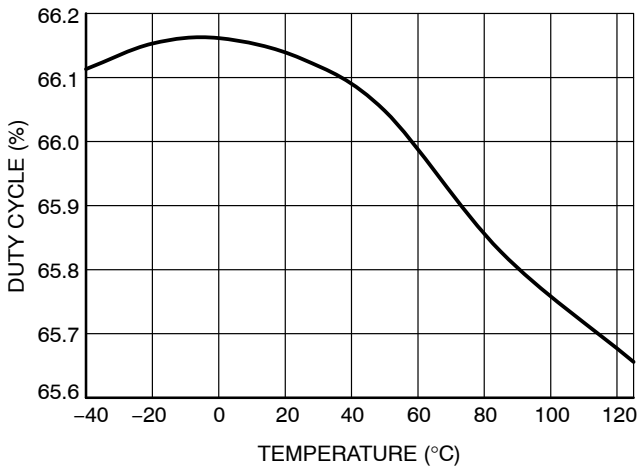


Figure 20. $D_{(max)}$ vs. Temperature

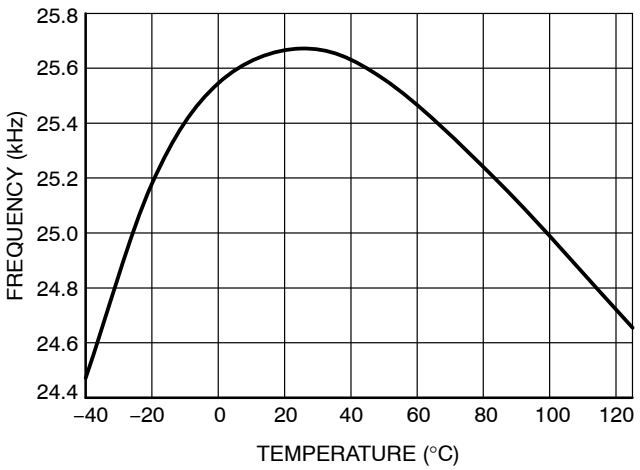


Figure 21. f_{min} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

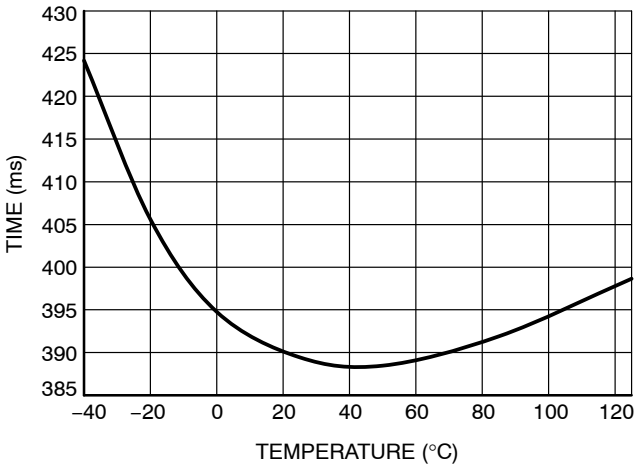


Figure 22. $t_{recovery}$ vs. Temperature

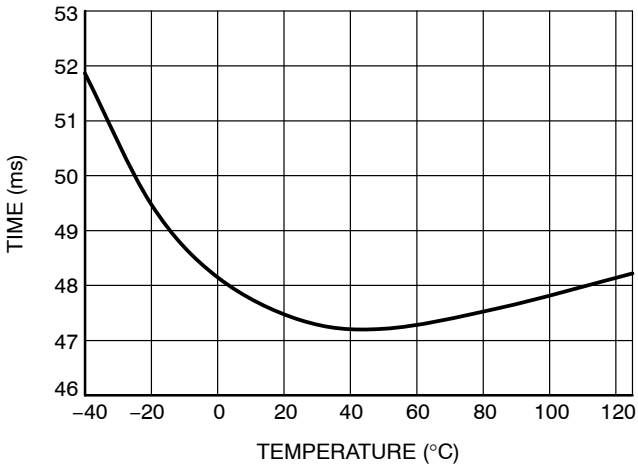


Figure 23. t_{SCP} vs. Temperature

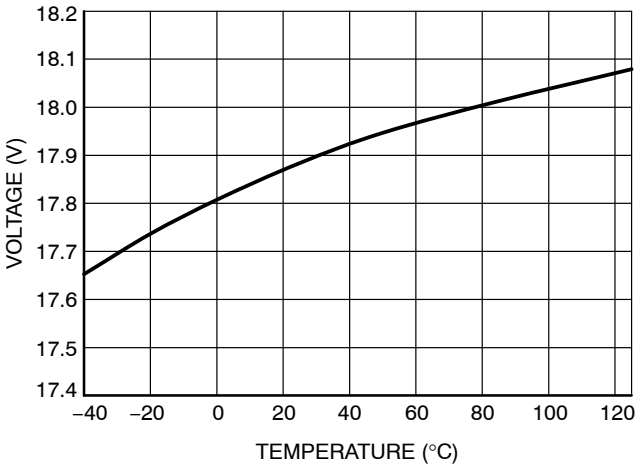


Figure 24. V_{OVP} vs. Temperature

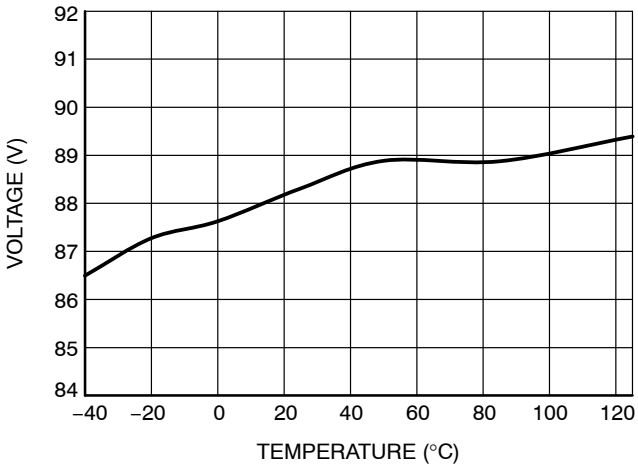


Figure 25. $V_{HV(EN)}$ vs. Temperature

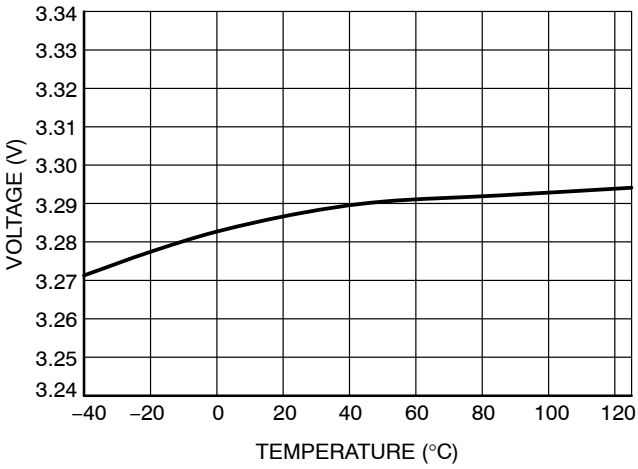


Figure 26. V_{REF} vs. Temperature

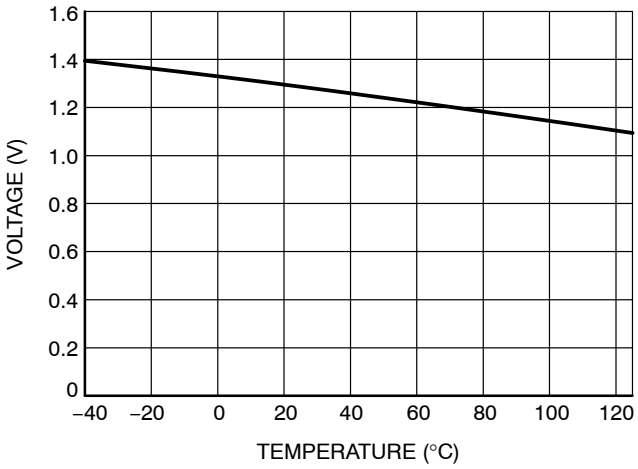


Figure 27. V_{OTAen} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

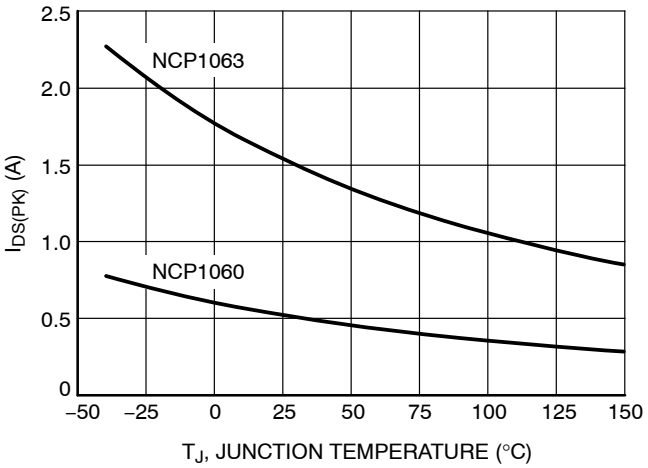


Figure 28. Drain Current Peak during Transformer Saturation vs. Junction Temperature

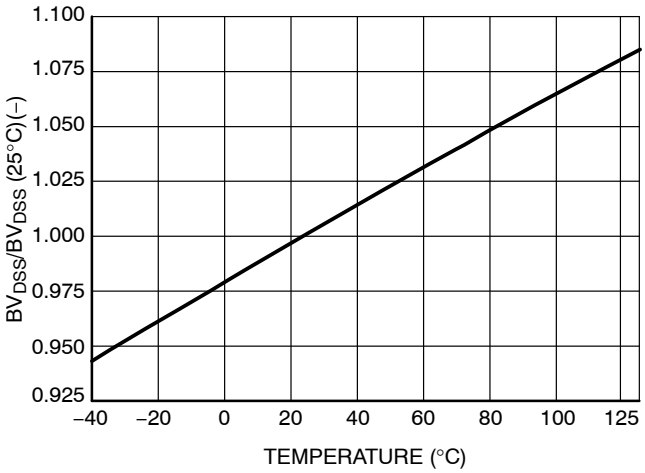


Figure 29. Breakdown Voltage vs. Temperature

APPLICATION INFORMATION

Introduction

The NCP106X offers a complete current−mode control solution. The component integrates everything needed to build a rugged and cost effective Switch−Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table, Table 6, details the differences between references, mainly peak current setpoints, $R_{DS(on)}$ value and operating frequency.

- **Current−mode Operation:** the controller uses current−mode control architecture.
- **700 V −_ Power MOSFET:** Due to **onsemi** Very High Voltage Integrated Circuit technology, the circuit hosts a high−voltage power MOSFET featuring a 34 Ω or 11.4 Ω $R_{DS(on)}$ − Tj = 25°C. This value lets the designer build a power supply up to 7.8 W or 15.5 W operated on universal mains. An internal current source delivers the startup current, necessary to crank the power supply.
- **Dynamic Self−supply:** Due to the internal high voltage current source, this device could be used in the application without the auxiliary winding to provide supply voltage.
- **Short Circuit Protection:** by permanently monitoring the COMP line activity, the IC is able to detect the presence of a short−circuit, immediately reducing the output power for a total system protection. A t_{SCP} timer is started as soon as the COMP current is below threshold, $I_{COMPfault}$, which indicates the maximum peak current. If at the end of this timer the fault is still present, then the device enters a safe, auto−recovery burst mode, affected by a fixed timer recurrence, $t_{recovery}$. Once the short has disappeared, the controller resumes and goes back to normal operation.
- **Built−in VCC Over Voltage Protection:** when the auxiliary winding is used to bias the V_{CC} pin (no DSS), an internal comparator is connected to V_{CC} pin. In case the voltage on the pin exceeds a level of V_{OVP} (18 V typically), the controller immediately stops switching and waits a full timer period ($t_{recovery}$) before attempting to restart. If the fault is gone, the controller resumes operation. If the fault is still there, e.g. a broken opto−coupler, the controller protects the load through a safe burst mode.
- **Line Detection:** An internal comparator monitors the drain voltage as recovering from one of the following situations:
  - Short Circuit Protection,
  - V_{CC} OVP is confirmed,
  - UVLO,
  - TSD
- If the drain voltage is lower than the internal threshold ($V_{HV(EN)}$), the internal power switch is inhibited. This avoids operating at too low ac input. This is also called brown−in function in some fields. For applications not using standard AC mains (24 Vdc industrial bus for instance), the B version doesn't incorporate this line detection and let the device start as soon as voltage supply reaches $V_{start(min)}$.
- **Frequency Jittering:** an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering remains active in frequency foldback mode.
- **Soft−start:** a 4 ms soft−start ensures a smooth startup sequence, reducing output overshoots.
- **Frequency Foldback Capability:** a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the COMP pin current information and when it reaches a level of $I_{COMPfold}$, the oscillator then starts to reduce its switching frequency as the feedback current continues to increase (the power demand continues to reduce). It can go down to 25 kHz (typical) reached for a feedback level of $I_{COMPfold(end)}$ (100 μA roughly). At this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- **Skip:** if SMPS naturally exhibits a good efficiency at nominal load, it begins to be less efficient when the output power demand diminishes. By skipping un−needed switching cycles, the NCP106X drastically reduces the power wasted during light load conditions.
- **Ipeak Set:** If current in range 26 μA and 285 μA is drawn from the pin, the peak current is proportionally reduced down to 40% of its original value. This feature enables to designer to set up the peak current to the value which is ideal for the application.

By routing a portion of the negative voltage present during the on−time on the auxiliary winding to the LIM/OPP pin, the user has a simple and non−dissipative means to alter the maximum peak current setpoint as the bulk voltage increases.

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 8.0 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level (typically 9.0 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET if the bulk voltage is above $V_{HV(EN)}$ level (87 V typically) for A version and if bulk voltage is above $V_{start(min)}$ (21 V dc) for B version. There is no disable level for drain pin voltage, the device will stop switching when the input voltage is removed and sub−sequentially the V_{CC} reaches the $V_{CC(OFF)}$ level, or t_{SCP} timer elapses. Figure 30 details the simplified internal circuitry.

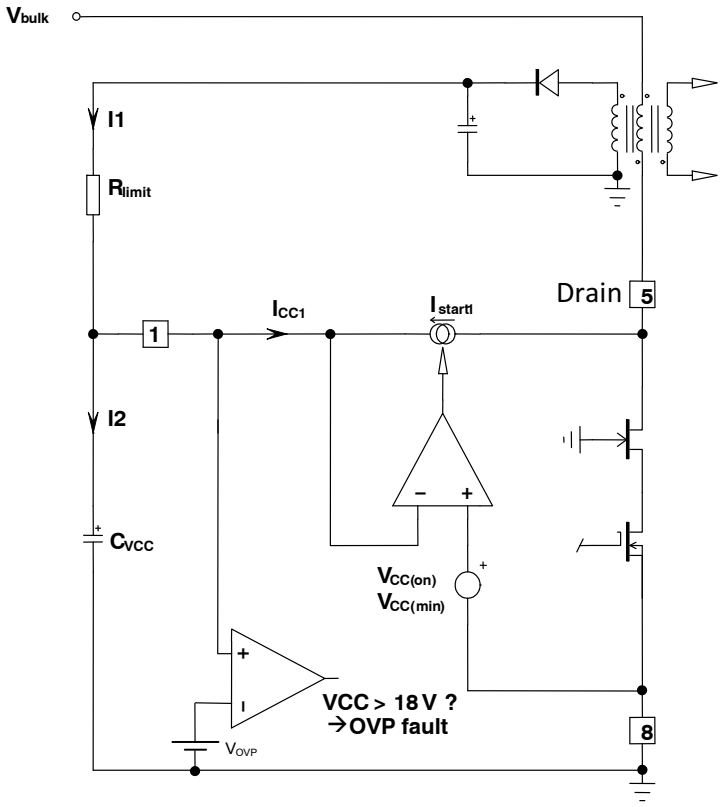


Figure 30. The Internal Arrangement of the Start−up Circuitry

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When V_{CC} is below $V_{CC(min)}$ level (7.5 V typically), it activates the internal current source to bring V_{CC} toward $V_{CC(on)}$ level and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.5 V ripple takes place on the V_{CC} pin whose average value equals ($V_{CC(on)}$ + $V_{CC(min)}$)/2. Figure 31 portrays a typical operation of the DSS.

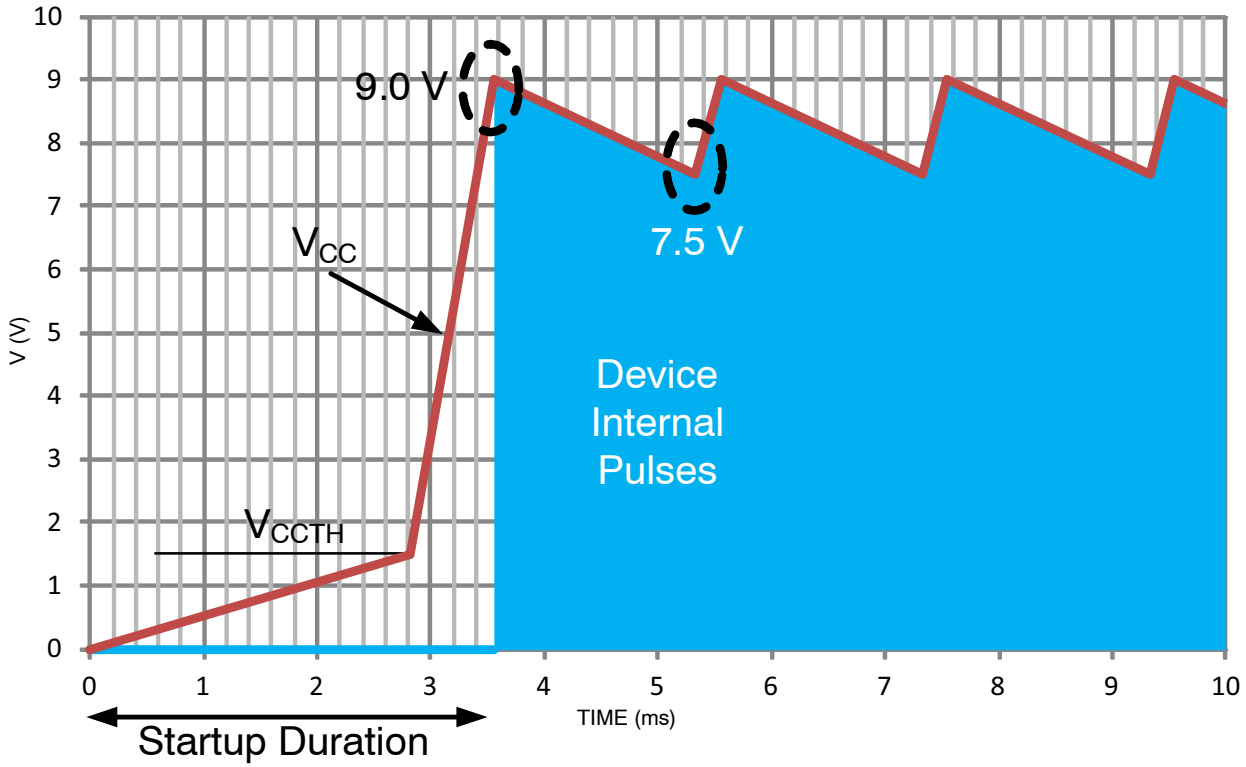


Figure 31. The Charge/Discharge Cycle over a 1 μF V_{CC} Capacitor

As one can see, even if there is auxiliary winding to provide energy for V_{CC}, it happens that the device is still biased by DSS during start−up time or some fault mode when the voltage on auxiliary winding is not ready yet. The V_{CC} capacitor shall be dimensioned to avoid V_{CC} crosses $V_{CC(off)}$ level, which stops operation. The ΔV between $V_{CC(min)}$ and $V_{CC(off)}$ is 0.5 V. There is no current source to charge V_{CC} capacitor when driver is on, i.e. drain voltage is close to zero. Hence the V_{CC} capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} \cdot D_{max}}{f_{OSC} \cdot \Delta V} \qquad \text{(eq. 1)}$$

Take the 60 kHz device as an example. C_{VCC} should be above

$$\frac{0.8\ m \cdot 72\%}{54\ kHz \cdot 0.5} = 21\ nF.$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1 μF is appropriate.

The V_{CC} capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 30, an internal OVP comparator, protects the switcher against lethal V_{CC} runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the over voltage protection (OVP) circuit and immediately stops the output pulses for $t_{recovery}$ duration (400 ms typically). Then a new start−up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

Fault Condition − Short−circuit on V_{CC}

In some fault situations, a short−circuit can purposely occur between V_{CC} and GND. In high line conditions (V_{HV} = 370 V_{DC}) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I_{start1} equals 5 mA (the min corresponds to the highest T_j), the device would dissipate 370 x 5 m = 1.85 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I_{start1} and I_{start2}. At power−up, as long as V_{CC} is below a 1.4 V level, the source delivers I_{start2} (around 500 μA typical), then, when V_{CC} reaches 1.4 V, the source smoothly transitions to I_{start1} and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 x 500 μ = 185 mW. Figure 31 portrays this particular behavior.

The first startup period is calculated by the formula C x V = I x t, which implies a 1 μ x 1.4 / 500 μ = 2.8 ms startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of $V_{CC(on)}$ − V_{CCTH} = 9.0 − 1.4 = 7.6 V, which finally leads to a second startup time of 1 μ x 7.6 / 8 m = 0.95 ms. The total startup time becomes 2.8 m + 0.95 m = 3.75 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

Fault Condition – Output Short−circuit

As soon as V_{CC} reaches $V_{CC(on)}$, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the V_{CC} pin as the output voltage rises. During the start−sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I_{IPK}, which is reached after a typical period of 4 ms. When the output voltage is not regulated, the current coming through COMP pin is below $I_{COMPfault}$ level (40 μA typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter t_{SCP} (48 ms typically). If at counter completion, I_{pflag} remains asserted, all driving pulses are stopped and the part stays off in $t_{recovery}$ duration (about 400 ms). A new attempt to re−start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty−cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 32 depicts this particular mode:

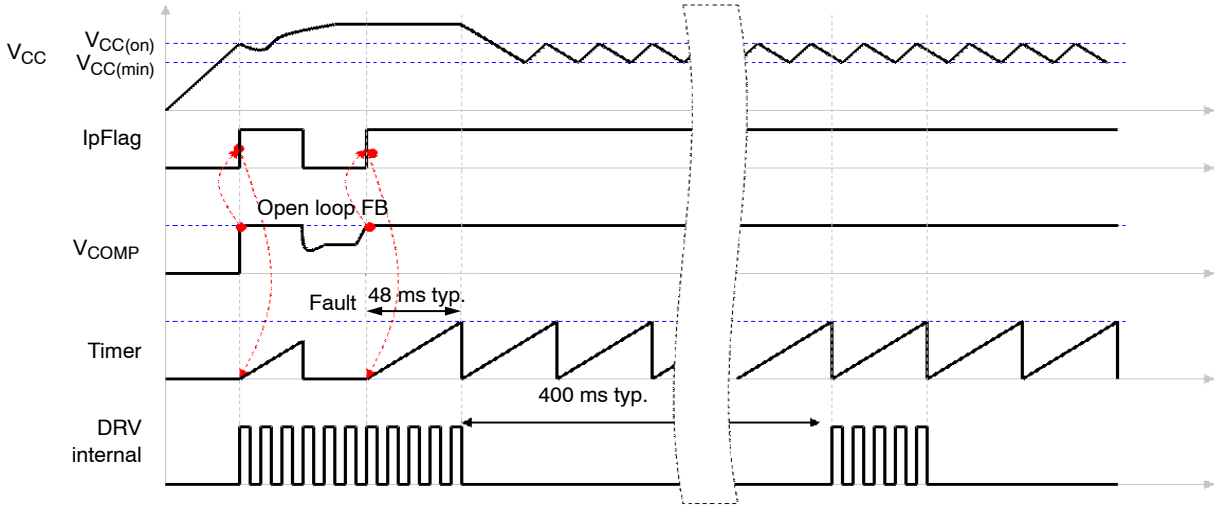


Figure 32. In Case of Short−circuit or Overload, the NCP106X Protects Itself and the Power Supply via a Low Frequency Burst Mode. The V_{CC} is Maintained by the Current Source and Self−supplies the Controller

Auto−recovery Over Voltage Protection

The particular NCP106X arrangement offers a simple way to prevent output voltage runaway when the optocoupler fails. As Figure 33 shows, a comparator monitors the V_{CC} pin. If the auxiliary pushes too much voltage into the C_{VCC} capacitor, then the controller considers an OVP situation and stops the internal drivers. When an OVP occurs, all switching pulses are permanently disabled. After $t_{recovery}$ delay, it resumes the internal drivers. If the failure symptom still exists, e.g. feedback opto−coupler fails, the device keeps the auto−recovery OVP mode. It is recommended insertion of a resistor (R_{limit}) between the auxiliary dc level and the V_{CC} pin to protect the IC against high voltage spikes, which can damage the IC, and to filter out the Vcc line to avoid undesired OVP activation. R_{limit} should be carefully selected to avoid triggering the OVP as we discussed, but also to avoid disturbing the V_{CC} in low / light load conditions.

Self−supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency re−fueling rate of the V_{CC} capacitor is not enough to keep a proper auxiliary voltage.

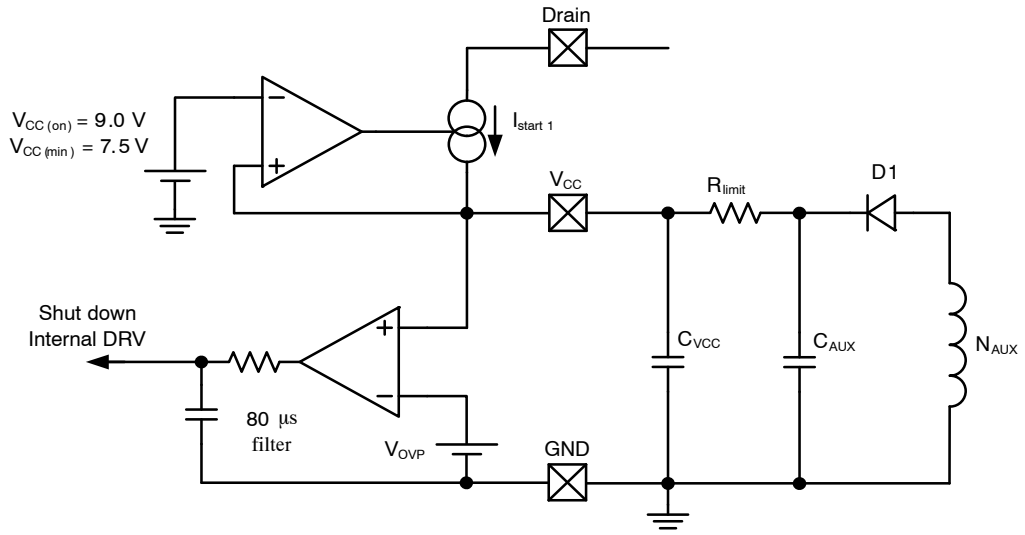


Figure 33. A More Detailed View of the NCP106X Offers Better Insight on how to Properly Wire an Auxiliary Winding

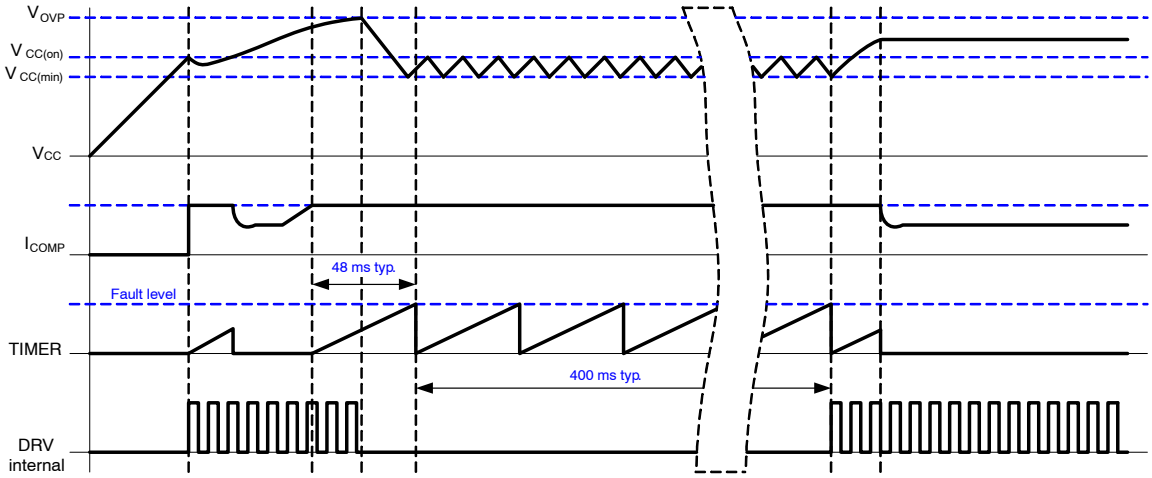


Figure 34. Describes the Main Signal Variations when the Part Operates in Auto−recovery OVP

Soft−start

The NCP106X features a 4 ms soft−start which reduces the power−on stress but also contributes to lower the output overshoot. Figure 35 shows a typical operating waveform. The NCP106X features a novel patented structure which offers a better soft−start ramp, almost ignoring the start−up pedestal inherent to traditional current−mode supplies.

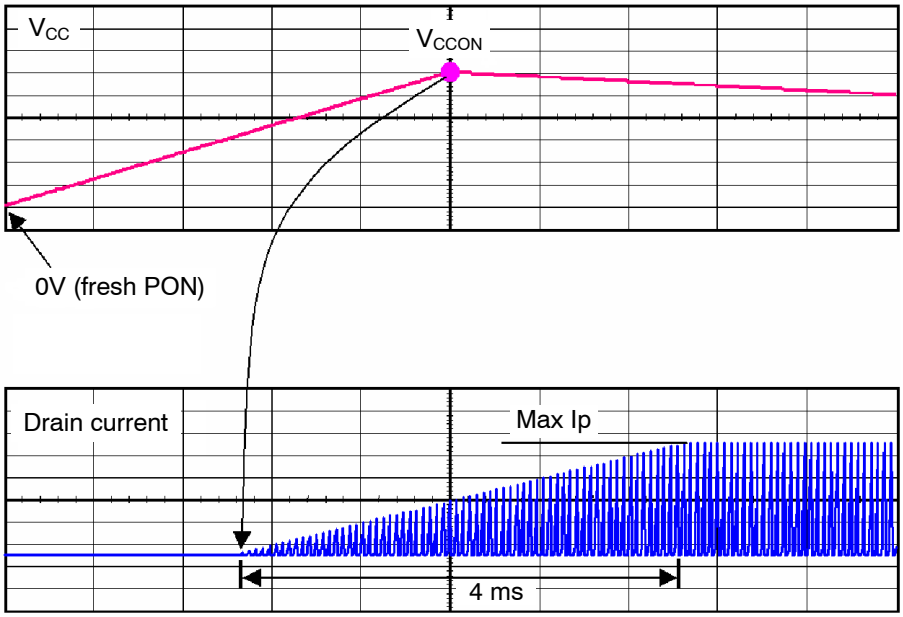


Figure 35. The 4 ms Soft−start Sequence

Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP106X offers a ±6% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 36 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

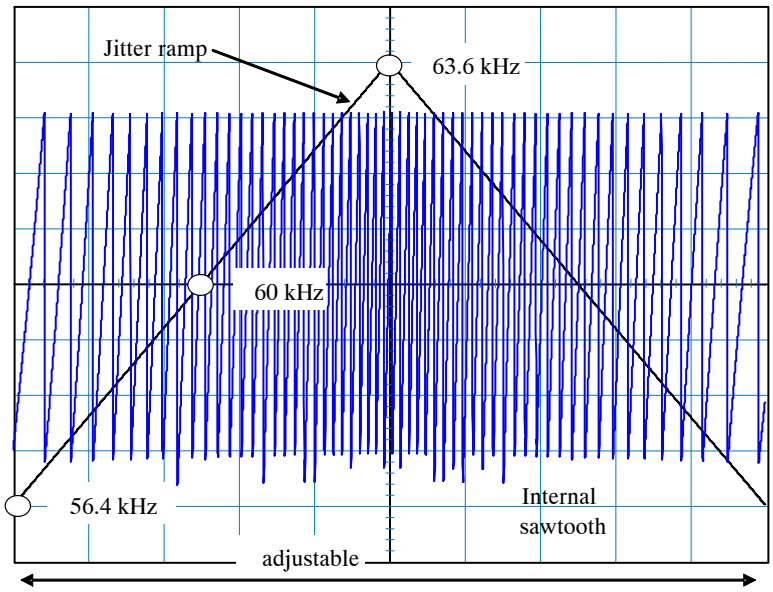


Figure 36. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Line Detection (for A version only)

An internal comparator monitors the drain voltage as recovering from one of the following situations:

- Short Circuit Protection,
- V_{CC} OVP is confirmed,
- UVLO
- TSD

If the drain voltage is lower than the internal threshold $V_{HV(EN)}$ (87 Vdc typically), the internal power switch is inhibited. This avoids operating at too low ac input.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires to change the traditional fixed−frequency type of operation. This device implements a switching frequency foldback when the COMP current passes above a certain level, $I_{COMPfold}$, set around 68 μA. At this point, the oscillator enters frequency foldback and reduces its switching frequency.

The internal peak current set−point is following the COMP current information until its level reaches I_{Freeze}. Below this value, the peak current setpoint is frozen to 30% of the $I_{PK(0)}$. The only way to further reduce the transmitted power is to diminish the operating frequency down to F_{min} (25 kHz typically). This value is reached at a COMP current level of $I_{COMPfold(end)}$ (100 μA typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figure 37 and Figure 38 depict the adopted scheme for the part.

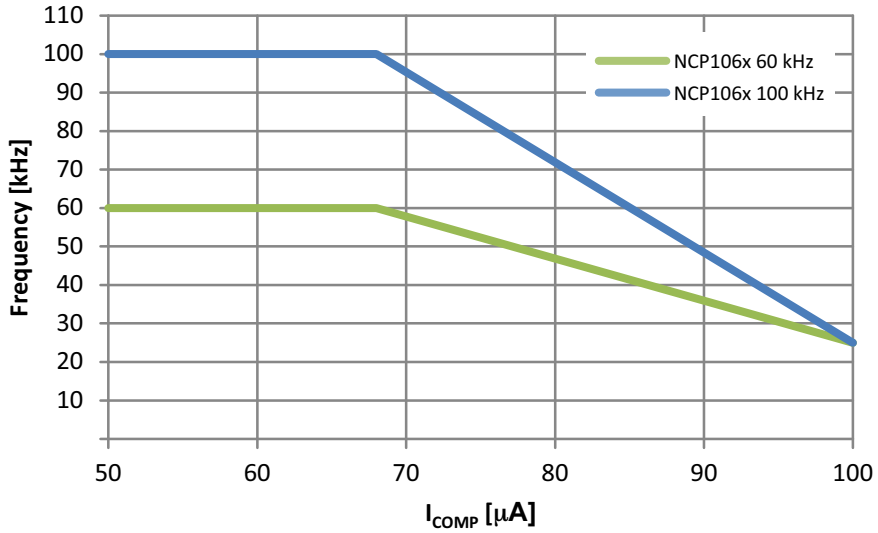


Figure 37. By Observing the Current on the COMP Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

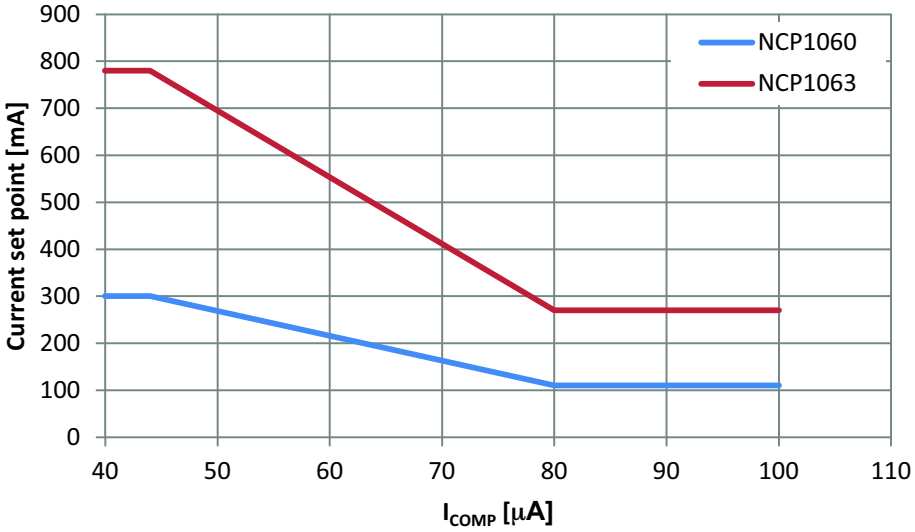


Figure 38. Ipk Set−point is Frozen at Lower Power Demand

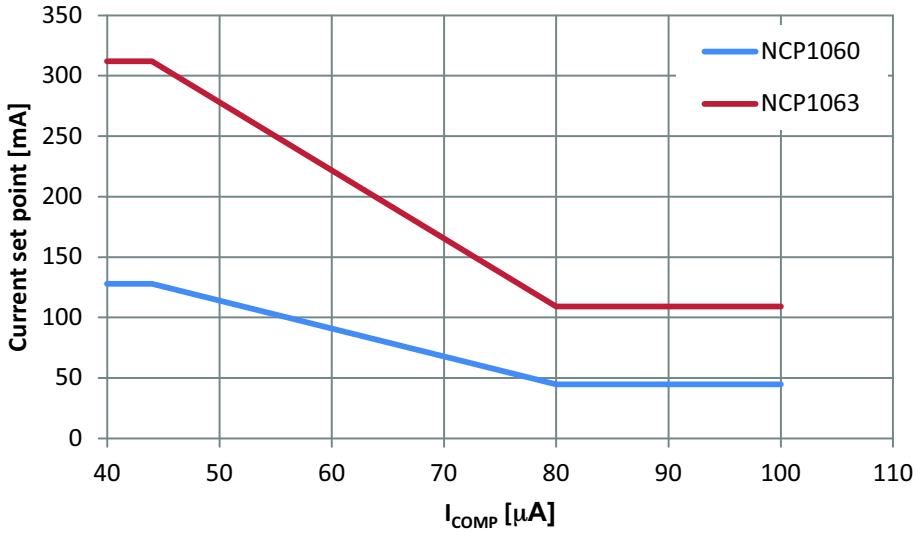


Figure 39. Ipk Set−point is Frozen at Lower Power Demand (I_{LMOP} ≥ 285 μA)

Feedback and Skip

Figure 40 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current (I_{COMP}) is above 40 μA. In this linear operating range, the dynamic resistance is 17.7 kΩ typically ($R_{COMP(up)}$) and the effective pull up voltage is 2.7 V typically ($V_{COMP(REF)}$). When I_{COMP} is decreases, the COMP voltage will increase to 3.2 V.

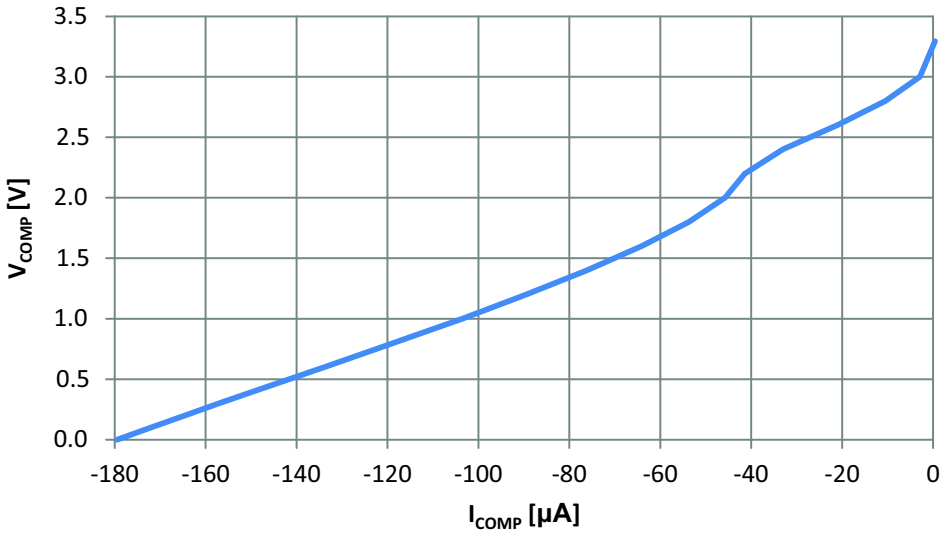


Figure 40. COMP Pin Voltage vs. Current

Figure 41 depicts the skip mode block diagram. When the COMP current information reaches $I_{COMPskip}$, the internal clock setting the flip−flop is blanked and the internal consumption of the controller is decreased. The hysteresis of internal skip comparator is minimized to lower the ripple of the auxiliary voltage for V_{CC} pin and V_{OUT} of power supply during skip mode. It easies the design of V_{CC} over load range.

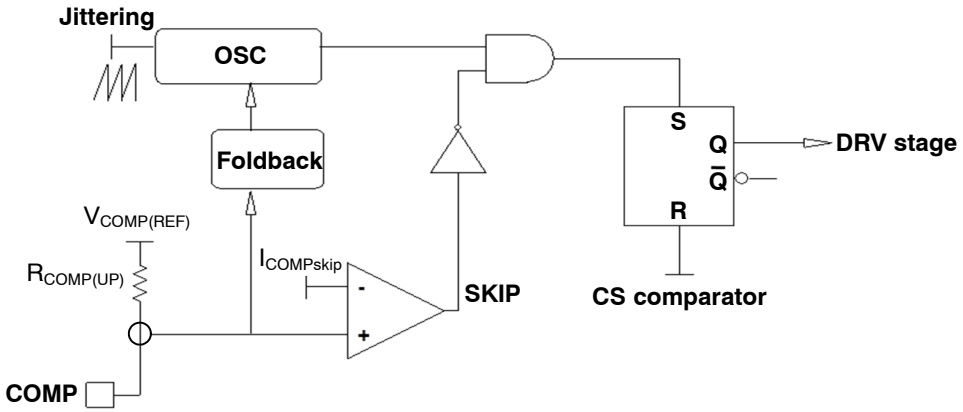


Figure 41. Skip Cycle Schematic

Ilimit and OPP Function

The function makes the integrated circuit more flexible. The current drawn out of LIM/OPP pin defines the current set point.

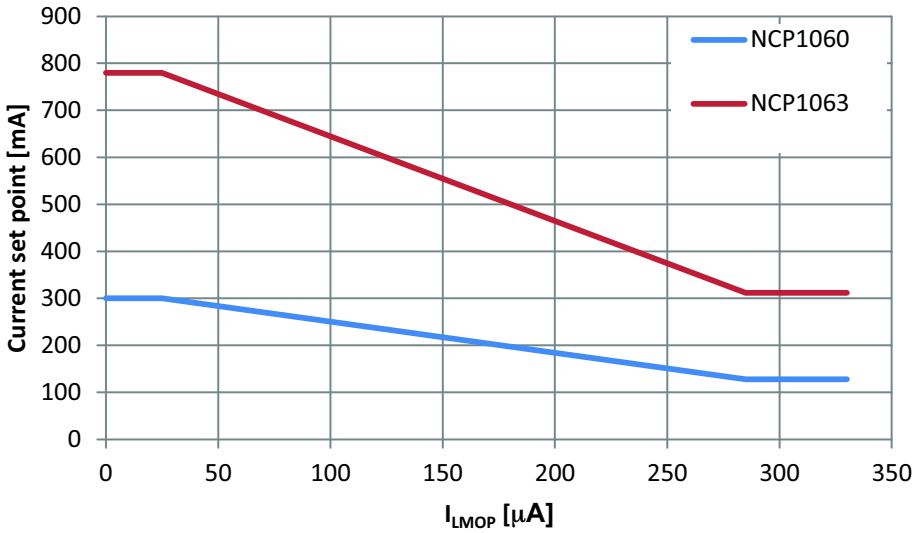


Figure 42. Ipk Set−point Dependence on I_{LMOP} Current

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the power switch on−time, this point dips to $-NV_{in}$, N being the turns ratio between the primary winding and the auxiliary winding. The negative plateau on auxiliary winding will have an amplitude dependant on the input voltage. Resistors R_{OPPU} and R_{OPPL} (Figure 43) define current drawn from LIM/OPP and the negative voltage on auxiliary winding. The negative voltage is tied up with bulk voltage, so the higher the bulk voltage is, the deeper is the negative voltage on auxiliary winding, the higher current is drawn from LIM/OPP pin and the lower the peak current is. During the internal MOSFET off period, voltage on auxiliary winding is positive, but the IC ignores the LIM/OPP current. The positive LIM/OPP current has no influence on proper IC function.

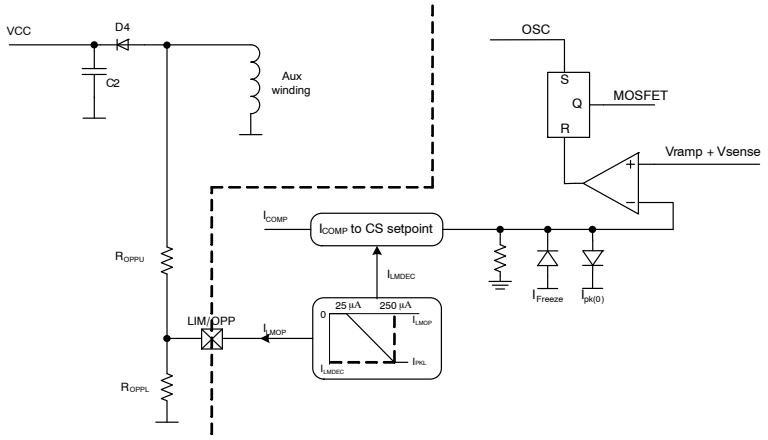


Figure 43. The OPP Circuitry Affects the Maximum Peak Current Set Point

Ramp Compensation and Ipk Set−point

In order to allow the NCP106X to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current−mode control.

Here we got a table of the ramp compensation, the initial current set point, and the final current set−point of different versions of switcher.

	NCP1060		NCP1063	
f_{sw}	60 kHz	100 kHz	60 kHz	100 kHz
S_a	8.4 mA/µs	14 mA/µs	15.6 mA/µs	26 mA/µs
$I_{pk(Duty=50\%)}$	250 mA		650 mA	
$I_{pk(0)}$	300 mA		780 mA	

Figure 44 depicts the variation of I_{PK} set−point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

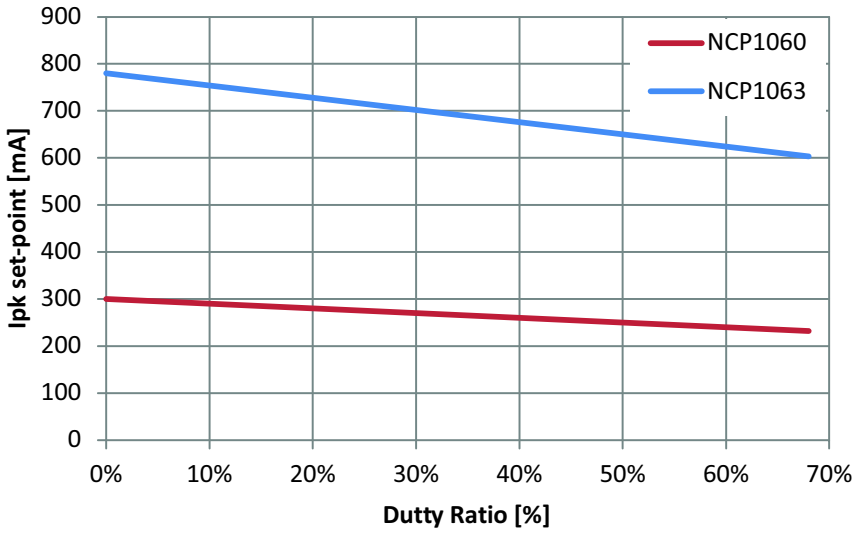


Figure 44. I_{PK} Set−point Varies with Power Switch on Time, which is Caused by the Ramp Compensation

FB Pin Function

The FB pin is used in non isolated SMPS application only. Portion of the output voltage is connected into the pin. The voltage is compared with internal V_{REF} (3.3 V) using Operation Transconductance Amplifier (Figure 45). The OTAs output is connected to COMP pin. The OTA output is accessible through the COMP pin and is used for the loop compensation, usually an RC network. The current capability of OTA is limited to −150 µA typically. The positive current is defined by internal $R_{COMP(up)}$ resistor and $V_{COMP(ref)}$ voltage. If FB path loop is broken (i.e. the FB pin is disconnected), an internal current I_{FB} (1 µA typ.) will pull up the FB pin and the IC stops switching to avoid uncontrolled output voltage increasing.

In isolated topology, the FB pin should be connected to GND pin. In this configuration no current flows from OTA to COMP pin (OTA is disabled) so the OTA has no influence on regulation at all.

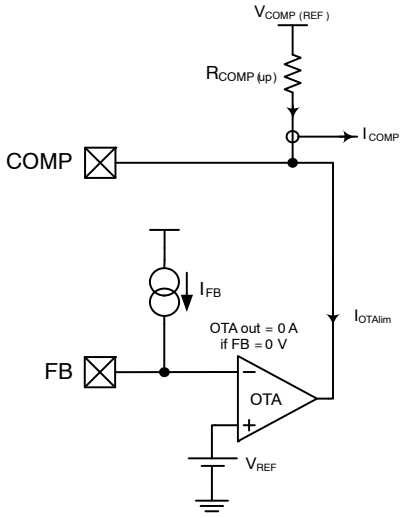


Figure 45. FB Pin Connection

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

V_{in} min = 90 Vac or 127 Vdc once rectified, assuming a low bulk ripple

V_{in} max = 265 Vac or 375 Vdc

V_{out} = 12 V

P_{out} = 5 W

Operating mode is CCM

η = 0.8

1. The lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown in Figure 46. This condition sets the maximum voltage that can be reflected during toff. As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N \cdot (V_{out} + V_f) < V_{in,min} \qquad \text{(eq. 2)}$$

2. In our case, since we operate from a 127 V DC rail while delivering 12 V, we can select a reflected voltage of 120 V dc maximum. Therefore, the turn ratio Np:Ns must be smaller than

$$\frac{V_{reflect}}{V_{out} + V_f} = \frac{120}{12 + 0.5} = 9.6 \text{ or } Np : Ns < 9.6.$$

Here we choose N = 8 in this case. We will see later on how it affects the calculation.

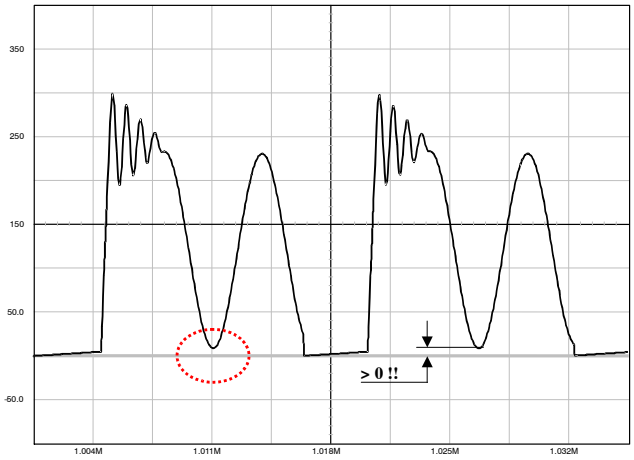


Figure 46. The Drain−source Wave Shall always be Positive

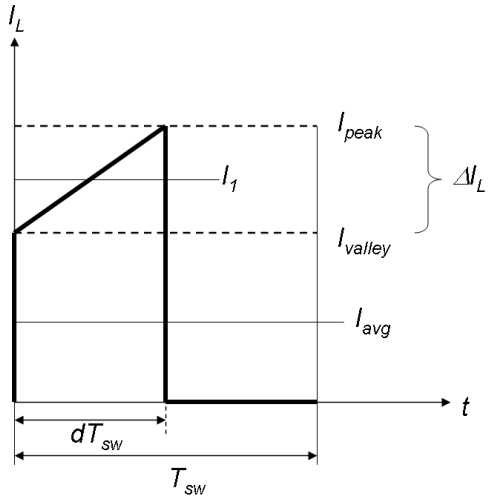


Figure 47. Primary Inductance Current Evolution in CCM

3. Lateral MOSFETs have a poorly doped body−diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{drain,max} = V_{in} + N \cdot (V_{out} + V_f) + I_{peak} \cdot \sqrt{\frac{L_f}{C_{tot}}} \quad \text{(eq. 3)}$$

where L_f is the leakage inductance, C_{tot} the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source), N the N_P:N_S turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_{peak} the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_{peak} is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at V_{in} = 375 Vdc). This voltage is given by the RCD clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty−cycle for this flyback converter operated in CCM:

$$d_{max} = \frac{N \cdot (V_{out} \cdot V_f)}{N \cdot (V_{out} \cdot V_f) + V_{in,min}} = \frac{1}{1 + \frac{V_{in,min}}{N \cdot (V_{out} \cdot V_f)}} = 0.44 \quad \text{(eq. 4)}$$

5. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{in} \cdot d)^2}{f_{sw} \cdot K \cdot P_{in}} \quad \text{(eq. 5)}$$

$$\text{where } K = \frac{\Delta I_L}{I_{Lavg}}$$

and defines the amount of ripple we want in CCM (see Figure 47).

- Small K: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- Large K: approaching DCM where the RMS losses are worse, but smaller inductance, leading to a better leakage inductance.

From Equation 6, a *K* factor of 1 (50% ripple), gives an inductance of:

$$L = \frac{(127 \cdot 0.44)^2}{60k \cdot 1 \cdot 5} = 10.04 \text{ mH}$$

$$\Delta I_L = \frac{V_{in} \cdot d}{L \cdot f_{sw}} = \frac{127 \cdot 0.44}{10.04m \cdot 60k} = 92.8 \text{ mA peak to peak}$$

The peak current can be evaluated to be:

$$I_{peak} = \frac{I_{avg}}{d} + \frac{\Delta I_L}{2} = \frac{49.2 \text{ m}}{0.44} + \frac{92.8 \text{ m}}{2} = 158 \text{ mA}$$

On I_L, I_{Lavg} can also be calculated:

$$I_{Lavg} = I_{peak} - \frac{\Delta I_L}{2} = 158m - \frac{92.8m}{2} = 111.6 \text{ mA}$$

6. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{d,rms} = \sqrt{d \cdot \left(I_{peak}^2 - I_{peak} \cdot \Delta I_L + \frac{\Delta I_L^2}{3}\right)} = \sqrt{0.44 \cdot \left(0.158^2 - 0.158 \cdot 0.0928 + \frac{0.0928^2}{3}\right)} = 57 \text{ mA}$$

If we take the maximum $R_{DS(on)}$ for a 125°C junction temperature, i.e. 34 Ω, then conduction losses worse case are:

$$P_{cond} = I_{d,rms}^2 \cdot R_{DS(on)} = 110 \text{ mW}$$

7. Off−time and on−time switching losses can be estimated based on the following calculations:

$$P_{off} = \frac{I_{peak} \cdot (V_{bulk} + V_{clamp}) \cdot t_{off}}{2T_{SW}} = \frac{0.158 \cdot (127 + 100 \cdot 2) \cdot 10n}{2 \cdot 16.7\ \mu} = 15.5 \text{ mW} \quad \text{(eq. 6)}$$

Where, assume the V_{clamp} is equal to 2 times of reflected voltage.

$$P_{on} = \frac{I_{valley} \cdot \left(V_{bulk} + N \cdot (V_{out} + V_f)\right) \cdot t_{on}}{6 \cdot T_{SW}} \quad \text{(eq. 7)}$$

$$= \frac{0.0464 \cdot (127 + 100) \cdot 10\,n}{6 \cdot 16.7\,\mu}$$

$$= 2.1\ \text{mW}$$

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the t_{off} and t_{on} in Equation 7 and Equation 8 have to be modified after measuring on the bench.

8. The theoretical total power is then
   117 + 15.5 + 2.1 = 127.6 mW
9. If the NCP106X operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:

$$P_{DSS} = I_{CC1} \cdot V_{in.max} = 0.8m \cdot 375 = 300\ \text{mW} \quad \text{(eq. 8)}$$

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BVdss which is 700 V. Figure 48 **a–b–c** present possible implementations:

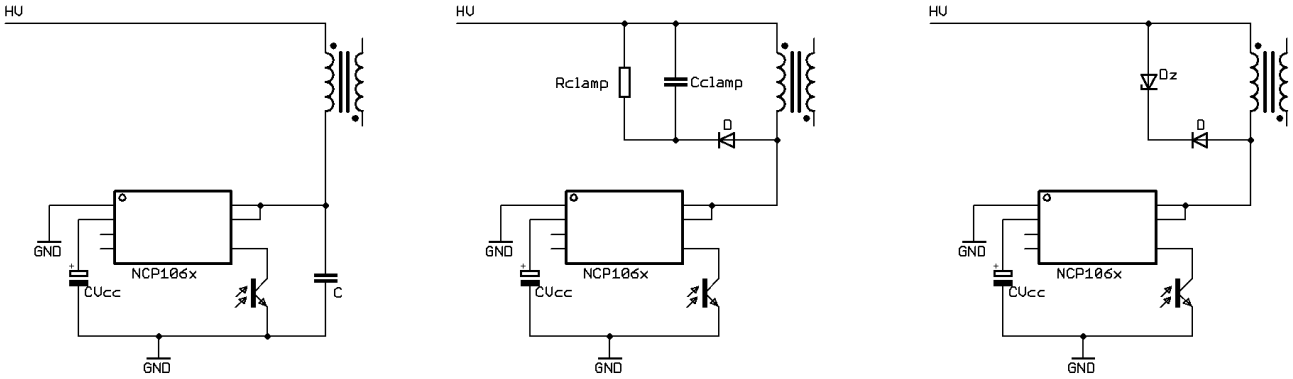


Figure 48. a, b, c : Different Options to Clamp the Leakage Spike

Figure 48a: the simple capacitor limits the voltage according to the lateral MOSFET body−diode shall never be forward biased, either during start−up (because of a large leakage inductance) or in normal operation as shown by Figure 46. This condition sets the maximum voltage that can be reflected during t_{off}. As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you must adopt a turn ratio which adheres to the following Equation 3. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with (Equation 4). Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

Figure 48b: the most standard circuitry is called the RCD network. You calculate R_{clamp} and C_{clamp} using the following formulae:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot \left(V_{clamp} + N \cdot (V_{out} + V_f)\right)}{L_{leak} \cdot I_{leak}^{\,2} \cdot f_{sw}} \quad \text{(eq. 9)}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot f_{sw} \cdot R_{clamp}}$$

V_{clamp} is usually selected 50−80 V above the reflected value N x (V_{out} + V_f). The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worse case occurs when I_{peak} and V_{in} are maximum and V_{out} is close to reach the steady−state value.

Figure 48c: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

As a good design practice, it is recommended to implement one of this protection to make sure Drain pin voltage doesn't go above 650 V (to have some margin between Drain pin voltage and BVdss) during most stringent operating conditions (high Vin and peak power).

Power Dissipation and Heatsinking

The NCP106X welcomes two dissipating terms, the DSS current−source (when active) and the MOSFET. Thus, $P_{tot} = P_{DSS} + P_{MOSFET}$. It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. Take the PDIP−7 package as an example, when surrounded by a surface approximately 200 mm^2 of 35 μm copper, the maximum power the device can thus evacuate is:

$$P_{max} = \frac{T_{Jmax} - T_{ambmax}}{R_{\theta JA}} \quad \text{(eq. 10)}$$

which gives around 870 mW for an ambient of 50°C and a maximum junction of 150°C. If the surface is not large enough, the $R_{\theta JA}$ is growing and the maximum power the device can evacuate decreases. Figure 49 gives a possible layout to help drop the thermal resistance.

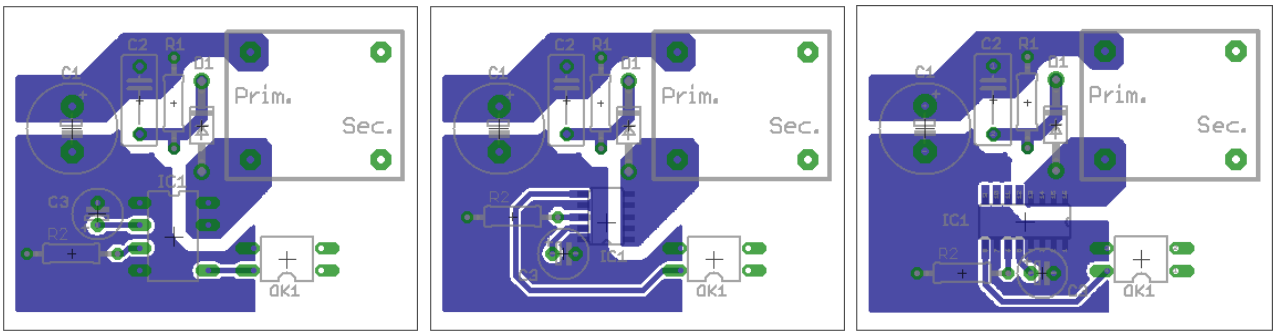


Figure 49. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction−to−Ambient

Bill of material:

C1	Bulk capacitor, input DC voltage is connected to the capacitor
C2, R1, D1	Clamping elements
C3	Vcc capacitor
OK1	Optocoupler
R2	Resistor to setting I_{PEAK} current

Table 6. ORDERING INFORMATION

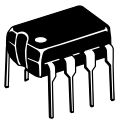
Device	Frequency	$R_{DS(on)}$	Brown In	Package Type	Shipping†
NCP1060AD060R2G	60 kHz	34	Yes	SOIC−10 (Pb−Free)	2500 / Tape & Reel
NCP1060AD100R2G	100 kHz	34	Yes		2500 / Tape & Reel
NCP1060BD060R2G	60 kHz	34	No		2500 / Tape & Reel
NCP1060BD100R2G	100 kHz	34	No		2500 / Tape & Reel
NCP1063AD060R2G	60 kHz	11.4	Yes	SOIC−16 (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

NCP1060AP060G	60 kHz	34	Yes	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1060AP100G	100 kHz	34	Yes		50 Units / Rail
NCP1063AP060G	60 kHz	11.4	Yes	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1063AP100G	100 kHz	11.4	Yes		50 Units / Rail
NCP1063AD100R2G	100 kHz	11.4	Yes	SOIC−16 (Pb−Free)	2500 / Tape & Reel

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

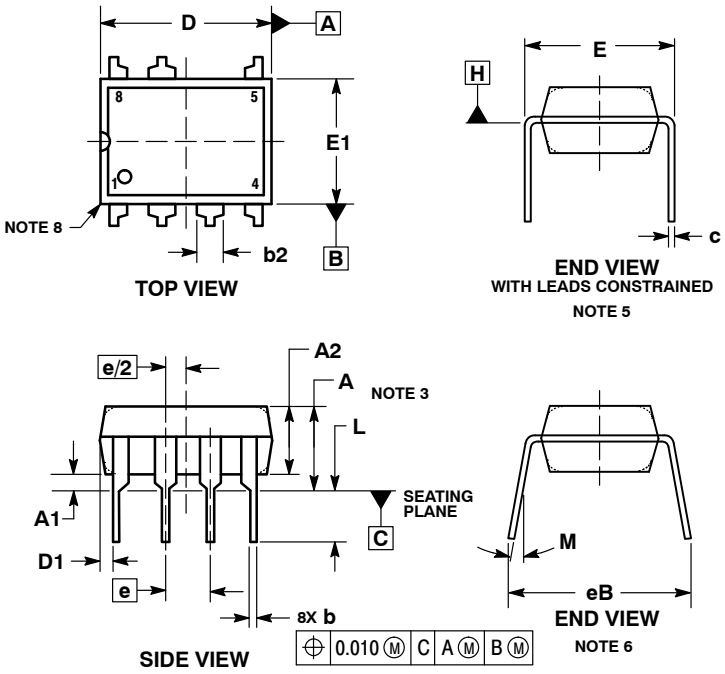
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C

DATE 22 APR 2015

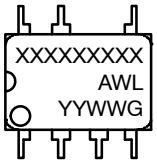
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

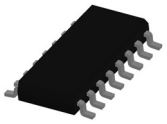
GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

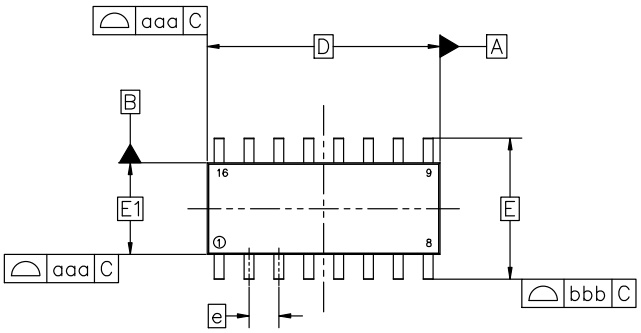
DOCUMENT NUMBER:	**98AON11774D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**PDIP−7 (PDIP−8 LESS PIN 6)**		**PAGE 1 OF 1**



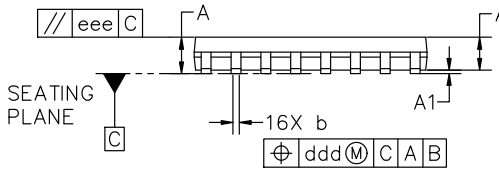
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

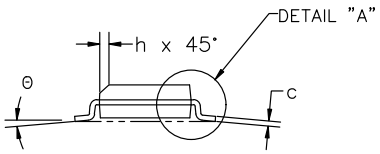
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

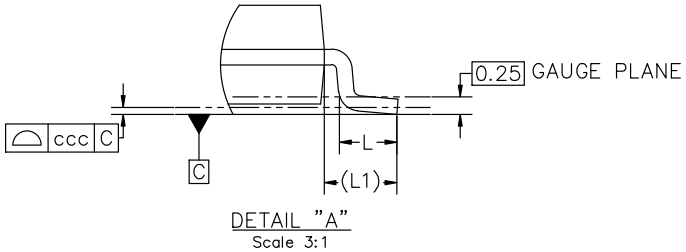


SIDE VIEW

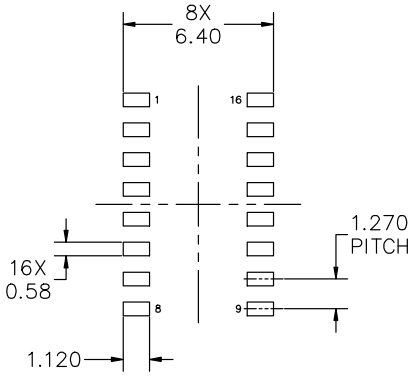


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

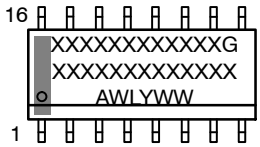
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**	**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

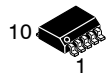
PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

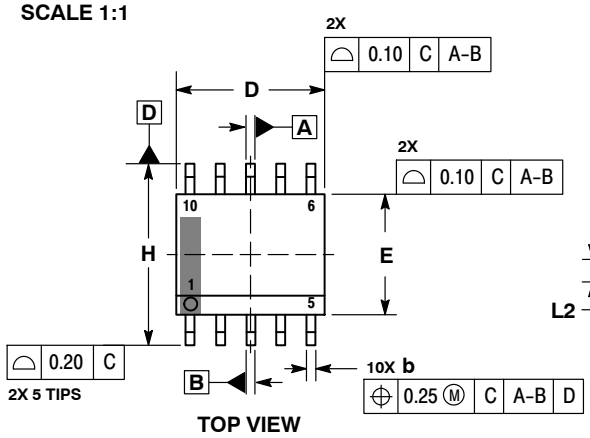
ON Semiconductor®

SOIC−10 NB
CASE 751BQ
ISSUE B

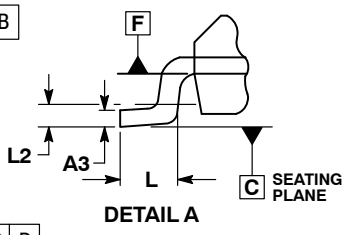
DATE 26 NOV 2013



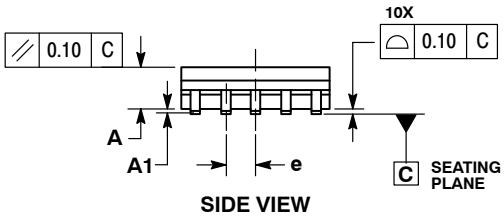
SCALE 1:1



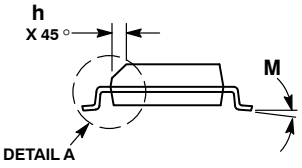
TOP VIEW



DETAIL A



SIDE VIEW

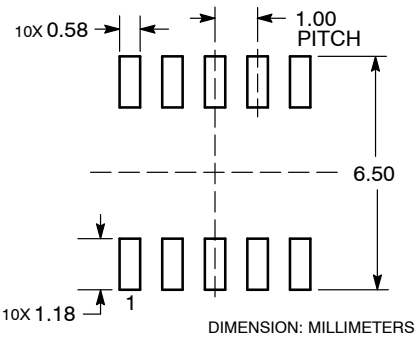


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	0.80
L2	0.25 BSC	
M	0°	8°

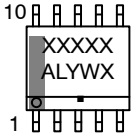
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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DESCRIPTION:	SOIC−10 NB		PAGE 1 OF 1

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