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Design Tool Guide for NCP1118x

Rev. 0.97

Switcher AE

OPS, ASG

Public Information

Abstract

NCP1118x is a highly enhanced switcher based on integrated robust 800 V super-junction MOSFET and a peak current mode PWM control. Even it employs a variety of functions and high reliable protections - a high-voltage startup circuit, mWSaver™ and frequency reduction technology for low standby power consumption, constant output power limit, brown-out, current sensing resistor short protection and etc, so that cost-effective off-line power supply could be designed with less BOM (bill of materials) counts and smaller PCB size.

However, designing with NCP1118x could be somewhat complicated because there are a lot of considerations e.g those plenty of functions & protections, some components for NCP1118x as well as its feedback loop. For the reason, a dedicated design tool for NCP1118x based on MS-Excel is provided with this design tool guide for optimal designs. This design tool guide introduces how to use the dedicated design tool with optimized design procedures while giving an example of 45W flyback converter. Some related documents such as schematic, transformer specification, BOM and experimental results, can be referred to design notes uploaded on the website. Additionally, a behavior simulation model based on Simplis is provided. With the behavior simulation model, design parameters from the design tool could be verified earlier than building up hardware design.

Design Procedures

1. Define Electrical Specification and DC Link Capacitor

2. Determine Operation Mode & L_M of Transformer

3. Select Kind of NCP1118x

4. Design Line Input Voltage Sensing Circuit

5. Design Transformer

6. Design RCD Snubber

7. Select Output Diodes & RC Snubbers

8. Determine Output Capacitor

9. Design Feedback Control Loop

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Before Getting Started

a) Data required for power supplies design using NCP1118x, can be input only at the blue colored cells. Important design parameters can be read in the red colored cells.

b) Select cells with a note marker or put your mouse cursor on that. Then, more tips & information can be found.

c) Additionally, further information helpful to your design provides some guide.

d) If a design does not follow some restrict recommendation, then it will warn through a message like that example.

e) Notice that this design tool provides just guide line for your design reference, but not mandatory to comply.

Public Information

1. Define Electrical Specification

1. Define Electrical Specifications							
A. Input Specification							
Minimum Line voltage (V_{LINE}^{MIN})	90	Vrms					
Maximum Line voltage (V_{LINE}^{MAX})	265	Vrms					
Line Frequency (f_L)	60	Hz					
Brown-out Voltage	60.0	Vrms					
Set Brown-in Voltage ($V_{LINE-BI}$)	77.1	Vrms					
Set Line OVP Voltage ($V_{LINE-OVP}$)	330.0	Vrms					
Set Line OVP Recovery Voltage	312.9	Vrms					
B. Output Speciation							
	$V_{o(n)}$		$I_{o(n)}$		$P_{o(n)}$		$P_{o(n)}/P_o$
1st output for feedback (Ns1)	12	V	3.50	A	42	W	93	%
2nd output (Ns2)	15	V	0.20	A	3	W	7	%
3rd output (Ns3)	0	V	0.00	A	0	W	0	%
4th output (Ns4)	0	V	0.00	A	0	W	0	%
Rated output power (P_o)	45.0	W					
Desired Over Power Level P_{OL}	60	W					
Estimated efficiency (E_{ff})	85	%					
Rated input power (P_{in})	52.9	W					

a) Define input voltage and frequency of a power supply for first step. If an input is from PFC, you may translate the PFC output dc-voltage to ac-voltage.

b) Additionally, set up brown-out voltage. If no need, set up the level to 80~90% of V_{LINE}^{MIN}. Then, $V_{LINE-BI}$ & $V_{LINE-OVP}$ are selected automatically.

c) Define output voltage and current of a power supply for first step.

d) Over power level P_{OL} stands for one just before when over-load protection is triggered, which is typically set up 1.3~1.5 times to P_O considering over power caused by load transient.

e) Generally, 80~90% of efficiency can be achievable in flyback converters using normal output diodes. In case using synchronous rectifiers, more than 90% can be obtained.

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1. Define DC Link Capacitor

2. Determine DC Link Capacitor				
a) DC link capacitor (C_{DC})	100	uF	Okay to use this Cap	
c) Minimum DC link voltage (V_{DC}^{MIN})	97	V		
Maximum DC link voltage (V_{DC}^{MAX})	375	V		

Figure 1. Ripple voltage on DC link capacitor

a) Adjust C_{DC} considering minimum line input voltage either of V_{LINE}^{MIN} or Brown-out. Once you choose proper values, then you will get 'Okay' message as shown in the left figure.

b) Recommended capacitance is 1uF per Watt of P_O at only 220Vac input voltage and 2~3uF per Watt at universal or 110Vac input voltage.

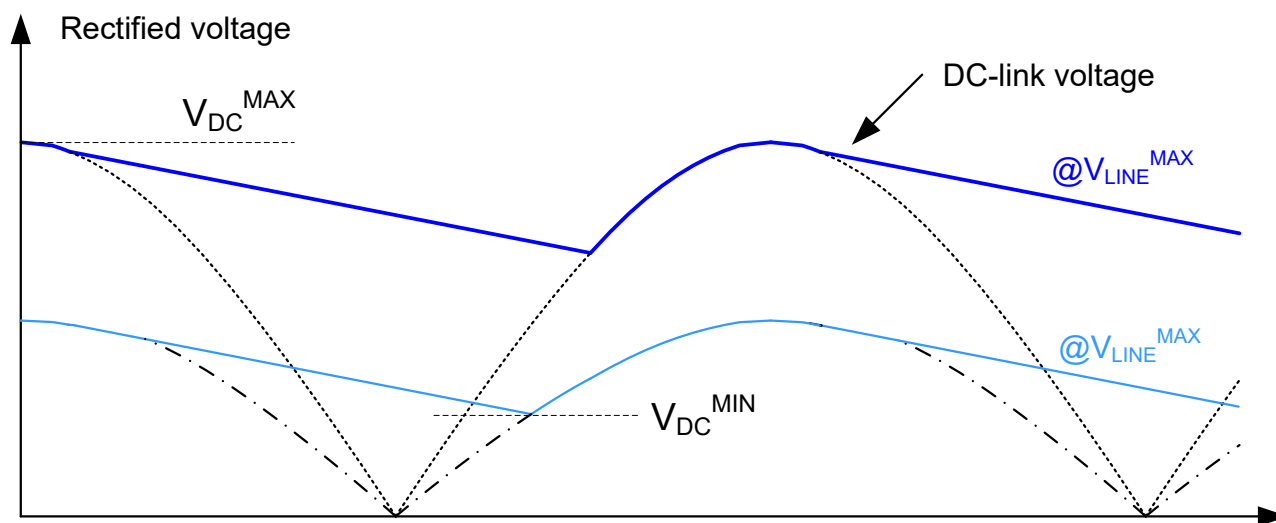c) V_{DC}^{MIN} stands for minimum ripple voltage on C_{DC} at minimum line input voltage.

Public Information

2. Determine Operation Mode & L_M of Transformer

3. Determine Primary-side Inductance (L_M) of Transformer			
a) Output voltage reflected to primary (V_{RO})	85	V	
b) Switching frequency of Switcher (f_s)	65	kHz	
c) Ripple factor (K_{RF}) @ V_{DC}^{MIN}	0.32		
Max. duty ratio @ CCM ($K_{RF} < 1$)	0.468		You choose CCM (KRF<1)
Desired Max.duty ratio @ DCM ($K_{RF} = 1$)	0.484		Valid only DCM (KRF=1)
Estimated Max. duty ratio	0.468		<-Max. Duty is set up by CCM
Recommended magnetizing inductance (L_M)	929	uH	
Select Magnetizing Inductance (L_M)	940	uH	Good Selection

a) Input proper V_{RO}. Recommend V_{RO} of 70 ~ 120 V. Too high V_{RO} makes duty ratio over 0.6 and L_M quite large. Whereas, too low V_{RO} could increase drain current with quite small L_M.

b) Choose fs considering NCP1118x line-up.

c) Unity K_{RF} stands for designing L_M which guarantees discontinuous conduction mode (DCM) in entire input / load condition. $K_{RF}<1$ makes L_M operating in continuous conduction mode (CCM). The smaller K_{RF} is, the more CCM operation is maintained under smaller load condition.
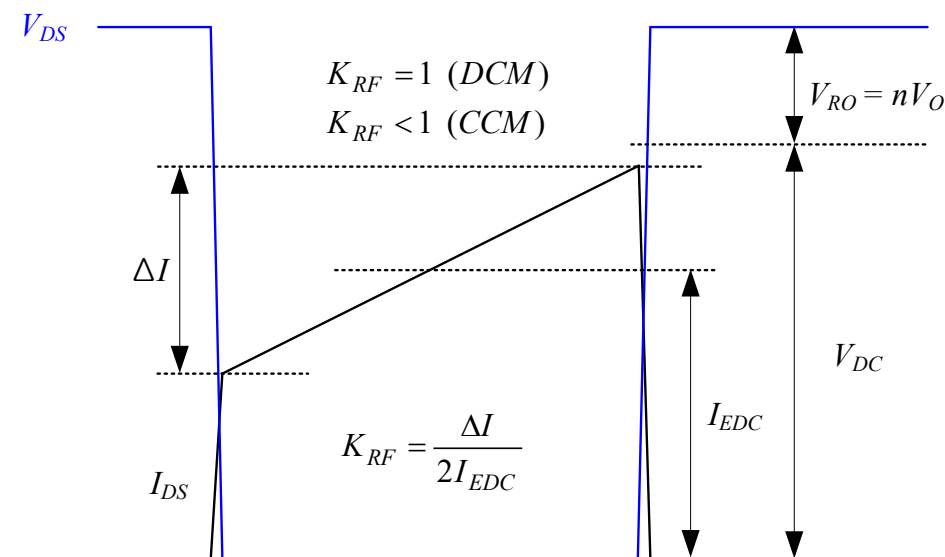

Figure 2. Drain voltage & current waveforms

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2. Determine Operation Mode & L_M of Transformer

3. Determine Primary-side Inductance (L_M) of Transformer			
Output voltage reflected to primary (V_{RO})	85	V	
Switching frequency of Switcher (f_s)	65	kHz	
d) Ripple factor (K_{RF}) @ V_{DC}^{MIN}	0.32		
e) Max. duty ratio @ CCM ($K_{RF} < 1$)	0.468		You choose CCM (KRF<1)
Desired Max.duty ratio @ DCM ($K_{RF} = 1$)	0.484		Valid only DCM (KRF=1)
Estimated Max. duty ratio	0.468		<-Max. Duty is set up by CCM
Recommended magnetizing inductance (L_M)	929	uH	
g) Select Magnetizing Inductance (L_M)	940	uH	Good Selection

d) Recommended K_{RF}: 0.4~1 for universal or only 110Vac, 0.6~1 for only 230Vac.

e) If $K_{RF} < 1$, then max. duty ratio is decided

f) If $K_{RF} = 1$, max. duty ratio can be determined by designers. Recommended value should be less than 0.5.

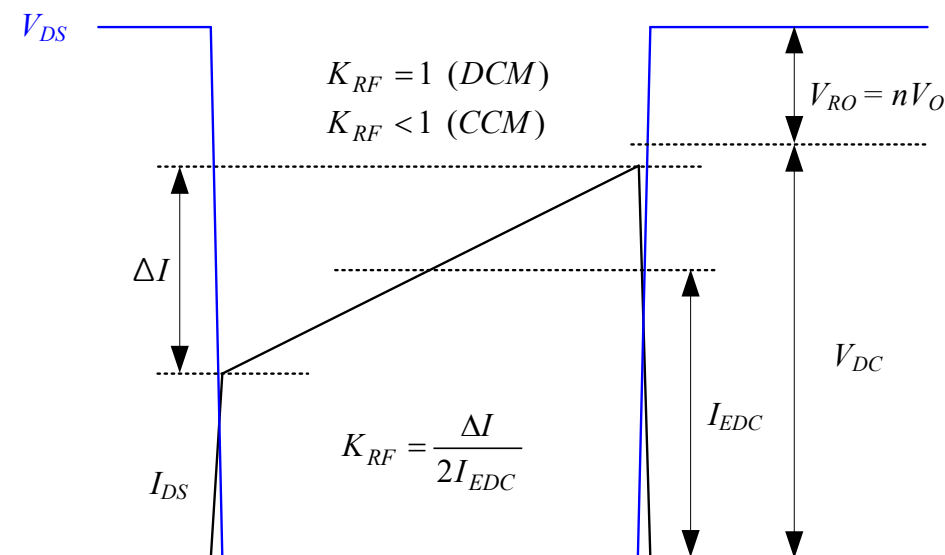g) Choose final L_M based on the value of 'Recommended L_M'

$$K_{RF} = 1 \ (DCM)$$
$$K_{RF} < 1 \ (CCM)$$
$$V_{RO} = nV_O$$
$$K_{RF} = \frac{\Delta I}{2 I_{EDC}}$$

Figure 2. Drain voltage & current waveforms

Public Information

2. Determine Operation Mode & L_M of Transformer

Select Magnetizing Inductance (L_M)	940	uH	Good Selection
a) Estimated Max. duty ratio @ selected L_M	0.468		
Maximum peak drain current (I_{DS}^{peak})	1.54	A	
RMS drain current (I_{DS}^{rms})	0.81	A	
Estimated Max. MOSFET Voltage @ V_{LINE}^{MAX}	502	V	
Estimated Max. MOSFET Voltage @ $V_{LINE-OVP}$	594	V	
b) DC Link Voltage of Boundary btw CCM & DCM	375	V	

a) With the selected L_M, final max. duty, drain current & voltage of MOSFET can be estimated as shown in the table above.

b) This values is a boundary voltage between CCM and DCM. When a dc-link voltage is higher than this value, a flyback with designed L_M starts to be operated under DCM.

3. Select Kind of NCP1118x

4. Select Kind of NCP1118x & Current Sensing Resistor R_{CS}			
$V_{CS\text{-}LIMIT}$ at V_{line}^{min}	0.83	V	
Rcommended Current-sensing Resistor (R_{CS})	0.46	Ω	
b) Selected Current-sensing Resistor (R_{CS})	0.50	Ω	->Good Selection
Estimated Current Limit @ $V_{CS\text{-}LIMIT}$	1.65	A	
Typical Over Power Level Set up by Selected R_{CS}	58	W	
c) Recommended Part	NCP11187		

a) Some key information can be seen e.g which V_{CS} will limit a peak current at min. line input voltage condition, a new peak current and over power can be seen by newly selected R_{CS}.

b) Choose proper R_{CS} considering the recommended R_{CS}.

c) Finally, a proper switcher comes out for the rated power among NCP11184, 5 and 7.

d) For more margin in thermal / power wise, another switcher with bigger MOSFET can be selected.

4. Design Line Input Voltage Sensing Circuit

5. Design Resistors & Capacitor for Line Input Voltage Sensing		
a) Low-side VIN Sensig Resistor (R_{VINL})	270	kΩ
Fixed Brown-in Voltage	77.1	V.rms
Fixed Line OVP Voltage	330.0	V.rms
Line Input Voltage Sensing @ DC-link Capacitor		
R_{VINH1}	32.46	MΩ
c) C_{VIN1}	1.15	nF
Line Input Voltage Sensing Before Rectifier		
R_{VINH2}	20.57	MΩ
C_{VIN2}	156.35	nF

a) Set up R_{VINL}, then the rest of R-C components can be found for two types of line sensing circuit.

b) Total resistance of R_{VINH} & R_{VINL} up to 30Mohm can be used.

c) C_{VIN1} and C_{VIN2} are recommended value to attenuate switching noise sensitivity. These values can be adjust from actual experiment.

Line input voltage sensing at the dc-link capacitor
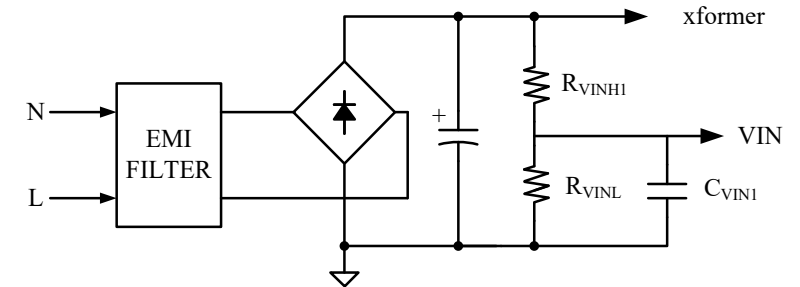
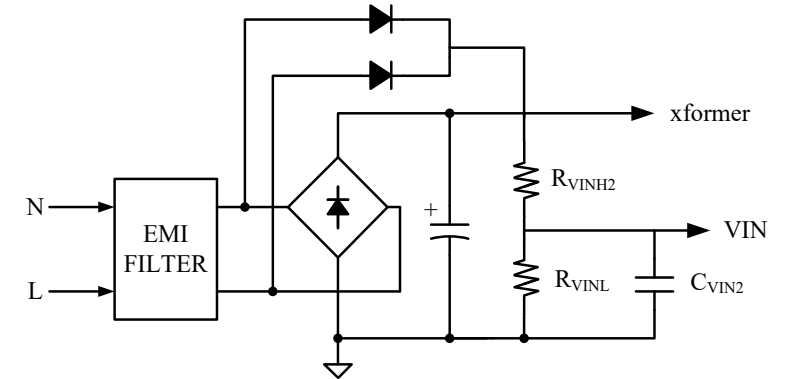Line input voltage sensing before the rectifier

Figure 3. Types of line sensing circuit

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5. Design Transformer

7. Design Transformer					
A. Calculation of min. Primary & Secondary Winding Turns					
a) Allowable Max. flux density (B_{MAX}) @ $V_{CS-LIMIT}$	0.30 Tesla				
b) Cross sectional area of core (A_e)	113 mm^2				
Recommended min. primary turns (N_P^{min})	34.0 T				
c) Choose Winding Turns of 1st Output (N_{S1})	7				
Primary Winding Turns (N_P)	48	->Enough turns			
Secondary Winding Turns	$V_{o(n)}$	$V_{F(n)}$	Calculated N of Turns	Recommended N of Turns e)	
Aux. Winding for V_{CC}	14 V	0.6 V	8.2 T	8 T
1st Output Winding for feedback (N_{S1})	12 V	0.4 V	7.0 T	7 T
2nd Output Winding (N_{S2})	15 V	0.4 V	8.7 T	9 T
3rd Output Winding (N_{S3})	0 V	0 V	0.0 T	0 T
4th Output Winding (N_{S4})	0 V	0 V	0.0 T	0 T

a) Max. flux usage is recommended 0.3~0.35T assuming core saturation level is 0.45T.

b) A_e (cross-sectional area) can be referred to a datasheet of core manufacturers.

c) Adjust N_{S1} to make N_P bigger than N_P^{min}.

d) Input an output voltage of aux. winding (typically 14V) and forward voltage drop of output diodes.

e) Then, recommended the number of turns can be obtained.

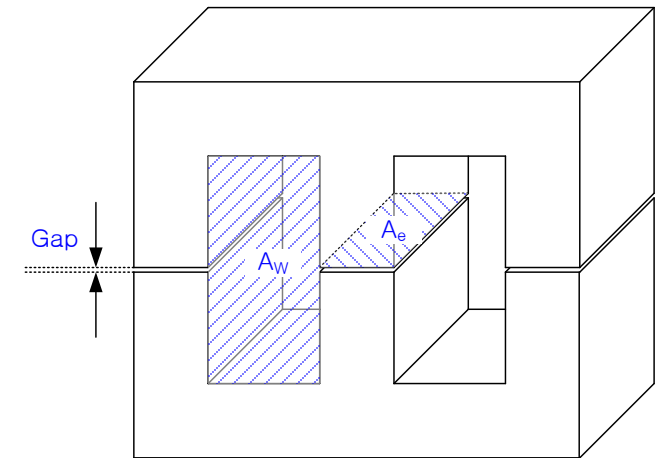f) The number of turns for Vcc should be adjusted from actual experiment

Figure 4. Transformer parameters

Public Information

5. Design Transformer

B. Wire Diameter for Each Winding	a) Diameter		Parallel		$I_{O(n)}^{rms}$		b) Current Density		Turns		Filling Area	
Primary Winding	0.5	mm	1	T	0.8	A	4.2	A/mm^2	48	T	9.42	mm^2
Aux. Winding for V_{CC}	0.25	mm	1	T	0.1	A	2.0	A/mm^2	8	T	0.39	mm^2
1st Output Winding for feedback (N_{S1})	0.65	mm	3	T	5.6	A	5.6	A/mm^2	7	T	6.97	mm^2
2nd Output Winding (N_{S2})	0.25	mm	1	T	0.3	A	6.6	A/mm^2	9	T	0.44	mm^2
3rd Output Winding (N_{S3})	0	mm	0	T	0.0	A	0.0	A/mm^2	0	T	0.00	mm^2
4th Output Winding (N_{S4})	0	mm	0	T	0.0	A	0.0	A/mm^2	0	T	0.00	mm^2
Copper area (A_C) =	17.23	mm^2										
d) Window area (A_W)	70.35	mm^2										
Fill factor (K_F)=	0.24											
e) Ungapped AL value (AL)	3708	nH/T^2										
Gap length (G) ; center pole gap =	0.43	mm										

$$A_L = \frac{\mu_0 \mu_r A_e}{l_m}$$

a) Fill desired diameter and the number of strands of each winding considering current density against the diameter.

b) Current density from 4 to 6 A/mm^2 is typically recommended.

c) A_W (window area), A_L value can be found in core's datasheet.

d) Adjust A_W to get proper K_F (fill factor) 0.2~0.25 for single output & 0.15~0.2 for multiple output.

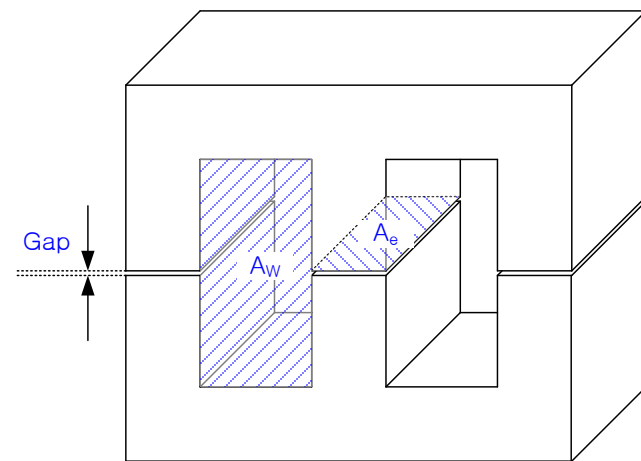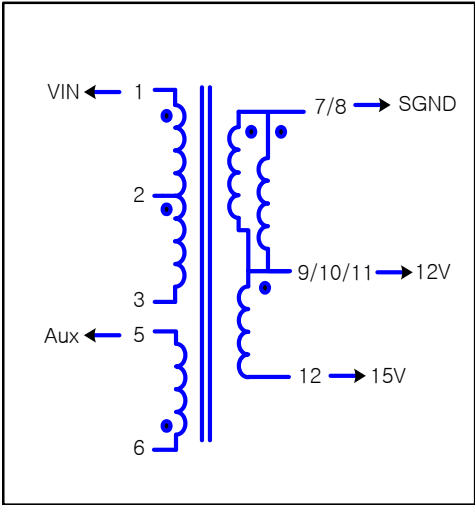e) Put A_L of the core, then gap length can be obtained.

Figure 4. Transformer parameters

5. Design Transformer

a) Previous designed transformer can be summarize as the following diagram & table.

- ✓ **Core : PQ2625**
- ✓ **Lm :940uH**
- ✓ **Leq: 7.5uH**

SETP	WINDING	MATERIAL	Parallel	START-FINISH	TURNS	TAPE
1	N_p	UEW- ϕ 0.45	1	1-2	24^{TS}	1^{TS}
2	N_{12V}	TIW - ϕ 0.4	3	7-9	7^{TS}	1^{TS}
3	N_{12V}	TIW - ϕ 0.4	3	8-10	7^{TS}	1^{TS}
4	N_{s5V}	TIW - ϕ 0.25	1	11-12	2^{TS}	1^{TS}
5	N_{Aux}	TIW - ϕ 0.2	1	6-5	9^{TS}	1^{TS}
6	N_p	UEW- ϕ 0.45	1	2-3	24^{TS}	1^{TS}

6. Design RCD Snubber

a) Put measured leakage inductance, desired V_{SN} and max. V_{SN} ripple.

b) It recommends that V_{SN} is 1.5 ~ 2 times of V_o.

c) Max. V_{SN} ripple would be 20~50% properly. Too big ripple could cause additional power consumption in light load & low switching frequency.

8. Design RCD Snubber		
a) Primary side leakage inductance (L_{lk})	10	uH
Maximum Voltage of snubber capacitor (V_{sn})	120	V
Maximum V_{sn} ripple	20	%
Snubber resistor (R_{sn})=	4.6	kΩ
Snubber capacitor (C_{sn})=	16.55	nF
Power loss in snubber resistor (P_{sn})=	3.1	W
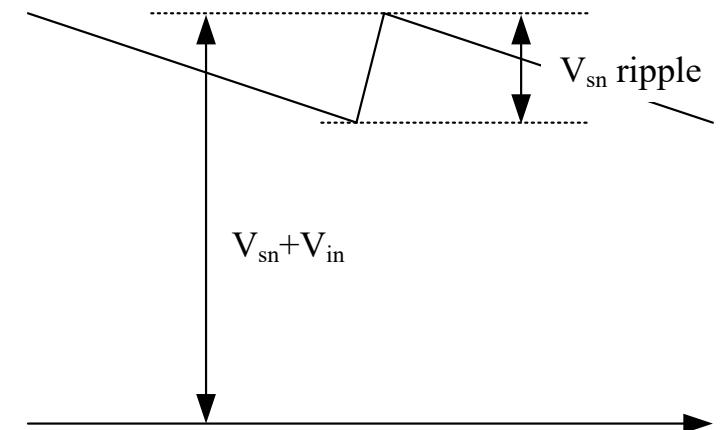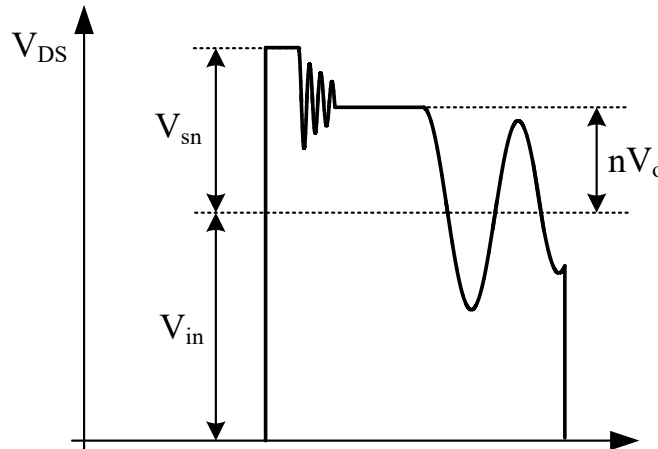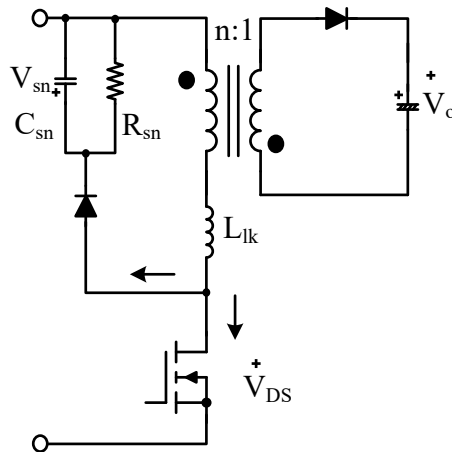
Figure 5. RCD snubber circuit and operating waveforms

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7. Select Output Diodes & RC Snubber

9. Voltage & Current Rating for Rectifier in Secondary Side

	a) Considering V_{LINE}^{MAX}	Considering $V_{LINE-OVP}$	
	$V_{D(n)}$	$V_{D(n)}$	$I_{F(n)}$
Vcc diode	140 V	170 V	0.10 A
1st output diode	120 V	150 V	7.00 A
2nd output diode	150 V	180 V	0.40 A
3rd output diode	0 V	0 V	0.00 A
4th output diode	0 V	0 V	0.00 A

10. Design RC Snubber for Rectifier in Secondary side

	d) $f_{resonant(n)}$	$L_{lk,S(n)}$	$R_{SN(n)}$	$C_{SN(n)}$
1st output diode	27 MHz	0.3 uH	50.9 Ω	0.116 nF
2nd output diode	27 MHz	0.4 uH	67.9 Ω	0.087 nF
3rd output diode	0 MHz	2 uH	0.0 Ω	0.000 nF
4th output diode	0 MHz	2 uH	0.0 Ω	0.000 nF

a) In this section, recommended voltage & current rating of the output diodes can be found depending on max. line input voltage & fixed line OVP voltage. A margin of 1.5 times is taken into account for this selection.

b) RC snubbers could be optionally added to reduce conducted EMI.

c) Measured resonant frequency of voltage spike occurring on diodes and secondary side leakage inductance of a transformer.

d) Put the measured values. But, these should be adjusted based results of actual experiment results.

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8. Determine Output Capacitor

11. Determine Output Capacitor				
	$C_{o(n)}$	$ESR_{C(n)}$	$I_{C(n)}$	세로 (값) 축 $V_{o(n)}$
1st output capacitor	4400 uF	10 mΩ	4.4 A	0.11 V
2nd output capacitor	680 uF	38 mΩ	0.3 A	0.03 V
3rd output capacitor	uF	mΩ	0.0 A	0.00 V
4th output capacitor	uF	mΩ	0.0 A	0.00 V

a) Ripple voltage of the outputs consists of voltage caused by ESR(equivalent series resistor) and switching noise.

b) In this estimation, switching noise is not considered. Thus, the capacitance should be chosen considering actual experimental result.

c) Roughly, choose capacitance of 100uF per 0.1A in low output voltage less than 15V and adjust it considering actual ripple voltage.

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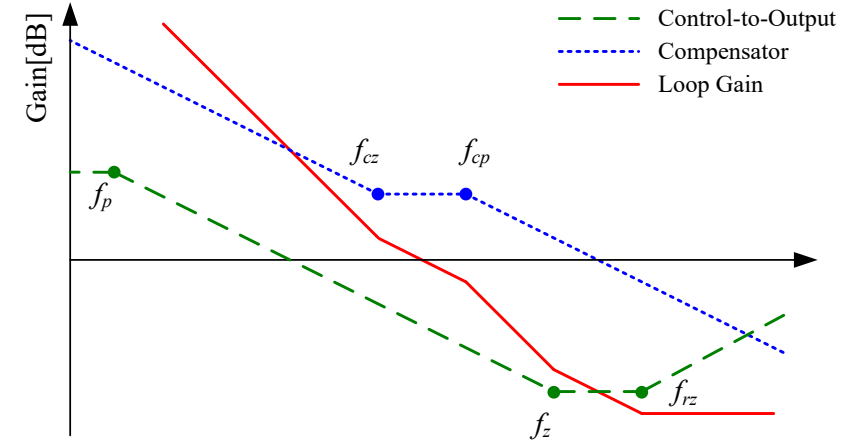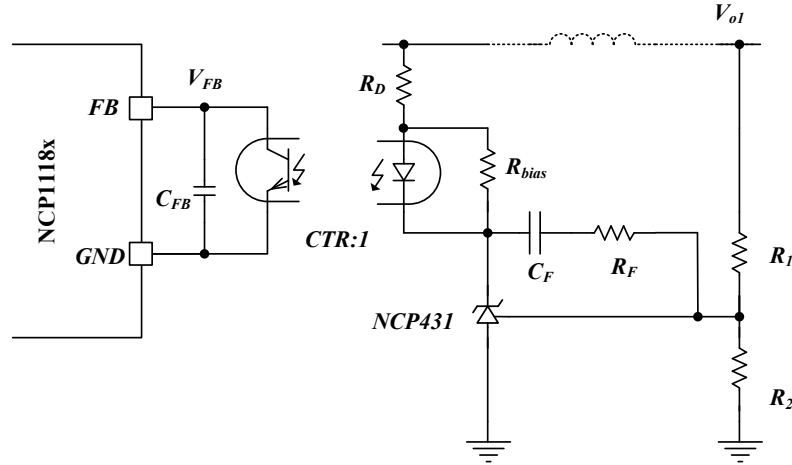# 9. Design Feedback Control Loop

Figure 6. Typical feedback circuit and gain curve

a) f_p, f_z & f_{rz} are a pole, zero and right half-plane zero in a transfer function of typical flyback converter with CCM. f_{cz} and f_{cp} are for the feedback circuit shown in the left.

b) Each transfer function can be simply expressed as following.

Control-to-Output: $\dfrac{\hat{v}_o}{\hat{v}_{FB}} = K_{DC} \cdot \dfrac{\left(1 + \dfrac{s}{\omega_z}\right)\left(1 - \dfrac{s}{\omega_{rz}}\right)}{1 + \dfrac{s}{\omega_p}}$

Compensator: $\dfrac{\hat{v}_{FB}}{\hat{v}_o} = \dfrac{\omega_i}{s} \cdot \dfrac{1 + \dfrac{s}{\omega_{cz}}}{1 + \dfrac{s}{\omega_{pc}}}$

$K_{DC} = \dfrac{I_{LIM}}{V_{FB,Max}} \dfrac{R_L \cdot V_{IN}}{2V_{RO} + V_{IN}} \dfrac{N_P}{N_S}$, $\omega_z = \dfrac{1}{ESR_C \cdot C_o}$, $\omega_{rz} = \dfrac{R_L(1-D)^2}{D \cdot L_M(N_S / N_P)^2}$, $\omega_p = \dfrac{(1-D)}{R_L \cdot C_o}$

$\omega_i = \dfrac{R_{FB}}{R_1 R_D C_F}$, $\omega_{cz} = \dfrac{1}{C_F(R_F + R_1)}$, $\omega_p = \dfrac{1}{R_{FB} \cdot C_{FB}}$

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9. Design Feedback Control Loop

15. Design Feedback Control Loop		
Control-to-output DC gain =	3.4	
Control-to-output zero (f_z) =	3,617	Hz
Control-to-output RHP zero (f_{rz})=	17,825	Hz
Control-to-output pole (f_p)=	19	Hz

Recommended Value				
R_D Range	1.06	~	6.38	kΩ
C_{FB} Range	0.7	~	2.7	nF
R_F Range	0	~	221.0	kΩ
C_F Range	2.0	~	19.9	nF

a) The design tool calculates a transfer function of the designed flyback converter and shows key parameters for designing feedback loop, e.g. a dc gain, zero and pole

b) A bode plot of gain & phase can be found in the graphs.

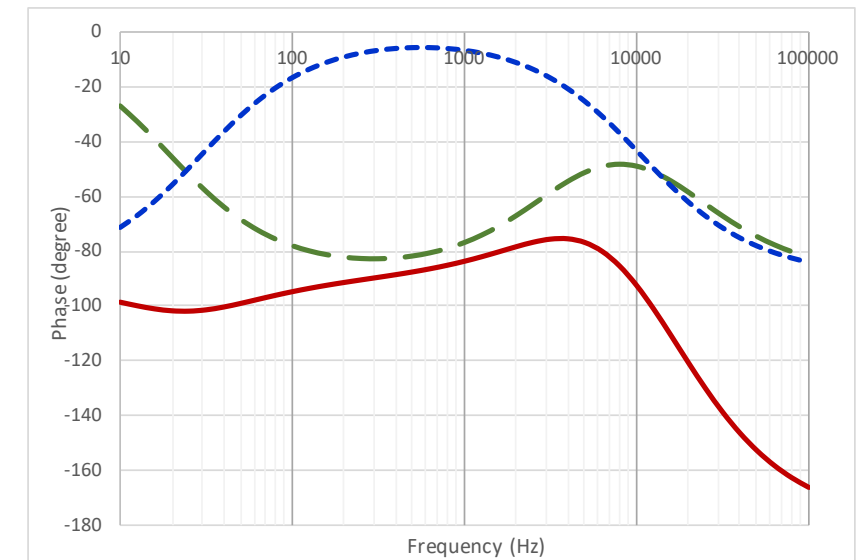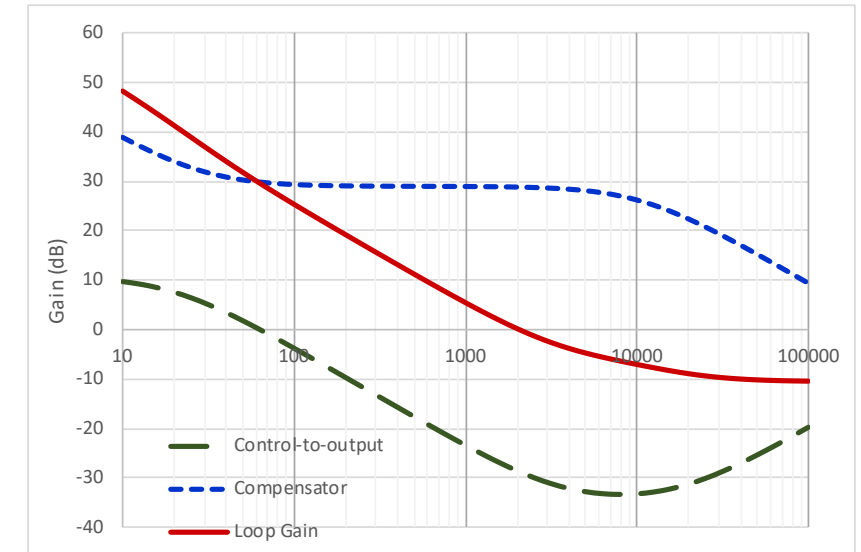c) Recommended values of the compensator can be referred to the table.

Figure 7. Bode plot of the transfer functions

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9. Design Feedback Control Loop

a) Set up fc. Generally, f_c is set up lower than 1/3 of f_{rz} in CCM or high frequency in DCM due to no f_{rz} in the mode.

b) f_{cz} and f_{cp} are generally set around $f_c/3$ and $3f_c$, respectively.

c) Based on these rules, a compensator design can be started. Notice that this design procedure is a reference and should be checked and adjusted from actual experiment.

d) CTR can be found in datasheet of opto-couplers.

e) In the equation shown in previous page, R_D and R_1 are one of factors to determine dc-gain of the compensator. Thus, set them up and make the dc-gain so as to cancel a gain of the control-to-output transfer function at f_c.

f) R_1 can be set up considering bias current of a voltage reference IC and current consumption of total dividing resistance.

g) The bigger C_{FB} makes f_{cp} & bandwidth go down low frequency so response of the converter could go slower as well.

h) R_F and C_F determines f_{cz} position and dc-gain. As C_F increases, feedback loop could be more stable, but low frequency is subject to decrease.

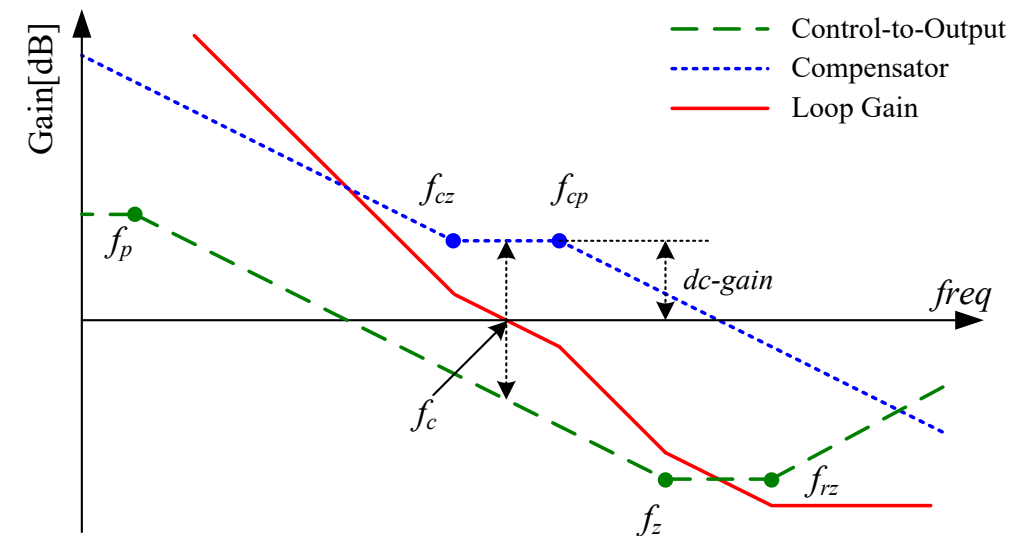|	
Set desired crossover frequency (fc)	2 kHz
Opto coupler current-transfer ratio (CTR)	1 A/A
Voltage divider resistor (R₁)	144.0 kΩ
Voltage divider resistor (R₂)=	37.7 kΩ
Shunt regulator Bias resistor (R_bias)	1 kΩ
Opto coupler diode resistor (R_D)	0.75 kΩ
Feeback pin capacitor (C_FB) =	1 nF
Feedback resistor (R_F) =	56 kΩ
Feedback Capacitor (C_F) =	27 nF

Figure 7. Bode plot of the transfer functions

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Appendix (will be updated)

✓ NCP1118x Pages

-https://www.onsemi.com/~~~

✓ Reference Board Link

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Thanks You