

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# NCP4326

## Secondary Controller for Multi-Output Quasi-Resonant Switchmode Power Supplies

This secondary controller significantly improves the overall efficiency and cross-regulation figures when used in a Switchmode Power Supply. Compared to traditional regulation schemes, the NCP4326 provides superior performance in cross-regulation by individually regulating outputs. Powered from a main winding, the device actuates two independent switches that precisely adjust the considered outputs to resistor-selectable voltages. This controller also integrates a precision reference voltage, which together with a dedicated operational amplifier reduces the feedback loop elements to the minimum. In the end three independent output voltages can be controlled by a single device.

A skip cycle feature improves the stand by power in light load condition. Finally, dedicated shutdown pins offer an easy mean to disable the secondary outputs in applications where a low standby power performance is key.

### Features

- 0% to 100% Duty Cycle Range
- Integrated Shunt Regulator for Optocoupler Control
- Internal Voltage Reference (1.25 V, 1% @ 25°C)
- 2 Independent Power MOSFET Drivers
- Enable/Disable for Each Driver
- Independent Soft-Starts on both Output Drivers
- Independent Skip Cycle on both Output Drivers
- Standby Pin
- 580 / 650 mA Peak Current Source/Sink Driver Capability
- Synchronization Pin
- 5 V Undervoltage Lock-Out on Vcc
- This is a Pb-Free Device

### Applications

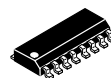
- Consumer Electronics Applications:  
DVD, Set Top Box, CDR, Game Console
- Any Multi-Output Voltage Quasi-Resonant SMPS



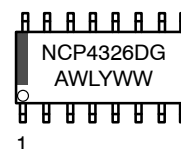
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM

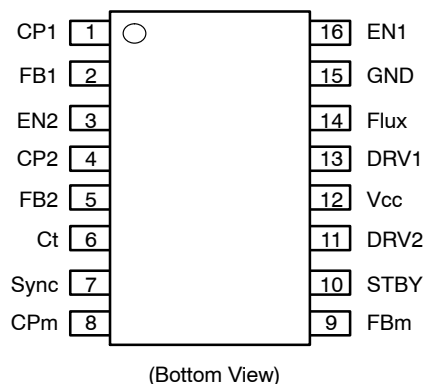


SOIC-16  
D SUFFIX  
CASE 751B



A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Device

### PIN CONNECTIONS

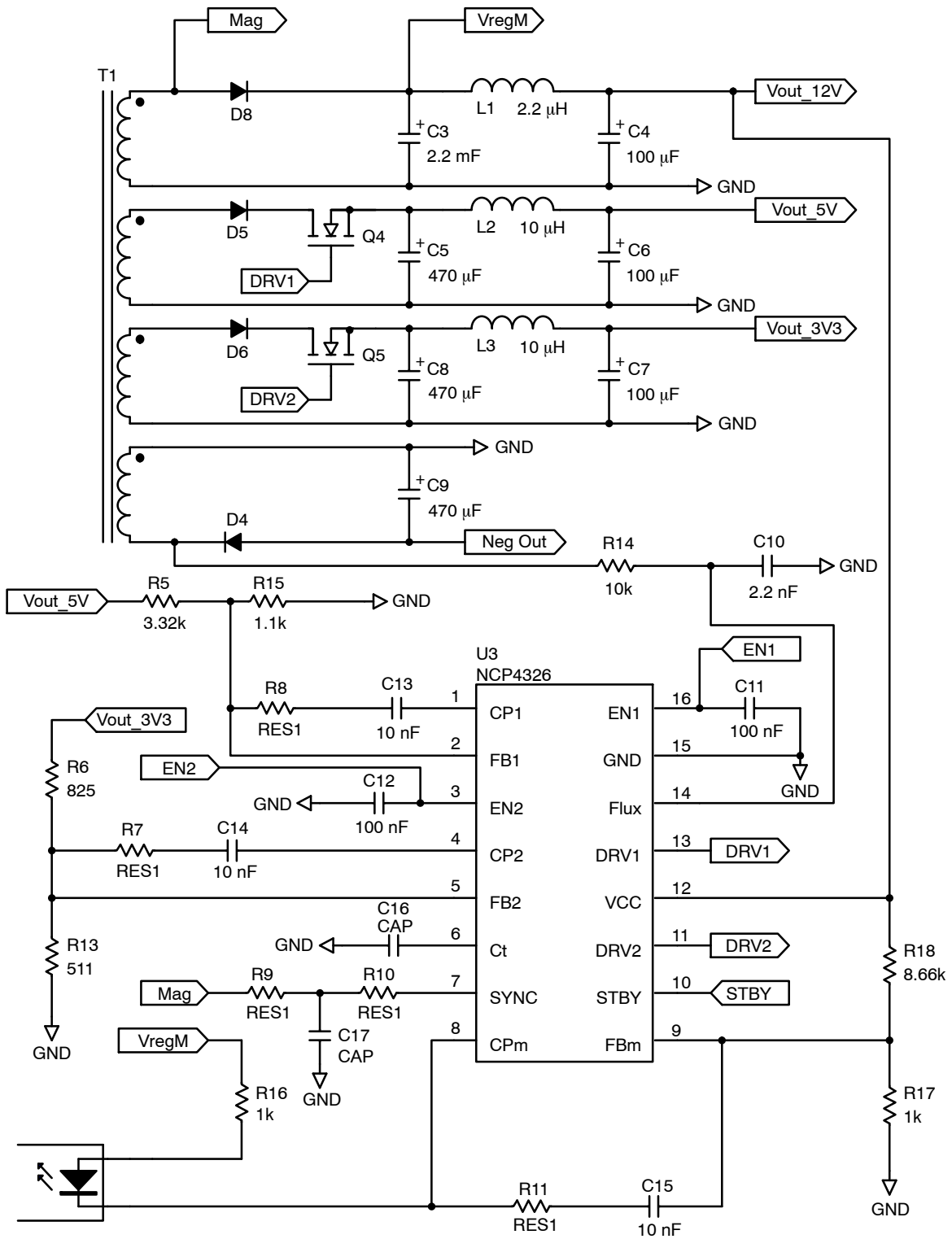


### ORDERING INFORMATION

| Device      | Package              | Shipping <sup>†</sup> |
|-------------|----------------------|-----------------------|
| NCP4326DR2G | SOIC-16<br>(Pb-Free) | 3000 Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP4326



**Figure 1. Typical Application Schematic**

# NCP4326

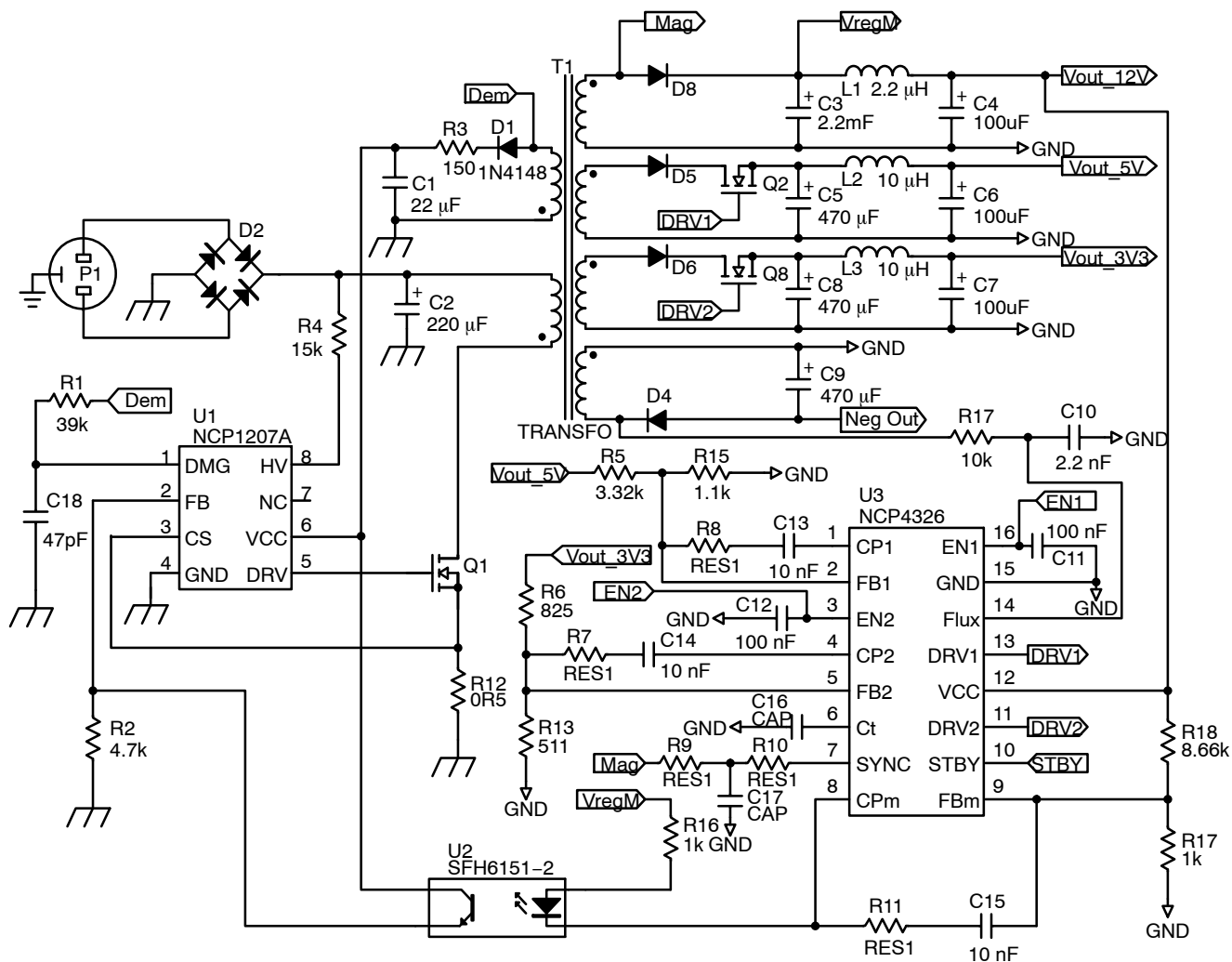


Figure 2. Typical Application Schematic

# NCP4326

## PIN FUNCTION DESCRIPTION

| Pin No. | Symbol | Type  | Description   |
|---------|--------|---|---|
| 1       | CP1    | Error Amplifier Output 1                      | This pin is the output of the error amplifier 1 (monitoring the secondary voltage #1) and is available for loop compensation purpose.   |
| 2       | FB1    | Voltage Feedback 1                            | This is the inverting input of the error amplifier 1. It is connected to the secondary voltage #1 via a bridge resistor divider.  |
| 3       | EN2    | Soft-Start and Enable or Disable the Driver 2 | This pin enables or disables the driver 2. An internal current source with an external capacitor generates also a soft-start feature for limiting the startup peak current on the controlled output.<br>This pin can be left open and by default it enables the driver 2, but without soft-start feature. |
| 4       | CP2    | Error Amplifier Output 2                      | This pin is the output of the error amplifier 2 (monitoring the secondary voltage #2) and is available for loop compensation purpose.   |
| 5       | FB2    | Voltage Feedback 2                            | This is the inverting input of the error amplifier. It is connected to the secondary voltage #2 via a bridge resistor divider.  |
| 6       | Ct     | Ct Pin  | Connect the timing capacitor between Ct and the ground.   |
| 7       | Sync   | Synchronization Pin                           | This pin monitors the main secondary winding, detects the beginning and the end of the demagnetization phase ( $T_{OFF}$ time on the primary winding) and allows the regulation on the two secondary outputs.   |
| 8       | CPm    | Shunt Regulator Output                        | This pin is the output of the shunt regulator (monitoring the main secondary voltage). An open collector configuration is implemented.  |
| 9       | FBm    | Main Voltage Feedback                         | This is the inverting input of the internal error amplifier. It is connected to the main output voltage via a bridge resistor divider.  |
| 10      | STBY   | Standby                                       | This pin is internally pulled up and allows standby mode feature. This pin can be left open and by default it enables standard working mode. When this pin is pulled down standby mode is activated and the quiescent current is reduced to the minimum. The output drivers are disabled.                 |
| 11      | DRV2   | Output Driver 2                               | This output directly drives the gate of a power MOSFET.   |
| 12      | Vcc    | Supplies the IC                               | This pin is connected to the main secondary output voltage and internally powers the IC.  |
| 13      | DRV1   | Output Driver 1                               | This output directly drives the gate of a power MOSFET.   |
| 14      | Flux   | Voltage image of the magnetic flux            | A RC network connected between this pin and a forward winding or a negative output winding generates the transformer's flux image. This flux image is compared to a slow ramp generated on ENx pin for the soft-start Duty Cycle generation controlling the both outputs.                                 |
| 15      | GND    | The IC ground                                 | -   |
| 16      | EN1    | Soft-Start and Enable or Disable the driver 1 | This pin enables or disables the driver 1. An internal current source with an external capacitor generates also a soft-start feature for limiting the startup peak current on the controlled output.<br>This pin can be left open and by default it enables the driver 1, but without soft-start feature. |

# NCP4326

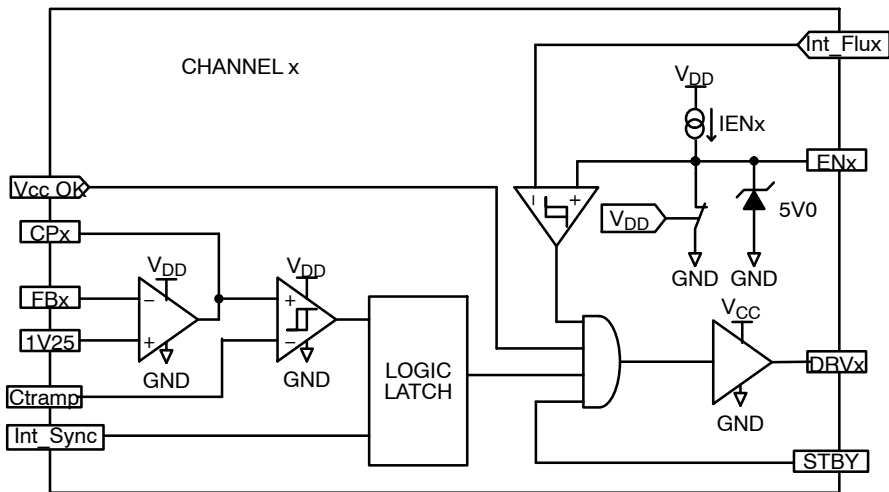
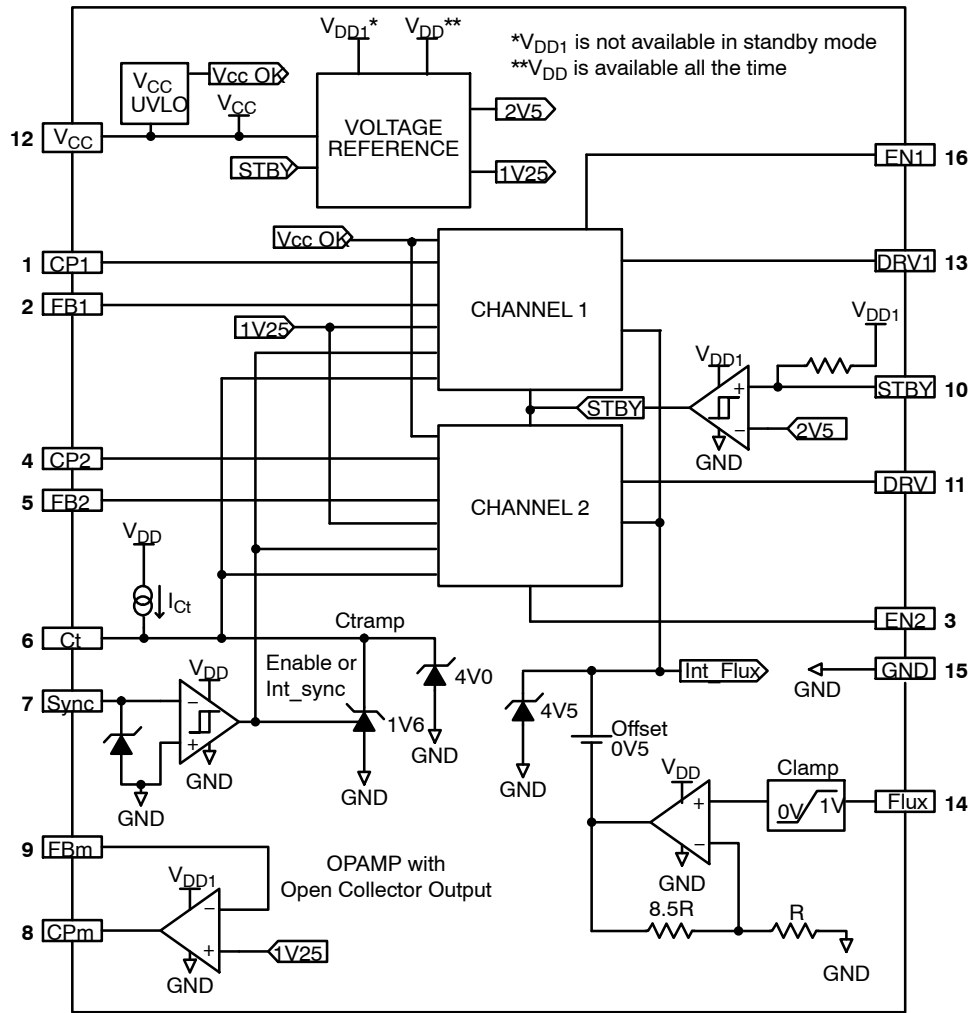


Figure 3. Internal Circuit Architecture

# NCP4326

## MAXIMUM RATINGS

| Rating  | Symbol                 | Value       | Unit                        |
|---|------------------------|-------------|-----------------------------|
| Power Supply Voltage on Pin 12 (Vcc), Pin 8 (CPm) and Pin 13/11 (DRV1/DRV2)                               |                        | 16          | V                           |
| Maximum Voltage on all other pins except Pin 12 (Vcc), Pin 8 (CPm) and Pin 13/11 (DRV1/DRV2)              |                        | -0.3 to 6   | V                           |
| Maximum Current into all pins except Pin 12 (Vcc) and Pin 13/11 (DRV1/DRV2) when ESD diodes are activated |                        | 5           | mA                          |
| Maximum current in Pin 7 (Sync)   |                        | +3/-3       | mA                          |
| Thermal Resistance, Junction-to-Case  | $R_{\theta JC}$        | 55          | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Air   | $R_{\theta JA}$        | 150         | $^{\circ}\text{C}/\text{W}$ |
| Maximum Junction Temperature  | $T_{JMAX}$             | 150         | $^{\circ}\text{C}$          |
| Storage Temperature Range   |                        | -60 to +150 | $^{\circ}\text{C}$          |
| ESD Capability  | Human Body Model (HBM) | 2           | kV                          |
|   | Machine Model (MM)     | 200         | V                           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# NCP4326

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$  unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|----------------|-----|--------|-----|-----|-----|------|
|----------------|-----|--------|-----|-----|-----|------|

## Drive Output (Note 1)

|   |        |                   |          |              |            |    |
|---|--------|-------------------|----------|--------------|------------|----|
| Output Voltage Rise Time ( $C_L = 1.0\text{ nF}$ , $T_J = 25^\circ\text{C}$ )   | 11, 13 | $t_{r1,2}$        | –        | 60           | 100        | ns |
| Output Voltage Fall Time ( $C_L = 1.0\text{ nF}$ , $T_J = 25^\circ\text{C}$ )   | 11, 13 | $t_{f1,2}$        | –        | 40           | 100        | ns |
| Output Voltage Low State @ $V_{CC} = 15\text{ V}$<br>( $I_{\text{sink}} = 250\text{ mA}$ )<br>( $I_{\text{sink}} = 20\text{ mA}$ )      | 11, 13 | $V_{OL1,2}$       | –<br>–   | 1.5<br>1.0   | 2.2<br>1.5 | V  |
| Output Voltage Low State with UVLO activated @ $V_{CC} = 4.0\text{ V}$<br>( $I_{\text{sink}} = 1.0\text{ mA}$ ) (Note 1)                | 11, 13 | $V_{OL\_UVLO1,2}$ | –        | 0.5          | 1.0        | V  |
| Output Voltage High State @ $V_{CC} = 15\text{ V}$<br>( $I_{\text{source}} = 250\text{ mA}$ )<br>( $I_{\text{source}} = 20\text{ mA}$ ) | 11, 13 | $V_{OH1,2}$       | 11<br>12 | 13.4<br>13.5 | –<br>–     | V  |

## Standby Pin

|  |    |                        |   |     |   |                  |
|--|----|------------------------|---|-----|---|------------------|
| Input Threshold Voltage ( $V_{\text{STBY}}$ increasing)  | 10 | $V_{\text{th}}$        | – | 2.5 | – | V                |
| Hysteresis ( $V_{\text{STBY}}$ decreasing)   | 10 | $V_{\text{H}}$         | – | 600 | – | mV               |
| Standby Propagation Delay when the Standby Mode is activated with 1 nF connected to DRVx pin and with $V_{\text{CPX}} > 4.0\text{ V}$ (Figure 4)                   | 10 | $T_{\text{stby\_on}}$  | – | 550 | – | ns               |
| Standby Propagation Delay when the Standby Mode is released, ENx pin is floating, $V_{\text{CPX}} > 4.0\text{ V}$ and with 1.0 nF connected to DRVx pin (Figure 4) | 10 | $T_{\text{stby\_off}}$ | – | 1.0 | – | $\mu\text{s}$    |
| Pullup Resistor Value  | 10 | $R_{\text{pullup}}$    | – | 40  | – | $\text{k}\Omega$ |

## Enable/Soft-Start Pin

|  |                                     |                          |     |      |     |               |
|--|-------------------------------------|--------------------------|-----|------|-----|---------------|
| Enable Soft-Start Mode or Disable Driver Mode Threshold (Note 2, Figure 5)   | 3, 16                               | $V_{\text{ENX\_TH1}}$    | 0.5 | 0.75 | 1.0 | V             |
| Maximum Voltage on ENx pin ending Soft-Start and Enable the Regulation Mode (Figure 5)   | 3, 16                               | $V_{\text{ENX\_TH2}}$    | –   | 4.5  | 4.8 | V             |
| Voltage on ENx pin when ENx is floating  | 3, 16                               | $V_{\text{ENX\_max1}}$   | –   | 5.0  | –   | V             |
| Voltage on ENx pin with External Sink Current @ 500 $\mu\text{A}$  | 3, 16                               | $V_{\text{ENX\_max2}}$   | –   | 5.1  | –   | V             |
| Internal Current Source when $V_{\text{ENX}} = 2.5\text{ V}$ (Note 3)  | 3, 16                               | $I_{\text{ENX}}$         | 120 | 160  | 220 | $\mu\text{A}$ |
| Turn ON Propagation Delay in Soft-Start Mode (Note 4) when applying an external falling edge on Flux pin from 100 mV to 0 V @ $V_{\text{ENX}} = 1.0\text{ V}$ , $V_{\text{CPX}} = 5.0\text{ V}$ and 1.0 nF connected to DRVx pin. (Timing definition see Figure 6) | 3, 14 and 11<br>or<br>16, 14 and 13 | $T_{\text{SS\_ON}}$      | –   | 450  | 800 | ns            |
| Turn OFF Propagation Delay in Soft-Start Mode (Note 4) when applying an external rising edge on Flux pin from 0 V to 100 mV @ $V_{\text{ENX}} = 1.0\text{ V}$ , $V_{\text{CPX}} = 5.0\text{ V}$ and 1.0 nF connected to DRVx pin. (Timing definition see Figure 6) | 3, 16                               | $T_{\text{SS\_OFF}}$     | –   | 450  | 800 | ns            |
| Discharge time when the controller is placed in Standby or when the $V_{\text{CC}}$ is removed @ $C_{\text{ENX}} = 330\text{ nF}$ from 90% of $V_{\text{EN\_max1}}$ to $V_{\text{ENX\_TH1}}$ (Figure 1)  | 3, 16                               | $T_{\text{stby\_disch}}$ | –   | 1.0  | –   | ms            |

1. The output drivers are kept OFF when the  $V_{\text{CC}} < \text{UVLO}$  level.
2. Below the  $V_{\text{ENX\_TH1}}$  threshold the driver is disabled and above this value the soft-start duty cycle generation is allowed.
3. See characterization curve for charging current versus  $V_{\text{CC}}$  and  $V_{\text{ENX}}$ .
4. Soft-Start mode operation when the  $V_{\text{CPX}}$  pin = 5.0 V (or when the controlled output voltage is not yet in regulation).



# NCP4326

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$  unless otherwise noted.)

| Characteristic  | Pin | Symbol                                       | Min    | Typ        | Max    | Unit          |
|---|-----|--|--------|------------|--------|---------------|
| <b>Flux Pin</b>   |     |  |        |            |        |               |
| Internal Current Sourced by Flux pin when it is grounded (Note 5)   | 14  | $I_{\text{Flux}}$                            | –      | 120        | –      | $\mu\text{A}$ |
| Maximum Sink Current on Flux pin when the internal 1.0 V clamp is activated   | 14  | $I_{\text{Flux\_max}}$                       | –      | –          | 1.0    | mA            |
| Input Clamp Voltage<br>High state: when a current is sunk by pin 14 ( $I_{\text{pin 14}} = I_{\text{Flux\_max}}$ )<br>Low state: when a current is sourced by pin 14 ( $I_{\text{pin 14}} = -1.0\text{ mA}$ ) | 14  | $V_{\text{Flux\_H}}$<br>$V_{\text{Flux\_L}}$ | –<br>– | 1.4<br>–60 | –<br>– | V<br>mV       |
| Internal Voltage gain of input signal sensed on Flux pin (guaranteed by design)   | 14  | Gain   | –      | 9.5        | –      | N/A           |

## Synchronization Block

|  |                                  |                                    |        |             |        |    |
|--|----------------------------------|------------------------------------|--------|-------------|--------|----|
| Input Threshold Voltage (Vpin 7 decreasing)  | 7                                | $V_{\text{sync\_th}}$              | 50     | 70          | 100    | mV |
| Hysteresis (Vpin 7 increasing)   | 7                                | $V_{\text{sync\_Hyst}}$            | –      | 35          | –      | mV |
| Maximum Sink Current on Sync pin when the internal 7.0 V clamp is activated  | 7                                | $I_{\text{sync\_max}}$             | –      | –           | 3.0    | mA |
| Input Clamp Voltage<br>High state: when a current is sunk by pin 7 ( $I_{\text{pin 7}} = I_{\text{sync\_max}}$ )<br>Low state: when a current is sourced by pin 7 ( $I_{\text{pin 7}} = -3.0\text{ mA}$ )                | 7<br>7                           | $V_{\text{CH}}$<br>$V_{\text{CL}}$ | –<br>– | 7.4<br>–0.3 | –<br>– | V  |
| Delay between the Sync and DRVx pin (Figures 8 and 9), when applying a falling edge on Sync in normal mode operation (Note 6) with 1.0 nF connected to DRVx pin  | 7 and 11<br>or<br>7 and 13       | $T_{\text{prop\_ON}}$              | –      | 200         | 500    | ns |
| Delay between the Ct voltage ( $V_{\text{Ct}}$ ) and DRVx pin (Figures 8 and 9), when applying a rising edge on Ct @ $V_{\text{CPx}} = 1.7\text{ V}$ in normal mode operation (Note 6) with 1.0 nF connected to DRVx pin | 4, 7 and 11<br>or<br>1, 7 and 13 | $T_{\text{prop\_OFF}}$             | –      | 280         | 500    | ns |
| Internal input capacitance at Vpin 7 = 1.0 V   | 7                                | $C_{\text{par}}$                   | –      | 10          | –      | pF |

## Error Amplifier Section 1 and 2

|   |              |  |          |             |           |               |
|---|--------------|--|----------|-------------|-----------|---------------|
| Voltage Feedback Input @ $T_J = 25^\circ\text{C}$ (Note 7)<br>* Voltage follower measurement to reach 1% accuracy   | 2, 5         | $V_{\text{FB1, 2}}$                              | 1.241    | 1.253       | 1.266     | V             |
| Input Bias Current ( $V_{\text{FB}} = 1.30\text{ V}$ )  | 2, 5         | $I_{\text{IB1, 2}}$                              | –        | –0.1        | –         | $\mu\text{A}$ |
| Open Loop Voltage Gain ( $V_{\text{CPx}} = 1.0\text{ V}$ to $5.0\text{ V}$ )  | 2, 5         | $A_{\text{VOL1, 2}}$                             | –        | 90          | –         | dB            |
| Unity Gain Bandwidth ( $T_J = 25^\circ\text{C}$ )   | 2, 5         | $\text{BW}_{1, 2}$                               | –        | 3.3         | –         | MHz           |
| Power Supply Rejection Ratio<br>( $V_{\text{CC}} = 10\text{ V}$ to $15\text{ V}$ , Frequency range 120 Hz)  | 2, 5         | $\text{PSRR}_{1, 2}$                             | –        | 55          | –         | dB            |
| Output Current<br>Sink Current ( $V_{\text{CPx}} = 1.1\text{ V}$ , $V_{\text{FB}} = 1.45\text{ V}$ )<br>Source Current ( $V_{\text{CPx}} = 4.5\text{ V}$ , $V_{\text{FB}} = 1.05\text{ V}$ )    | 1, 4<br>1, 4 | $I_{\text{sink1, 2}}$<br>$I_{\text{source1, 2}}$ | 2.0<br>– | +6.0<br>–13 | –<br>–5.0 | mA            |
| Output Voltage Swing<br>High State ( $R_L = 15\text{ k}$ to Ground, $V_{\text{FB}} = 1.05\text{ V}$ )<br>Low State ( $R_L = 15\text{ k}$ to $V_{\text{CC}}$ , $V_{\text{FB}} = 1.45\text{ V}$ ) | 1, 4<br>1, 4 | $V_{\text{OH1, 2}}$<br>$V_{\text{OL1, 2}}$       | 4.8<br>– | 5.0<br>0.7  | –<br>1.1  | V             |

5. See characterization curves  $I_{\text{Flux\_pin}}$  ( $V_{\text{Flux\_pin}}$ ) with  $-100\text{ mV} < V_{\text{Flux\_pin}} < +100\text{ mV}$ .

6. Normal operation when  $V_{\text{ENX}} > V_{\text{ENX\_TH3}}$ .

7. See characterization curve for Voltage Reference vs. Temperature.

# NCP4326

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$  unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|----------------|-----|--------|-----|-----|-----|------|
|----------------|-----|--------|-----|-----|-----|------|

## Shunt Regulator

|   |   |            |       |       |       |               |
|---|---|------------|-------|-------|-------|---------------|
| Voltage Feedback Input @ $T_J = 25^\circ\text{C}$ (Note 8)<br>* Voltage follower measurement to reach 1% accuracy | 9 | $V_{FB}$   | 1.241 | 1.253 | 1.266 | V             |
| Input Bias Current ( $V_{FB} = 1.30\text{ V}$ )   | 9 | $I_{IB}$   | –     | –0.1  | –     | $\mu\text{A}$ |
| Open Loop Voltage Gain ( $V_{CPM} = 1.0\text{ V}$ to $5.0\text{ V}$ )   | 9 | $A_{VOL}$  | –     | 90    | –     | dB            |
| Unity Gain Bandwidth ( $T_J = 25^\circ\text{C}$ )   | 9 | BW         | –     | 3.3   | –     | MHz           |
| Power Supply Rejection Ratio<br>( $V_{CC} = 10\text{ V}$ to $15\text{ V}$ , Frequency range 120 Hz)               | 9 | PSRR       | –     | 55    | –     | dB            |
| Output Current – Sink Current ( $V_{CPM} = 1.1\text{ V}$ , $V_{FB} = 1.45\text{ V}$ )                             | 8 | $I_{sink}$ | 12    | 60    | –     | mA            |
| Output Voltage Swing – Low State ( $R_L = 15\text{ k}$ to $V_{CC}$ , $V_{FB} = 1.45\text{ V}$ )                   | 8 | $V_{OL}$   | –     | 0.7   | 1.1   | V             |

## Ct Pin

|   |   |                 |     |     |     |               |
|---|---|-----------------|-----|-----|-----|---------------|
| Minimum Voltage on Ct pin   | 6 | $V_{CT\_min}$   | 1.4 | 1.6 | –   | V             |
| Maximum Voltage on Ct pin when Ct pin is floating   | 6 | $V_{CT\_max1}$  | –   | 4.0 | –   | V             |
| Maximum Voltage on Ct pin with External Sink Current @ $500\ \mu\text{A}$   | 6 | $V_{CT\_max2}$  | –   | 4.2 | –   | V             |
| Internal Current Source @ $V_{CT} = 2.5\text{ V}$ (Note 9)  | 6 | $I_{CT}$        | 450 | 500 | 700 | $\mu\text{A}$ |
| Discharge time for Ct capacitor @ $C_t = 2.7\text{ nF}$ when applying falling edge on Sync pin to ( $V_{ctmin} * 1.05$ ) (Figure 7) | 6 | $T_{CT\_disch}$ | –   | 230 | 500 | ns            |

## Undervoltage Lockout

|                   |    |          |     |     |     |   |
|-------------------|----|----------|-----|-----|-----|---|
| Startup Threshold | 12 | $V_{TH}$ | 4.8 | 5.3 | 6.0 | V |
| Hysteresis        | 12 | Hyste    | –   | 0.5 | –   | V |

## IC Current Consumption

|   |    |             |   |     |     |    |
|---|----|-------------|---|-----|-----|----|
| Power Supply Current in Standby Mode<br>$V_{CC} = 12\text{ V}$ , STBY = GND, EN1 = EN2 = OPEN (Note 11) | 12 | $I_{stdby}$ | – | 2.2 | 3.0 | mA |
| Power Supply Current in Working Mode<br>$V_{CC} = 12\text{ V}$ , STBY = EN1 = EN2 = OPEN                | 12 | $I_{CC}$    | – | 17  | 22  | mA |

8. See characterization curves for Voltage Reference vs. Temperature.

9. See characterization curve for Charging Current vs.  $V_{CC}$ .

10. When the  $V_{CC} < UVLO$  level, the outputs are automatically disabled.

11. During the standby mode the outputs drivers are disabled but the shunt regulator is kept fully functional in order to supply the primary feedback.

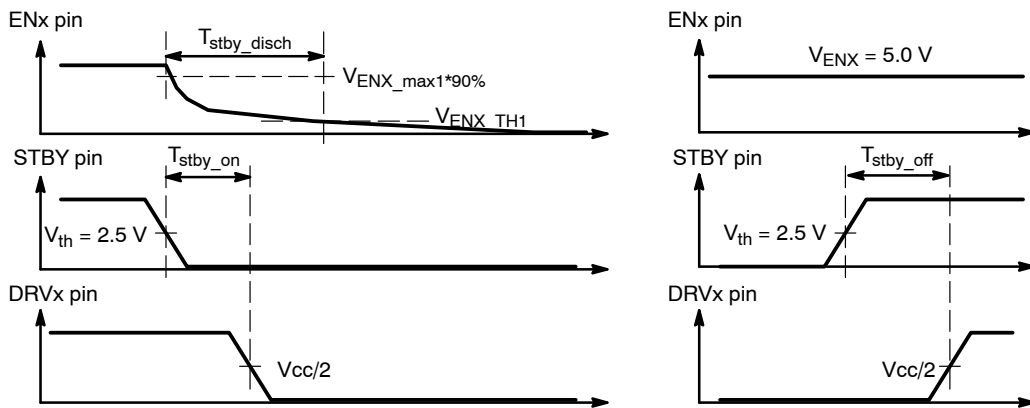


Figure 4. Standby Propagation Delay Definition

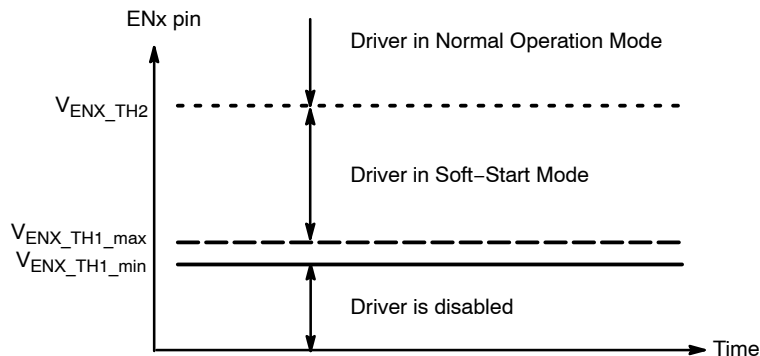


Figure 5. Enable Threshold Definition

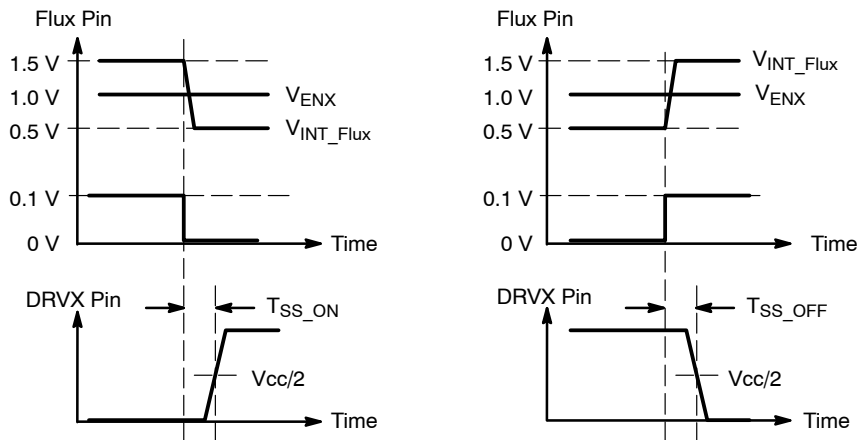


Figure 6. T<sub>SS\_ON</sub> and T<sub>SS\_OFF</sub> Propagation Delay Definition (in Soft-Start Mode Operation)

# NCP4326

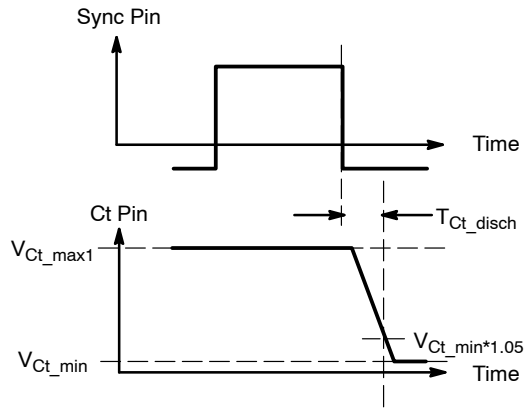


Figure 7. Discharging Time Definition (Ct Pin)

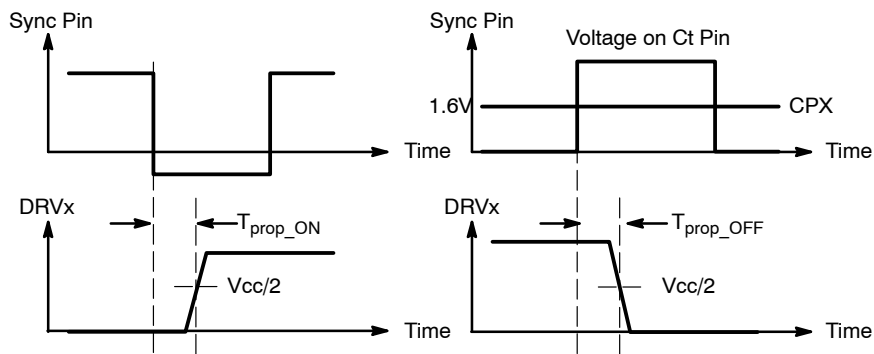


Figure 8.  $T_{prop\_ON}$  and  $T_{prop\_OFF}$  Propagation Delay Definition (in Normal Mode Operation)

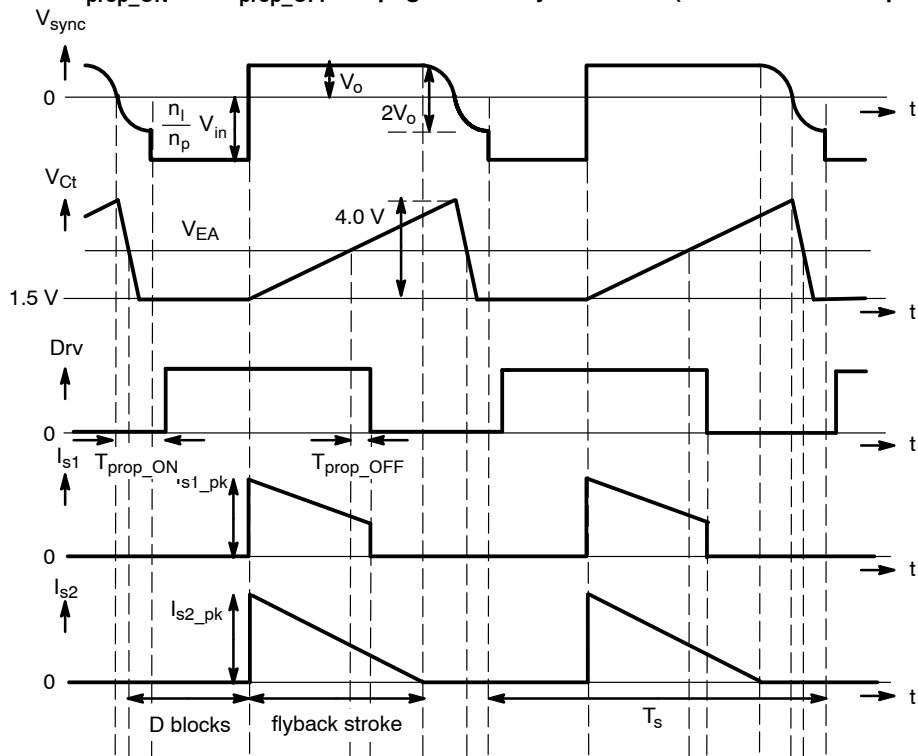
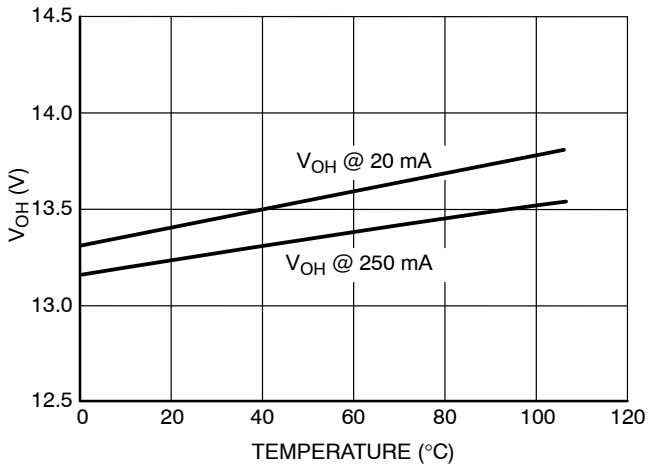
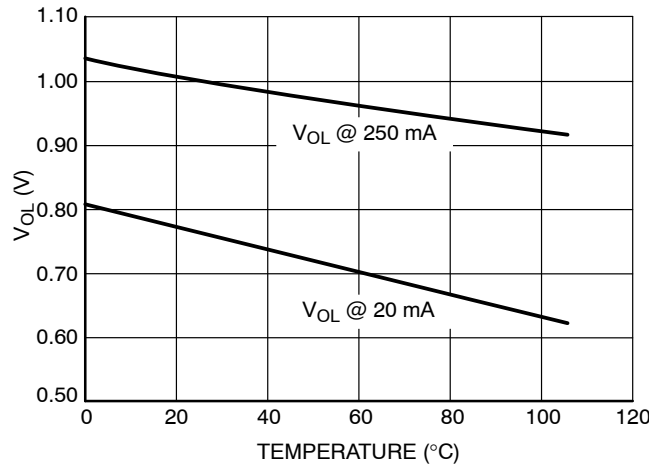


Figure 9.  $T_{prop\_ON}$  and  $T_{prop\_OFF}$  Timing Position in the Timing Application Diagram (in Normal Mode Operation)

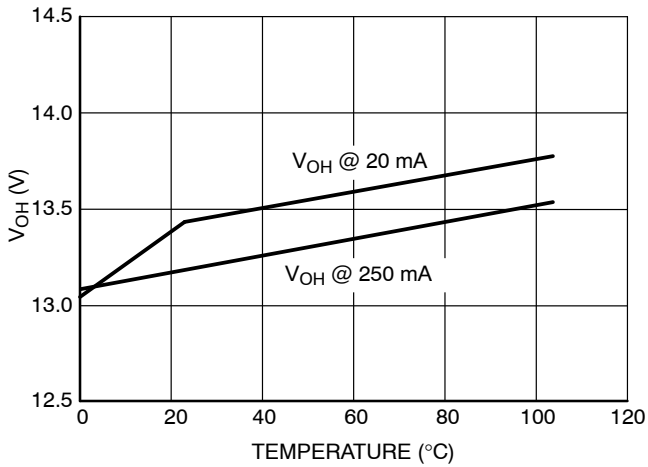
# NCP4326



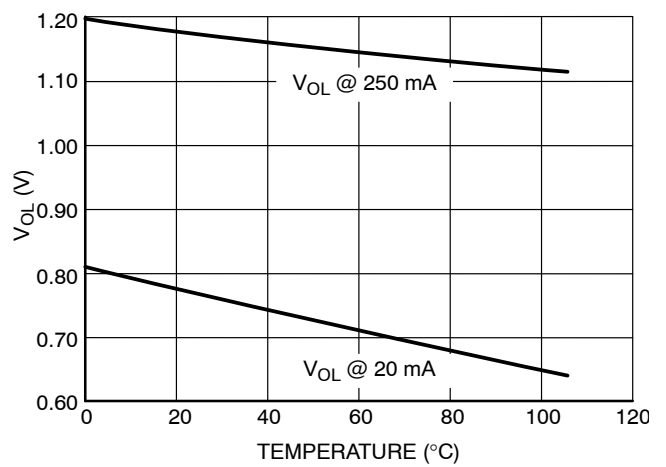
**Figure 10. Driver 1 Output Voltage High State @ V<sub>CC</sub> = 15 V vs. Temperature**



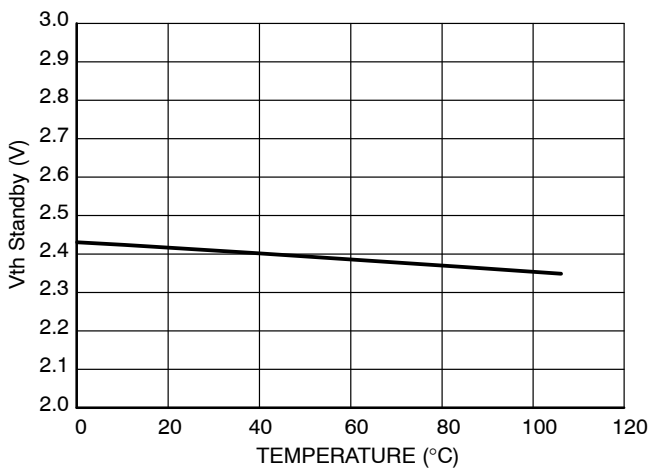
**Figure 11. Driver 1 Output Voltage Low State @ V<sub>CC</sub> = 15 V vs. Temperature**



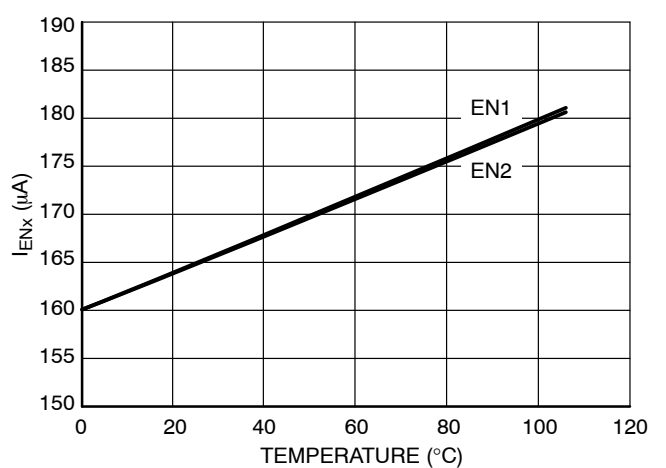
**Figure 12. Driver 2 Output Voltage High State @ V<sub>CC</sub> = 15 V vs. Temperature**



**Figure 13. Driver 2 Output Voltage Low State @ V<sub>CC</sub> = 15 V vs. Temperature**

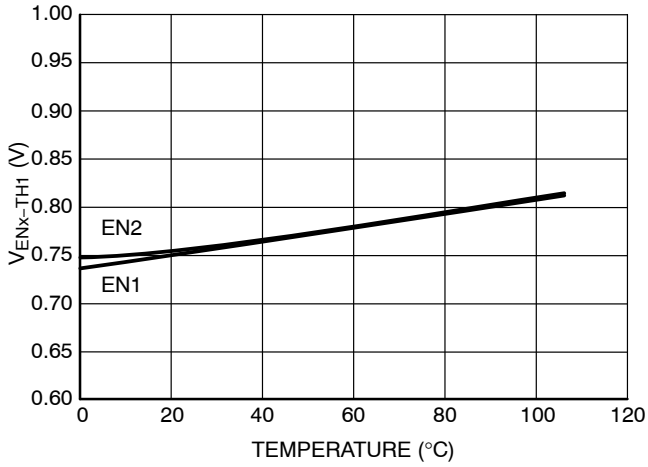


**Figure 14. Standby Pin Threshold Voltage vs. Temperature**

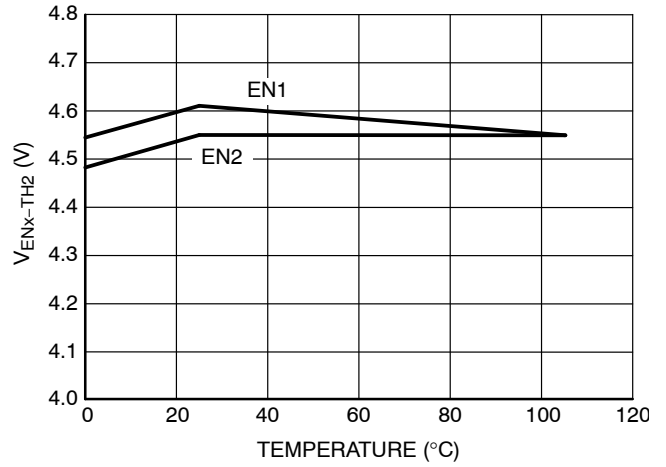


**Figure 15. Soft-Start Current Source on Enable Pin when V<sub>ENx</sub> = 2.5 V vs. Temperature**

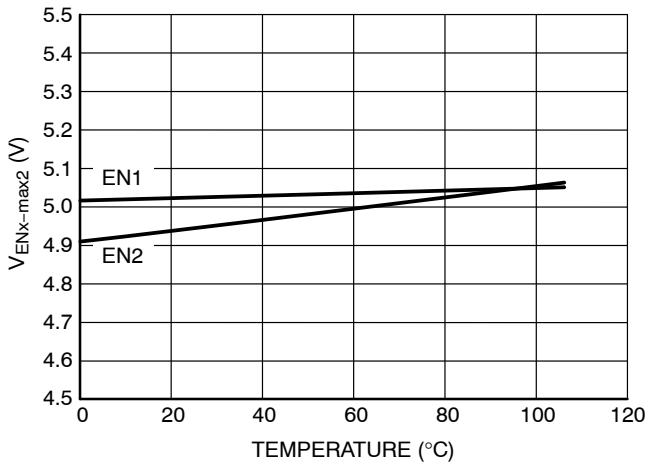
# NCP4326



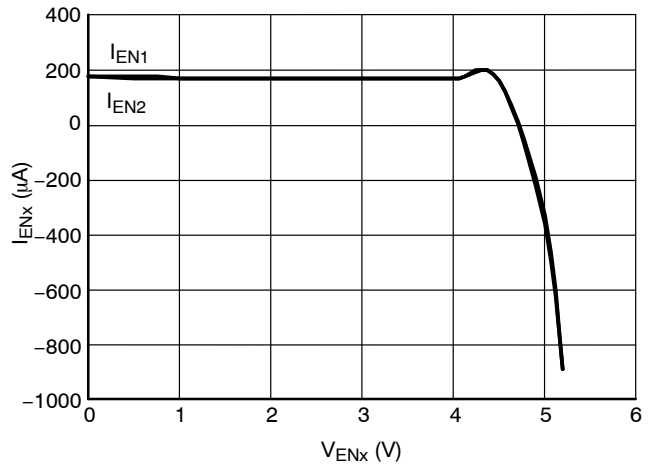
**Figure 16. Enable Soft-Start Mode or Disable Driver Mode vs. Temperature**



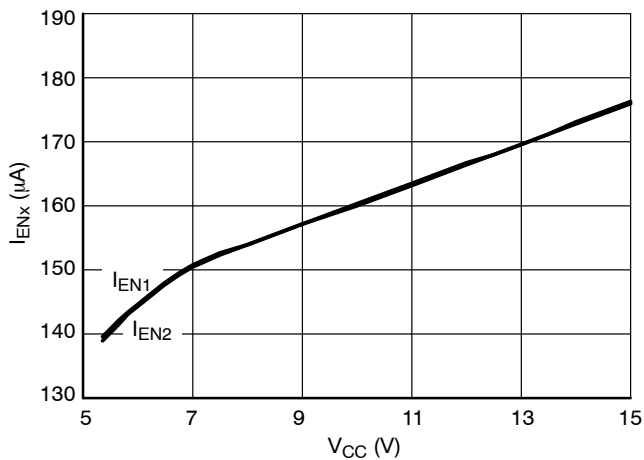
**Figure 17. Max Voltage on ENx Pin Ending Soft-Start and Enable the Regulation Mode vs. Temperature**



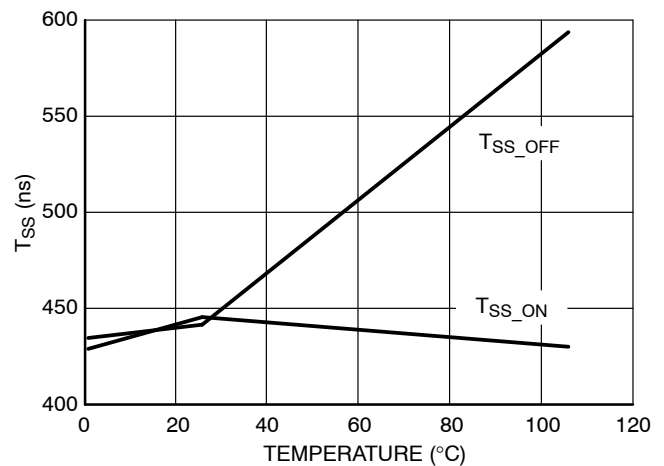
**Figure 18. Voltage on ENx Pin with an External Current Sink @ 500  $\mu$ A vs. Temperature**



**Figure 19. Soft-Start Current Source on Enable Pin vs.  $V_{EN}$**

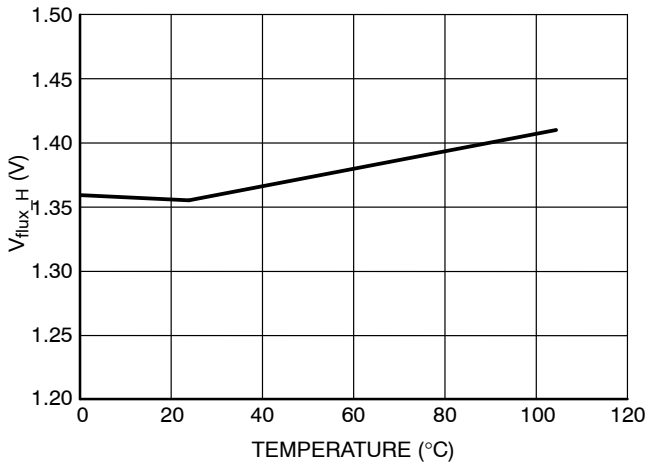


**Figure 20. Soft-Start Current Source on Enable Pin vs.  $V_{CC}$**

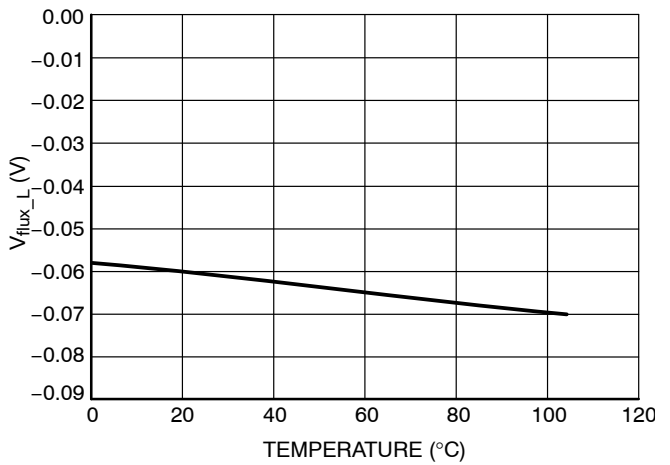


**Figure 21. Turn ON and OFF Propagation Delay in Soft-Start Mode vs. Temperature**

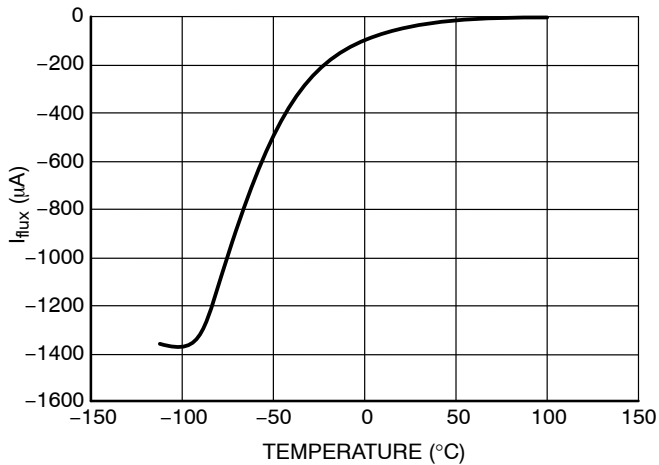
# NCP4326



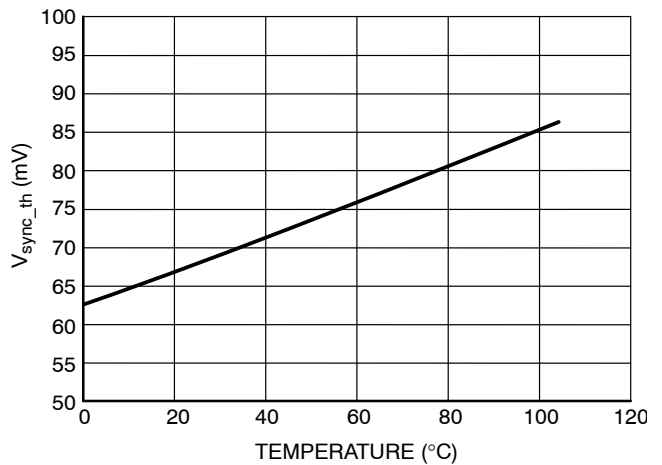
**Figure 22. High Level Flux Pin Clamp Voltage vs. Temperature**



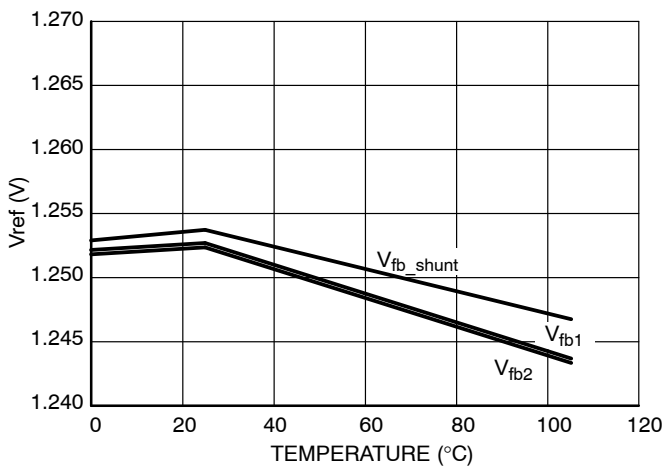
**Figure 23. Low Level Flux Pin Clamp Voltage vs. Temperature**



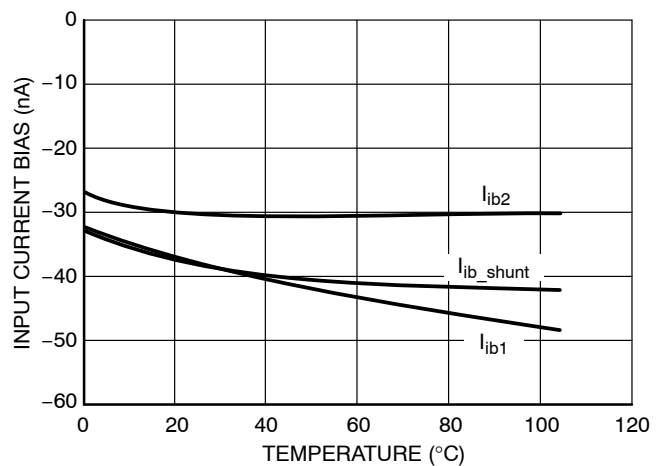
**Figure 24. Flux Pin Internal Current Source vs. Flux Voltage**



**Figure 25. Synchronization Input Voltage Threshold vs. Temperature**



**Figure 26. Error Amplifier Internal Voltage Reference vs. Temperature**



**Figure 27. Error Amplifier Input Bias Current vs. Temperature**

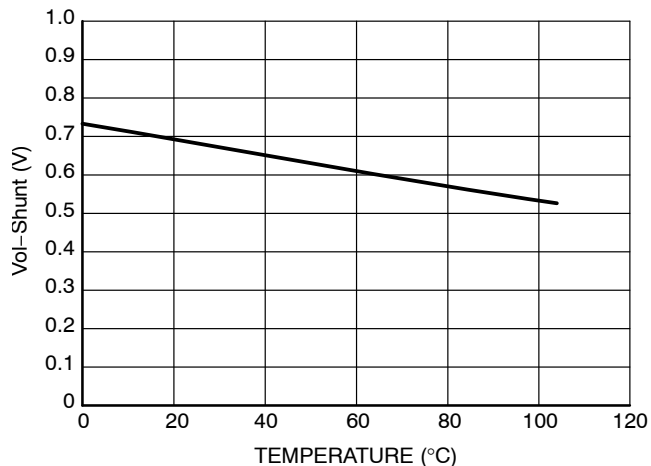


Figure 28. Error Amplifier Shunt Regulator Output Voltage Swing vs. Temperature

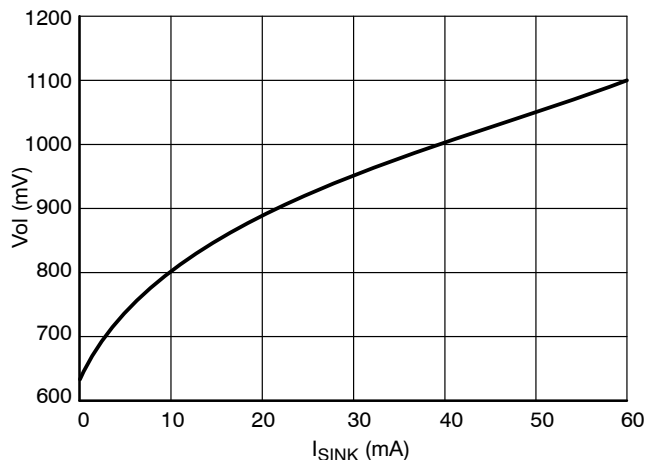


Figure 29. Error Amplifier Shunt Regulator Output Voltage Swing vs. Output Current (I<sub>SINK</sub>)

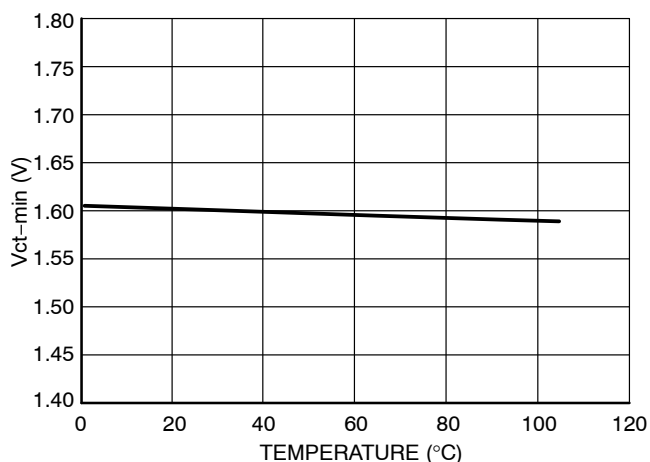


Figure 30. Minimum Voltage Clamp on Ct Pin vs. Temperature

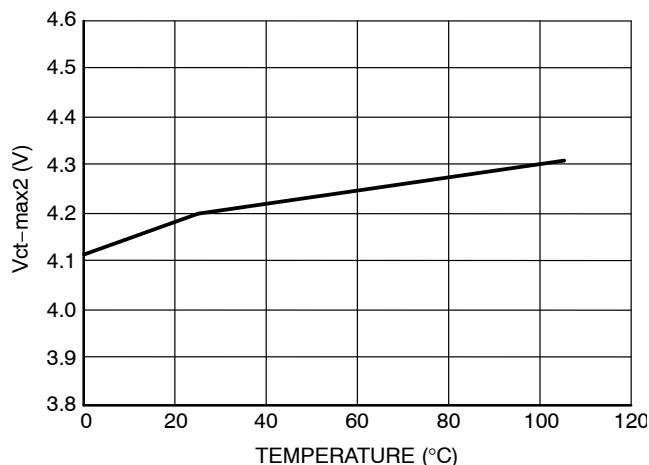


Figure 31. Maximum Voltage Clamp on Ct Pin @ 500 μA vs. Temperature

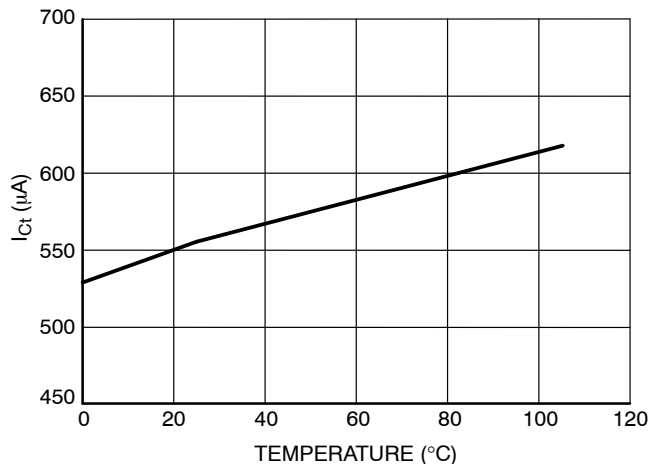


Figure 32. Internal Current Source on Ct Pin vs. Temperature

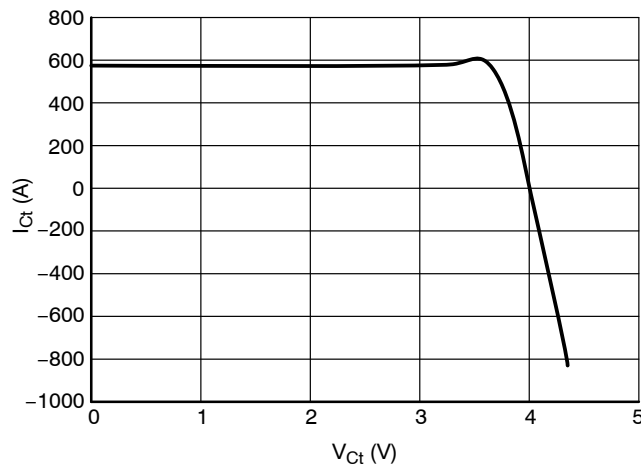
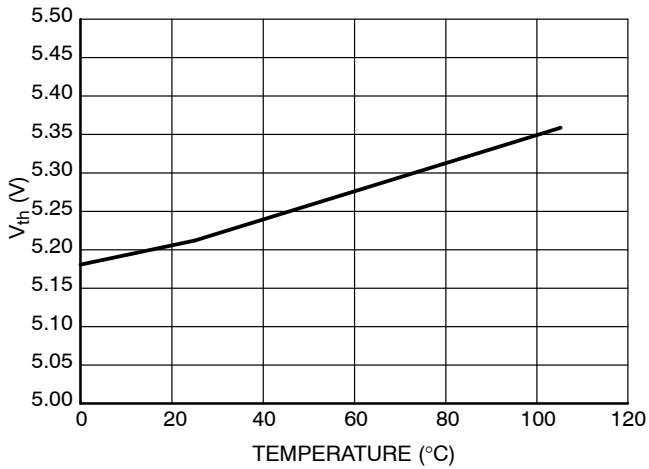


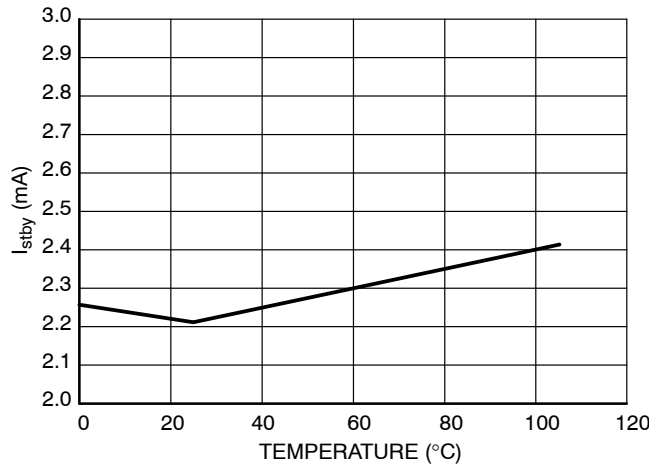
Figure 33. Internal Current Source on Ct Pin vs. V<sub>Ct</sub>



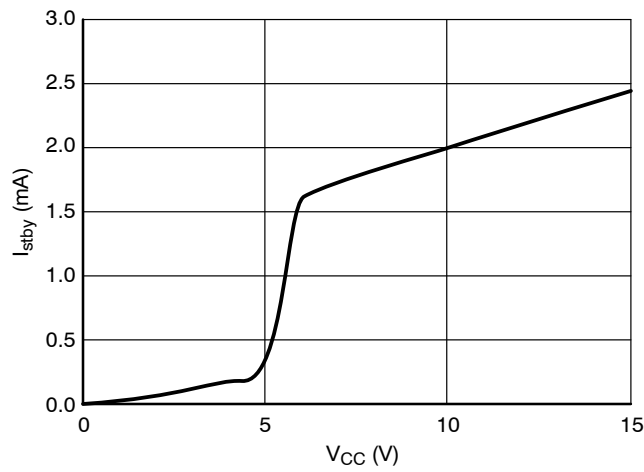
# NCP4326



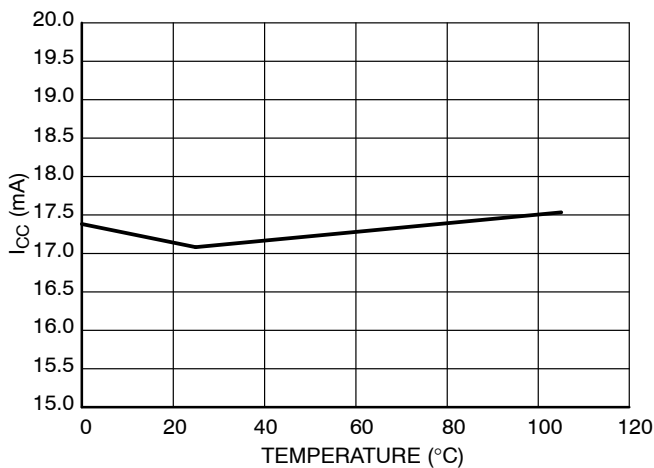
**Figure 34. Undervoltage Lockout, Startup Threshold vs. Temperature**



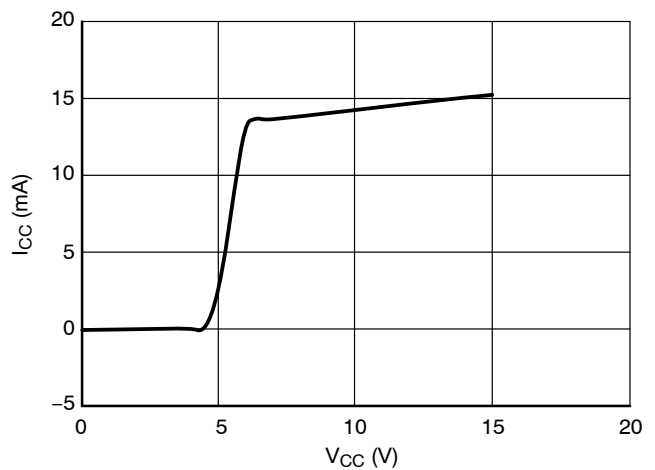
**Figure 35. Power Supply Current in Standby Mode vs. Temperature**



**Figure 36. Power Supply Current in Standby Mode vs. Power Supply Voltage – V<sub>CC</sub>**



**Figure 37. Power Supply Current in Working Mode vs. Temperature**



**Figure 38. Power Supply Current in Working Mode vs. Power Supply Voltage – V<sub>CC</sub>**

APPLICATION INFORMATION

Introduction

The NCP4326 is designed to regulate voltages in multiple output power supplies running in borderline or critical conduction mode. It controls two independent switches to precisely adjust two separate secondary outputs.

A precision reference voltage is integrated together with a dedicated operational amplifier to reduce the feedback loop elements to the minimum. A skip cycle feature improves the standby power in light load condition. A dedicated shutdown pin offers an easy mean to disable the secondary outputs.

Regulation Principle

The NCP4326 can handle up to three independent outputs: it provides the feedback for the main output, and can also regulate two others secondary outputs.

The secondary outputs behave as a buck converter:

- The voltage is supplied via a secondary winding voltage
- The switch, inserted in series with the flyback diode, is controlled by the NCP4326.

Q1 On time:

- Q2 is switched ON but no current flows through Q2 due to diode D2 polarized in reverse.

Q1 Off time:

- Q2 is still ON and the energy is delivered to the load.
- Q2 MOSFET is kept ON till the secondary output reaches the set point.

Mosfet Q2 is switch OFF until a new cycle begins.

Figure 39 illustrates the regulation principle with only one secondary output regulated by the NCP4326, but it can regulate independently another one output, that is to say 3 independent outputs.

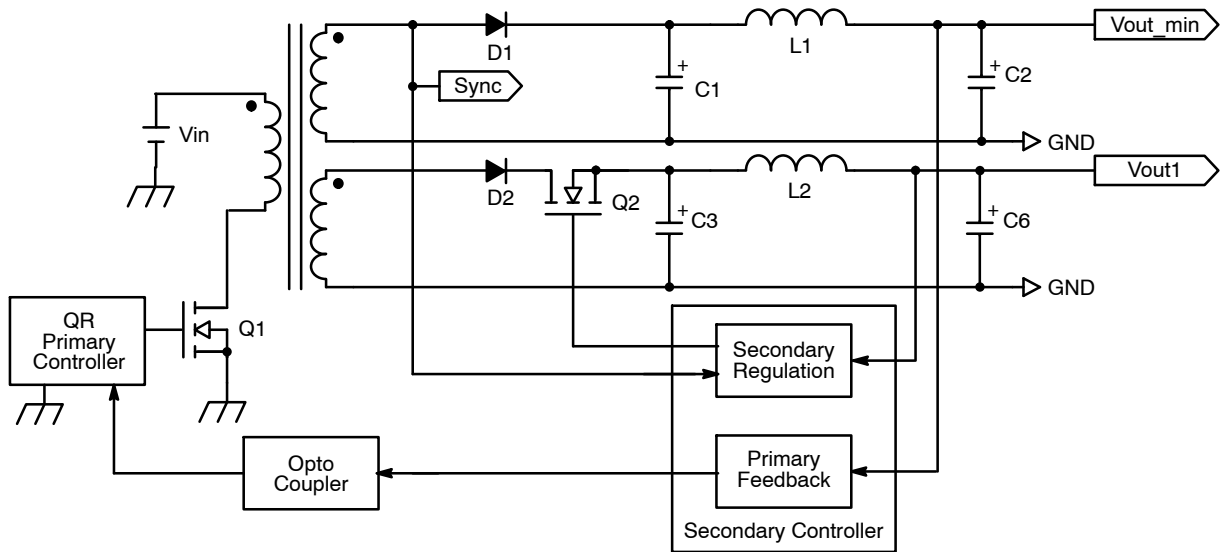


Figure 39. Regulation Principle Schematic

**Detailed Regulation Principle**

At the beginning of the  $T_{on}$  period the capacitor connected on Ct pin is discharged and the internal current source is shunted to  $V_{CT\_min}$  (1.6 V) via the bipolar transistor until the end of the  $T_{on}$  period.

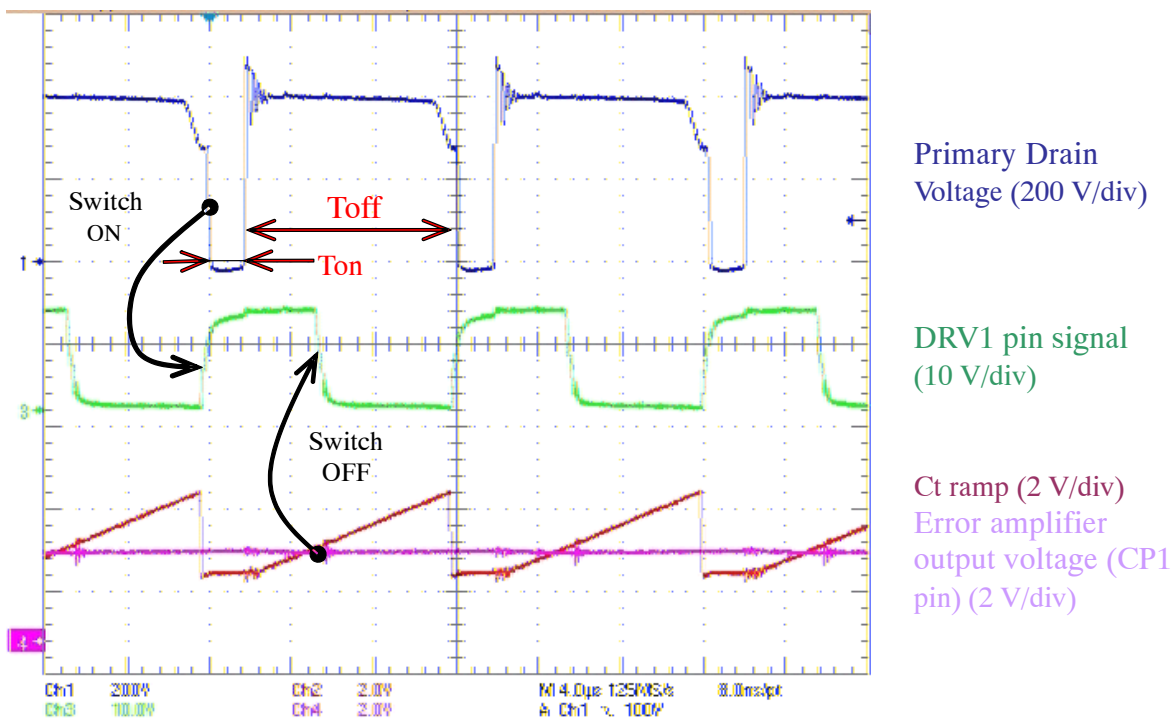
The internal current source starts to charge the capacitor connected on Ct pin at the beginning of the  $T_{off}$  period. As long as the voltage on the Ct pin is below the CPX pin, the secondary switch is kept ON (i.e.: The secondary switch is turned ON at the beginning of the primary on-time). By this method the secondary power MOSFET can only be switched ON one time per  $T_{off}$  period and prevents from any hysteretic switching to the secondary side. The secondary switch is synchronized with the primary switching frequency, the secondary controller sets only the duty cycle.

The Ct capacitor value determines only the voltage swing present at the Ct pin, which it used to generate the secondary duty cycle.

The secondary regulation is working in trailing edge mode control. The trailing edge mode control has been preferred for its superior cross load performance.

The following picture (Figure 40) shows only one output regulation, but the second output regulation works similarly and independently from the other one. Nevertheless, both regulations use the same synchronization signal:

- Beginning of ON time period (switch ON of the secondary mosfet)
- The same ramp on Ct pin for adjusting in respect to the error amplifier level the secondary duty-cycle to the both outputs drives.

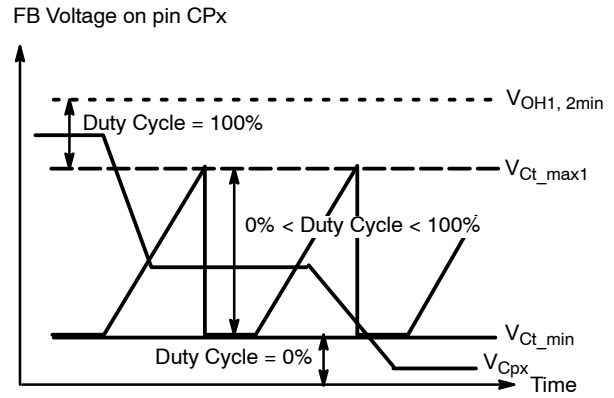


**Figure 40. Detailed Principle Regulation**

**Duty Cycle Control:**

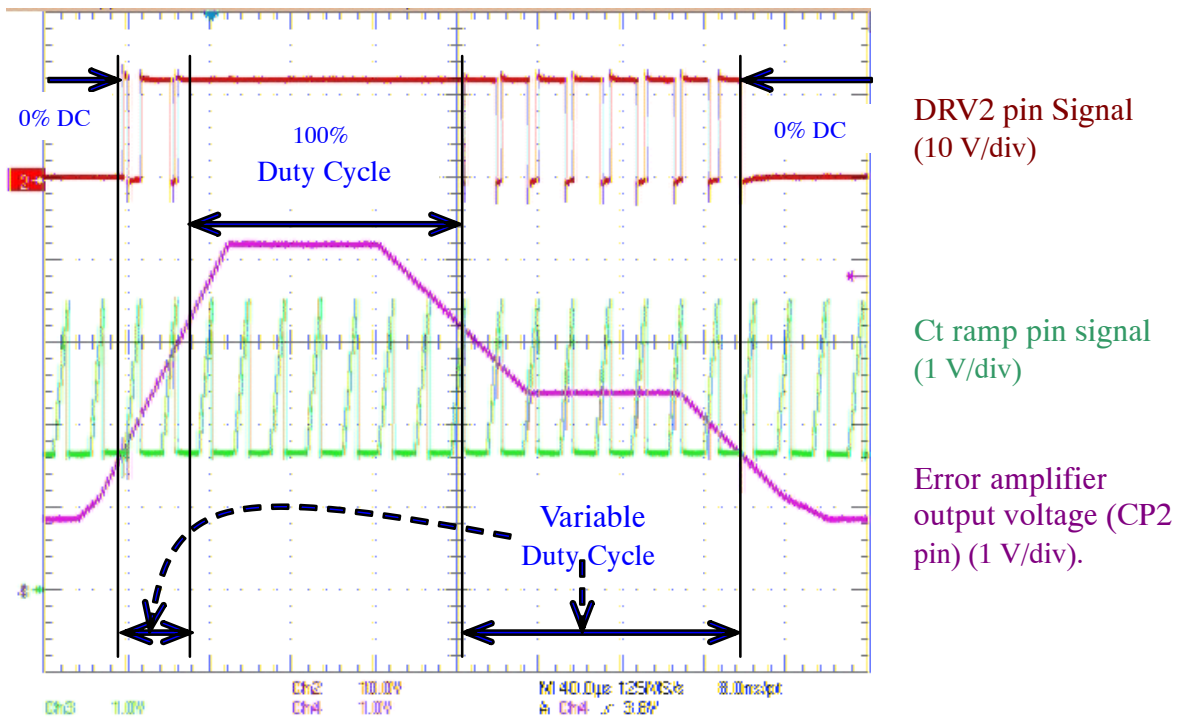
Figure 41 shows the duty cycle value according the opamp output voltage (CPx pin):

1. If the opamp output ( $V_{CPx}$ ) is above the maximum ramp value ( $V_{Ct\_max1}$ ) on "Ct" pin then the duty cycle will be equal to 100%.
2. If  $V_{CPx}$  is between the max and the min value of the ramp voltage, respectively  $V_{Ct\_max1}$  and  $V_{Ct\_min1}$  then the duty cycle will be included between 0 and 100%.
3. If  $V_{CPx}$  is below the min ramp value ( $V_{Ct\_min1}$ ) then the output driver will be place in skip cycle mode with a null duty cycle.



**Figure 41. Duty Cycle Variation versus the Feedback Voltage**

Here after find the experimental results illustrating the skip cycle feature:



**Figure 42. All Duty Cycle Representation**

**Detailed Soft-Start Behavior**

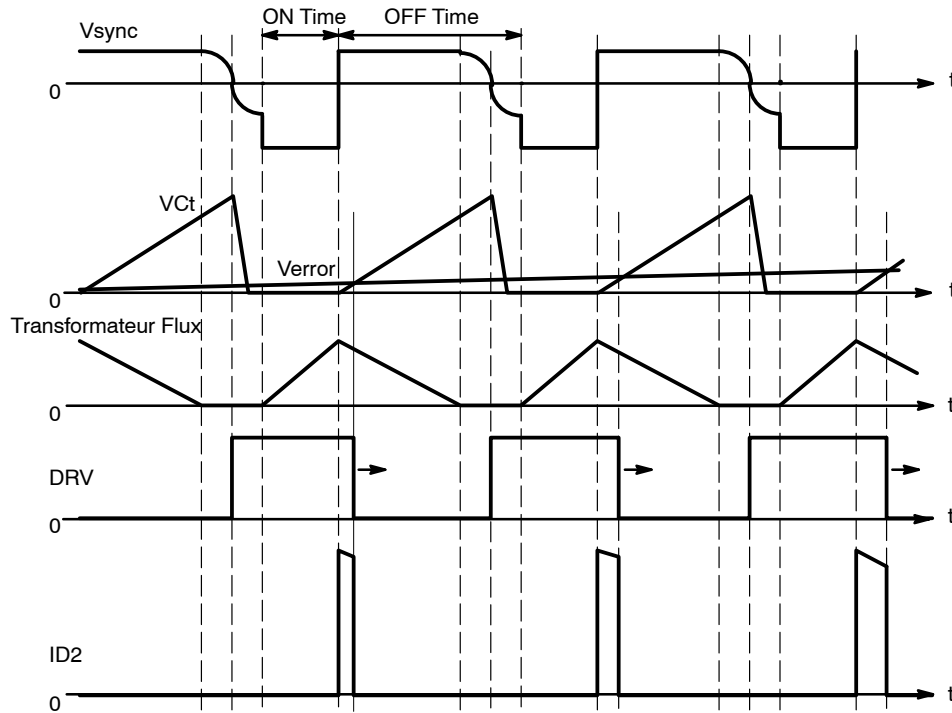
A soft-start is proposed to avoid a high peak current during startup sequences in trailing edge mode control. Increasing smoothly the secondary duty cycle from zero to the nominal value in trailing edge mode control does not limit this current (see Figure 43).

NCP4326 is a voltage mode controller type (i.e. the secondary peak current is not sensed); the peak current sensing can not be used to ensure a proper peak current ramp up on secondary side.

Instead of controlling the peak current ramp up, if the secondary controller smoothly ramps up the duty cycle then

the result will not yield a smooth ramp up peak current as in conventional PWM controllers (see Figure 43).

As depicted in Figure 43, when the secondary duty cycle is increased smoothly the peak current does not ramp up. It is not possible to have a ramp up peak current because at the beginning of the OFF time period the flux stored in the flyback transformer is at the maximum value so the peak current yields by this flux will be also at a maximum value. Consequently, the peak current is not linked to the duty cycle width. The peak current is only linked to the energy stored in the flyback transformer and the current sharing during the primary OFF time.



**Figure 43. Increasing Smoothly the Duty Cycle Does Not Yield a Smooth Peak Current Ramp up**

The new patented soft-start is based on the flux transformer reconstruction concept with leading edge mode control during a startup sequence only.

A startup sequence can be arisen with the 3 following cases:

1. The power supply unit is just plug on the main supply, in this case there is a general startup.
2. The power supply unit is running but one or the both outputs are disabled, thus by enabling the output a new startup happened.
3. The power supply unit is running but the secondary controller is in standby mode (STBY pin grounded), when the standby mode is left, a startup sequence happen if at least one of the outputs is enable.

The idea of this soft-start is to reconstruct the flux image inside the flyback transformer, and to compare this image with a slow ramp up voltage on enable pin, to generate a smooth increasing duty cycle in leading edge mode. The leading edge mode control guarantees that the peak current ramps up smoothly. Because the secondary duty cycle finishes at the OFF-time end and starts just before.

At the end of the off time period and due to the primary controller running in critical conduction mode; the flux in the transformer is null, so the peak will start from zero to reach the nominal value.

Figure 44 illustrates the driver synchronization in soft-start sequence.

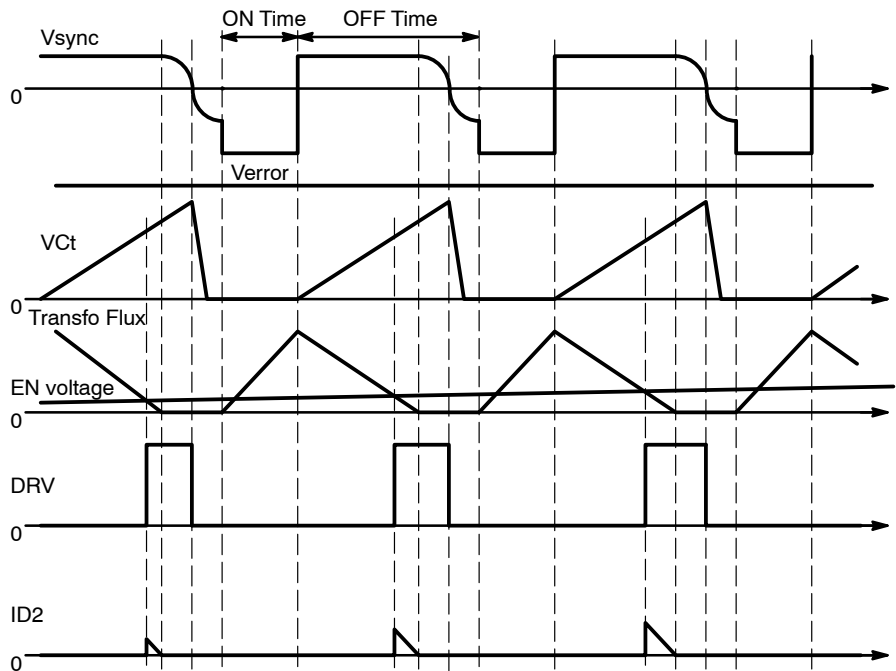


Figure 44. Startup Sequence Illustrating the Leading Edge Mode Control

Due to the internal current source and the external capacitor connected on enable pin (EN1 and EN2 pin); a voltage ramp is generated that it fixes the soft-start time; by

playing with the capacitor value the soft-start time can be adjusted to fit the application startup time.

**How Does the Enable Pin Work?**

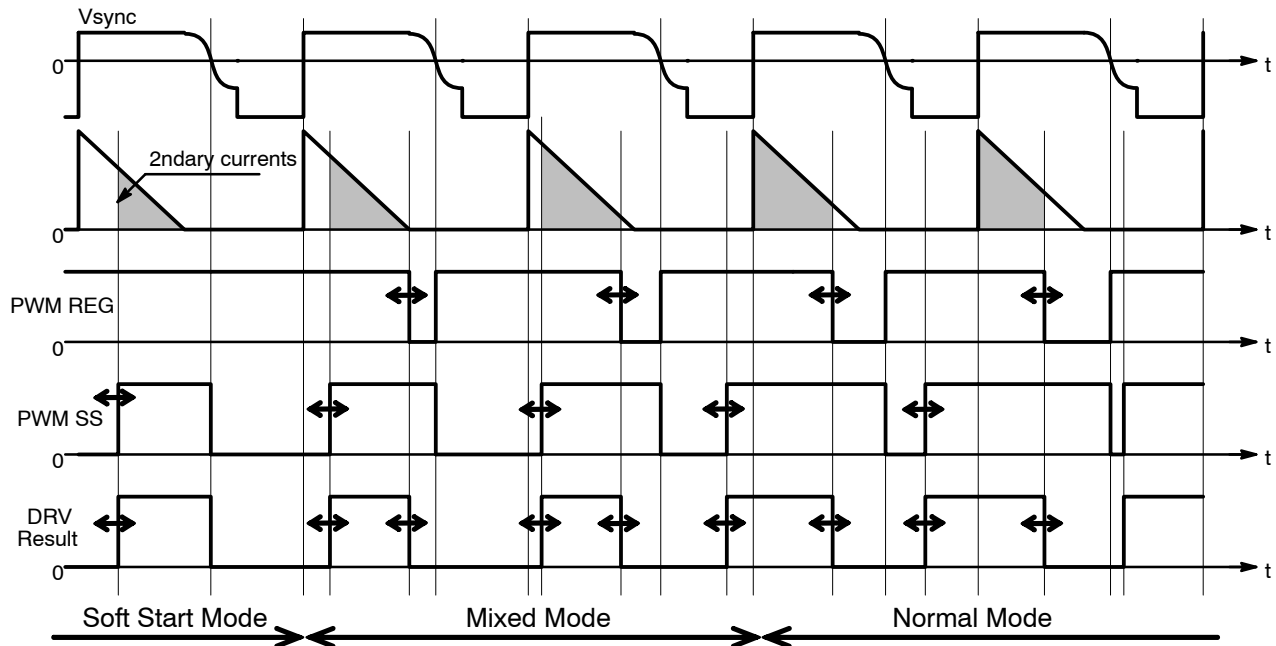
The enable pin cumulates two functions; it enables/disables the driver and it generates the soft-start time in leading edge mode control in order to control the ramp up peak current during a startup sequence.

According the enable pin voltage level ( $V_{ENX}$ ) there are three modes:

1. DISABLE MODE: when  $V_{ENX} < V_{ENX\_TH1}$
2. SOFT-START MODE;  
when  $V_{ENX\_TH1} < V_{ENX} < V_{ENX\_TH2}$
3. ENABLE MODE (or NORMAL OPERATION):  
when  $V_{ENX} > V_{ENX\_TH2}$

At the end of the soft-start mode (duration fixed by the capacitor connected to enable pin) if the output voltage is not entered in regulation then the duty cycle is fixed to 100% until the output reaches the regulation.

If the soft-start mode takes a longer time than the time needed to reach the regulation level, the controller enters in a mixed mode. During the mixed mode the duty cycle is a mixed of the soft-start mode duty cycle generation and the duty cycle from the normal regulation. Thus the transition from the soft-start mode and the normal operation is done smoothly without discontinuity on the duty cycle (see Figure 45).



**Figure 45. End of Startup Sequence Illustrating the Smooth Transition from Soft-Start to Normal Mode via the Mixed Mode**

**Flux Image Reconstruction**

With a primary controller working in critical conduction mode the core flux inside the transformer is null at each beginning primary switching cycle.

Measuring the flux means integrating the voltage present on a transformer winding. But a simple integration yields a saw tooth voltage waveform centered to zero volts. Thus this saw tooth represents the flux variation in the transformer core and must be offset in order to have a true image of the flux with a minimum voltage close to zero volts.

What we need is a triangle with a FIXED lower level, being equal to or somewhat above zero. This necessitates the resetting of the integrator at the beginning of each primary on-time. In practice, it means we quickly discharge the integrator capacitor just before the primary on-time and release this capacitor at the start of the primary on-time.

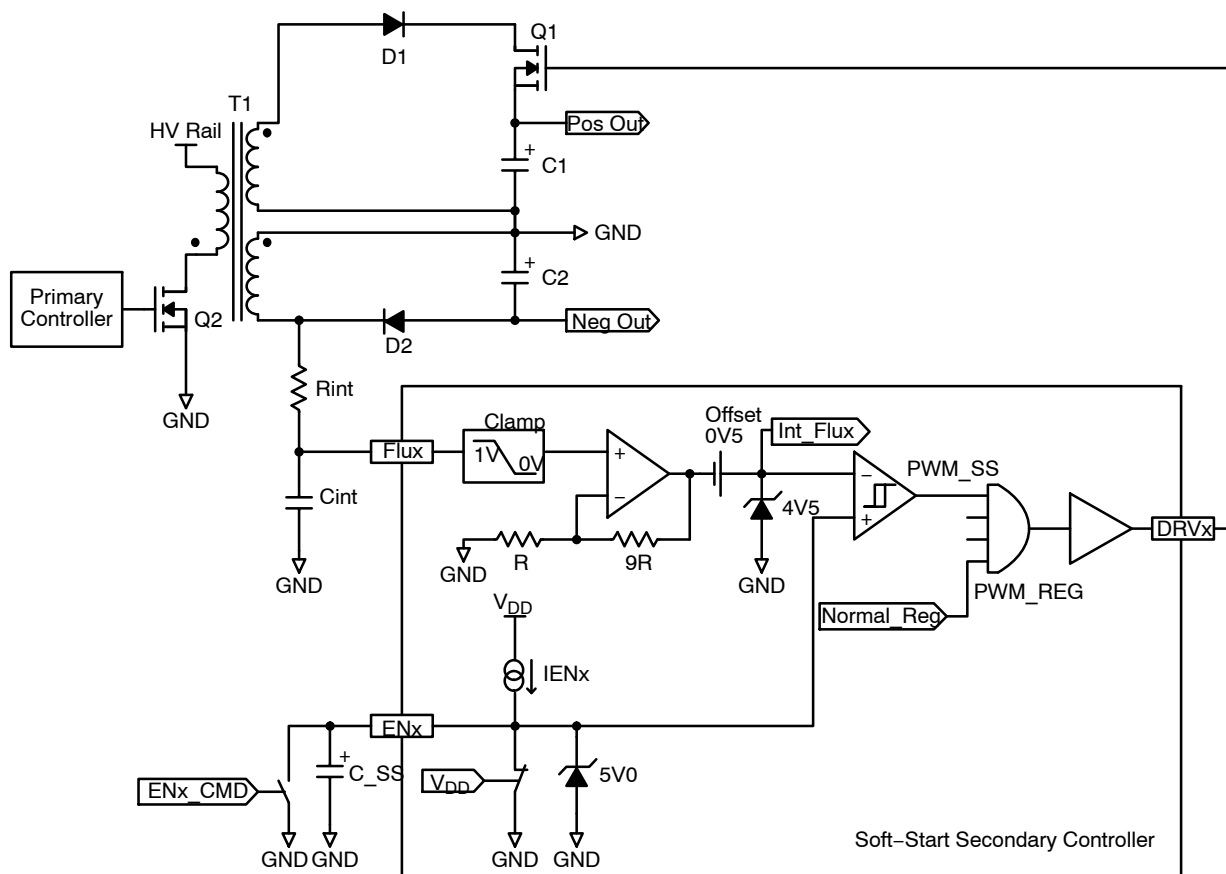
A negative auxiliary winding or a forward winding can be used to build the flux image via a simple RC network, which it ensures the integration then the NCP4326 fixes the lower level.

Figure 46 shows how the flux image is built and used for the soft-start sequence.

The RC network (Rint & Cint) connected to the negative output winding does the integration of the voltage present on this winding that it yields the flux image. Then the voltage available on Flux pin is clamped between a low and high level (respectively  $V_{Flux\_L}$  and  $V_{Flux\_H}$ ) in order to ensure a positive saw tooth on Flux pin. After that the voltage on Flux pin is amplified 10 times and an offset is inserted to ensure the disable function when the enable pin is below  $V_{ENX\_TH1}$ . More over the internal voltage clamp ( $V_{ENX\_TH2} = 4.5\text{ V}$ ) ending the soft-start duty cycle generation when the voltage on enable pin is between  $V_{ENX\_TH2}$  and  $V_{ENX\_max1}$ .

Next the internal Flux image (label Int\_Flux on Figure 46) is compared with the enable pin voltage for generating the soft-start duty cycle in leading edge mode control.

On enable pin we have an internal current source that it charge the external capacitor and fix the soft-start time by playing with the capacitor value. If the controller is placed in standby mode then the enable capacitor is discharged by the internal switch. The internal clamp limits the voltage range on the enable pin.



**Figure 46. Soft-Start Detailed Schematic View**



# NCP4326

Soft-start experimental results are illustrated by the Figure 47.

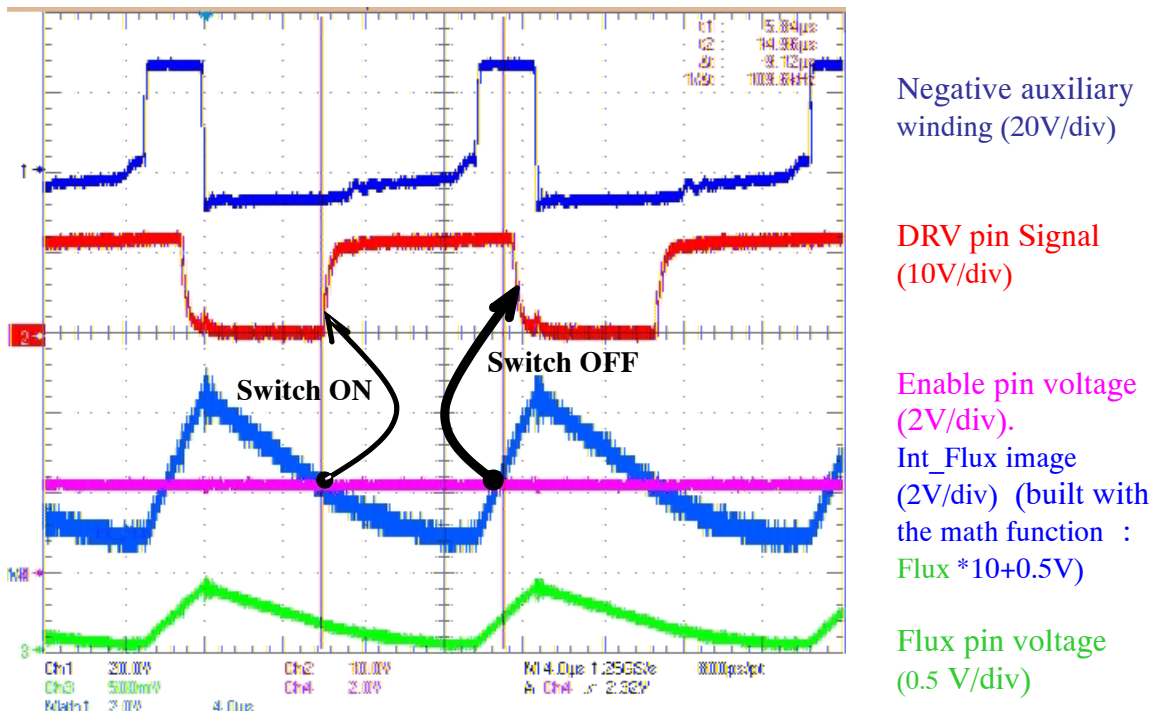


Figure 47. Soft-Start Duty Cycle Generation During the Startup Sequence

## NCP4326

In a startup sequence, the voltage output is null so the error amplifier output is at its max value, so the duty cycle from the PWM\_reg signal is at 100% duty cycle. The duty cycle is only limited by the soft-start feature: the switch ON is done when the Int\_Flux voltage is become lower than the enable pin voltage and the switch OFF is done when the Int\_Flux is become higher than the enable pin voltage.

The following Figure 48 show a real soft-start on a typical application. The limited peak current during the soft-start allows selecting smaller mosfet (for example SOT23 package without risk of exceeding the max non repetitive peak current "IDM").

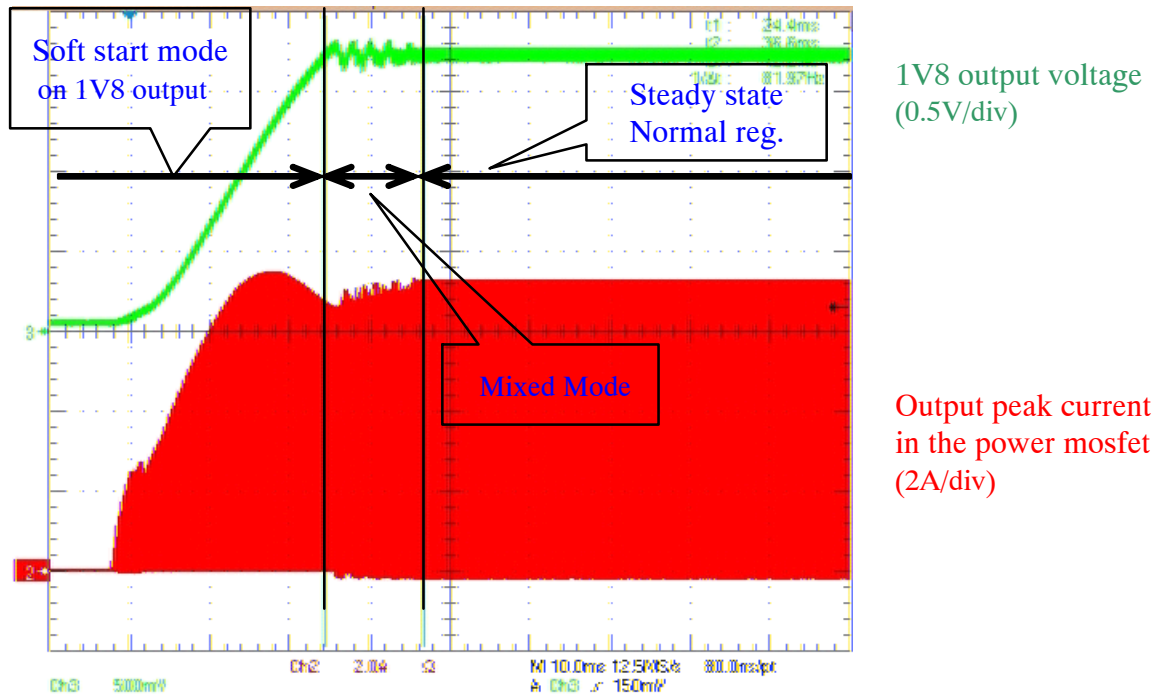


Figure 48. Startup Sequence with Soft-Start on 1V8 Output at Full Load

**Standby Pin Feature Description**

The standby pin enables or disables the controller in order to save some power when the power supply is in standby mode. In standby mode all the internal power supplies and references are shut down, except the  $V_{DD1}$  and the voltage reference connected to the shunt regulator. The shunt regulator bloc works during the standby mode for supplying the feedback to the primary controller.

When the standby pin is released the both drivers are kept in OFF state during  $T_{stby\_off}$  time to prevent any parasitic switches on the driver before the internal power ON of the controller is fully finished.

Practically the internal standby signal for the driver is delayed and in the mean time the internal power waking up is done.

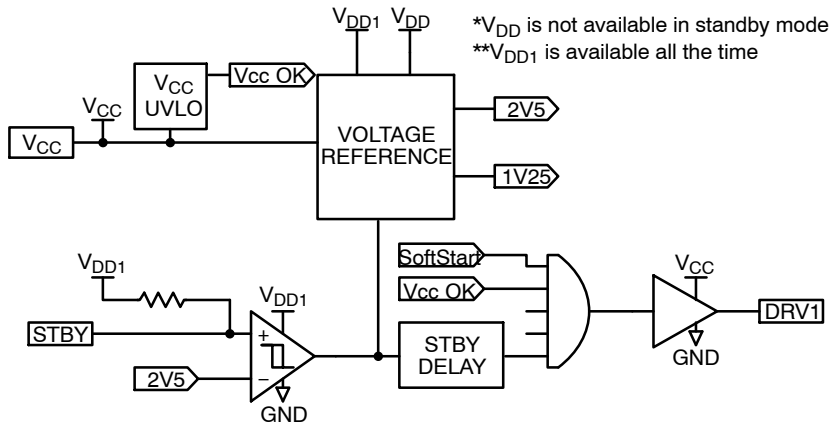


Figure 49. Standby Delay Definition

**Synchronization Pin**

The NCP4326 needs to be synchronized with the primary controller, a dedicated pin ensures this function just by sensing a secondary winding voltage and filtering it.

The RC network ( $R_{sync1}$  and  $C_{sync}$ ) filters the secondary winding and  $R_{sync2}$  limits the current through the internal zener diode when the voltage exceeds the zener clamp level or when the zener conduct in forward mode (when the voltage winding is negative).

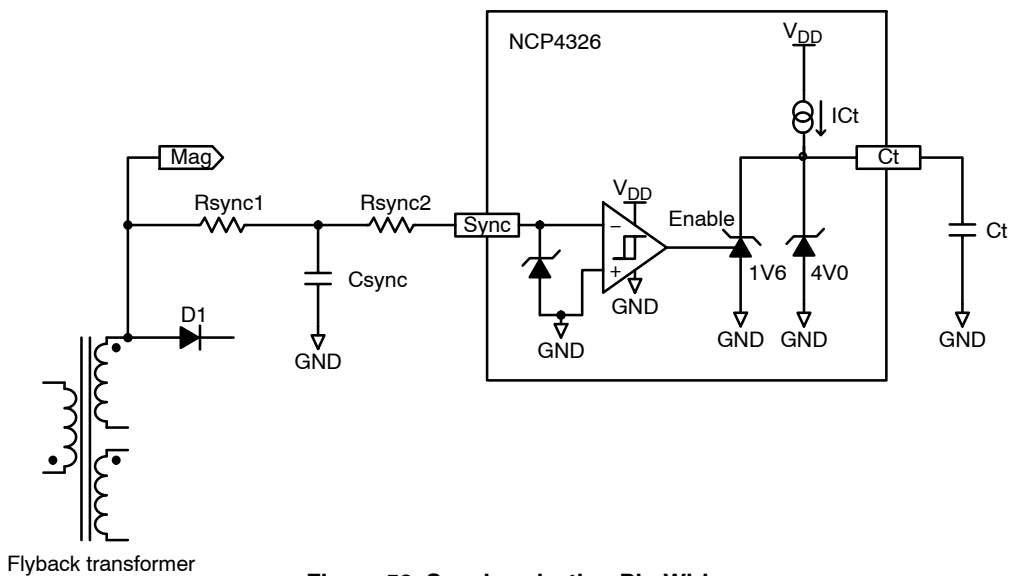
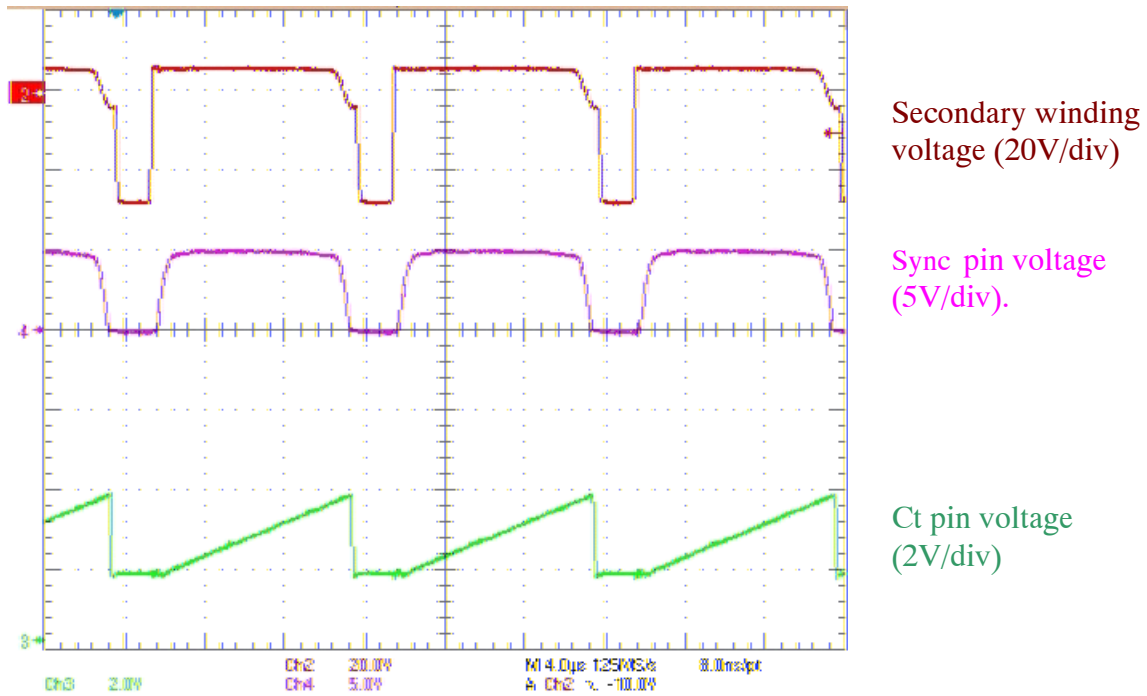


Figure 50. Synchronization Pin Wiring

# NCP4326

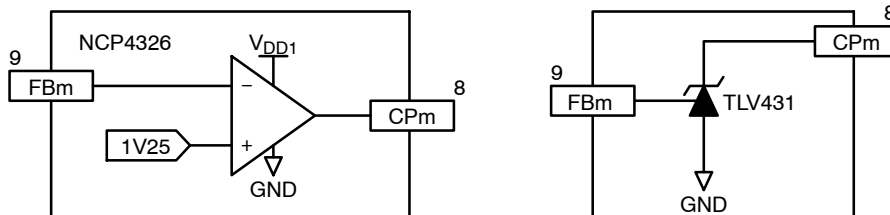


**Figure 51. Soft-Start Duty Cycle Generation During the Startup Sequence.**

During the primary on time, the secondary winding voltage is equal to the input voltage multiplied by the transformer turn ratio. At the primary switch on or the falling edge on the secondary winding voltage, the Ct capacitor voltage is reset to V<sub>Ct\_min</sub> and keeps it to this value as long as the primary switch is in ON state. Then when the primary ON time ends the Ct capacitor voltage is released, thus with the internal current source on Ct pin, the voltage capacitor rises linearly until a new primary switching cycle.

### Primary Feedback Regulation

The NCP4326 integrates a precision reference voltage, which together with a dedicated operational amplifier reduces the feedback loop elements to the minimum. This error operational amplifier with the reference voltage has called the shunt regulator and offers the same behavior of a traditional TL431 or TLV431.



**Figure 52. Equivalent Schematic of the Shunt Regulator**

## NCP4326

The operational amplifier is an open collector type that it allows to sink the current from the opto-coupler from any voltage source level.

Figure 53 illustrates an example of a close loop feedback connection from the secondary and the primary side.

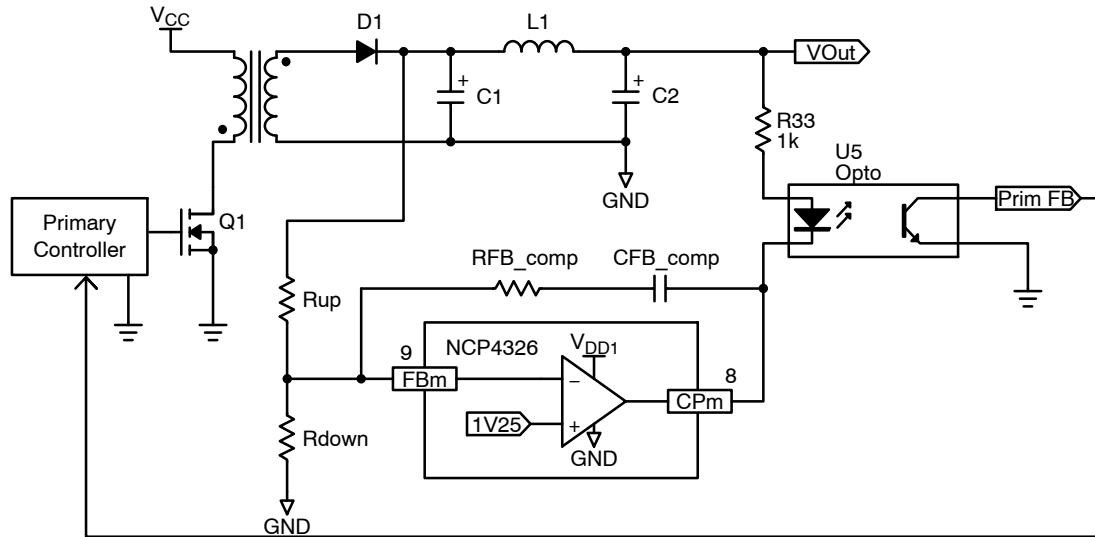


Figure 53. Primary Feedback Connection

### Components Determination

#### RC Network on Flux Pin

The flux image can be obtained with a negative output or with a forward configuration. The winding voltage integration yields the flux image inside the transformer. This integration will be done with a basic integrator.

The time constant of this integrator should be significantly large compare to the maximum primary switching period. For example the time constant can be 5–10 times larger. Thus the resistor acts like a constant current source during the period, so that the voltage across the capacitor rises and falls linearly.

The internal flux signal (Int\_Flux, see Figure 46) is clamped to 4.5 volts in order to ensure a proper disable soft-start function when the enable pin voltage is at its maximum value (5.0 V).

For achieving a proper soft-start without any action from the 4.5 V internal clamp, the maximum input voltage on flux pin must be lower or equal to:

$$\frac{V_{\text{clamp}} - V_{\text{offset}}}{\text{OpAmp\_gain}} \text{ that yields } \frac{4.5 - 0.5}{10} = 0.4 \text{ V.}$$

So  $V_{\text{flux\_pin}}$  should be lower or equal to 400 mV when the power supply is in full load condition and at low line input voltage.

Practically in case of universal input voltage range and with a maximum output power to 16 W, a 10 nF capacitor is selected and the resistor is adjusted to guaranteed a maximum voltage on the flux to 400 mV at low line input voltage. This gives a 22 k $\Omega$  resistor.

#### Ct Capacitor

This capacitor is used to create the saw tooth for achieving the pulse width modulation (PWM) for the both secondary outputs regulated by the NCP4326.

The capacitor value can be determined with the following equation:

$$I = C \frac{\Delta V}{\Delta t} \leftrightarrow C = I \frac{\Delta t}{\Delta V} \text{ where } I = I_{\text{CT}}, \Delta V = (V_{\text{CT\_max1}} - V_{\text{CT\_min}}), \Delta t = \text{primary off time (time during the capacitor is charged).}$$

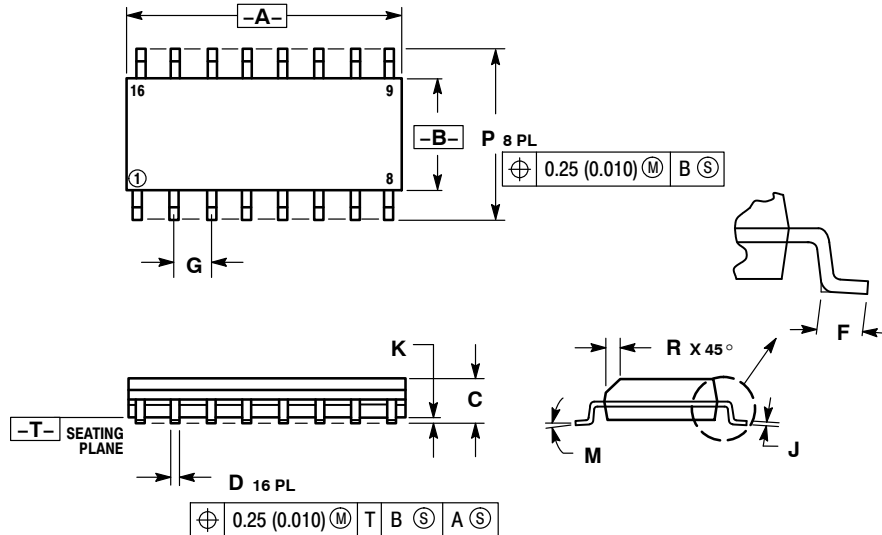
The capacitor value is calculated in the worst condition:

- $I = I_{\text{CTmax}} = 700 \mu\text{A}$
- $\Delta V = (V_{\text{CT\_max1}} - V_{\text{CT\_min}}) = 4.0 - 1.6 = 2.4 \text{ V}$
- $\Delta t = \text{maximum primary off time in worst case condition (Full load and low line input).}$

# NCP4326

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| A   | 9.80        | 10.00 | 0.386  | 0.393 |
| B   | 3.80        | 4.00  | 0.150  | 0.157 |
| C   | 1.35        | 1.75  | 0.054  | 0.068 |
| D   | 0.35        | 0.49  | 0.014  | 0.019 |
| F   | 0.40        | 1.25  | 0.016  | 0.049 |
| G   | 1.27        | BSC   | 0.050  | BSC   |
| J   | 0.19        | 0.25  | 0.008  | 0.009 |
| K   | 0.10        | 0.25  | 0.004  | 0.009 |
| M   | 0°          | 7°    | 0°     | 7°    |
| P   | 5.80        | 6.20  | 0.229  | 0.244 |
| R   | 0.25        | 0.50  | 0.010  | 0.019 |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative