NCP81143

Multiple-Phase Controller with SVID Interface for Desktop and Notebook CPU Applications

The NCP81143 Multi−Phase buck solution is optimized for Intel VR12.5 compatible CPUs with user configurations of 3/2/1 phases this controllers combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing the fastest initial response to dynamic load events at reduced system cost. They have the capability to shed to single phase during light load operation and can auto frequency scale in light load conditions while maintaining excellent transient performance.

The NCP81143 offers two internal MOSFET drivers with a single external PWM signal. High performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate digital current monitoring.

Features

- NCP81143 and Meets Intel® VR12.5 specifications
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- “Lossless” DCR Current Sensing for Current Balancing
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 200 kHz –1 MHz
- Vin range 4.5 V to 25 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- VR−RDY Output with Internal Delays
- These are Pb−Free Devices

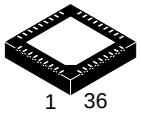
Applications

- Desktop & Notebook Processors

ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



QFN36
CASE 485CC

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

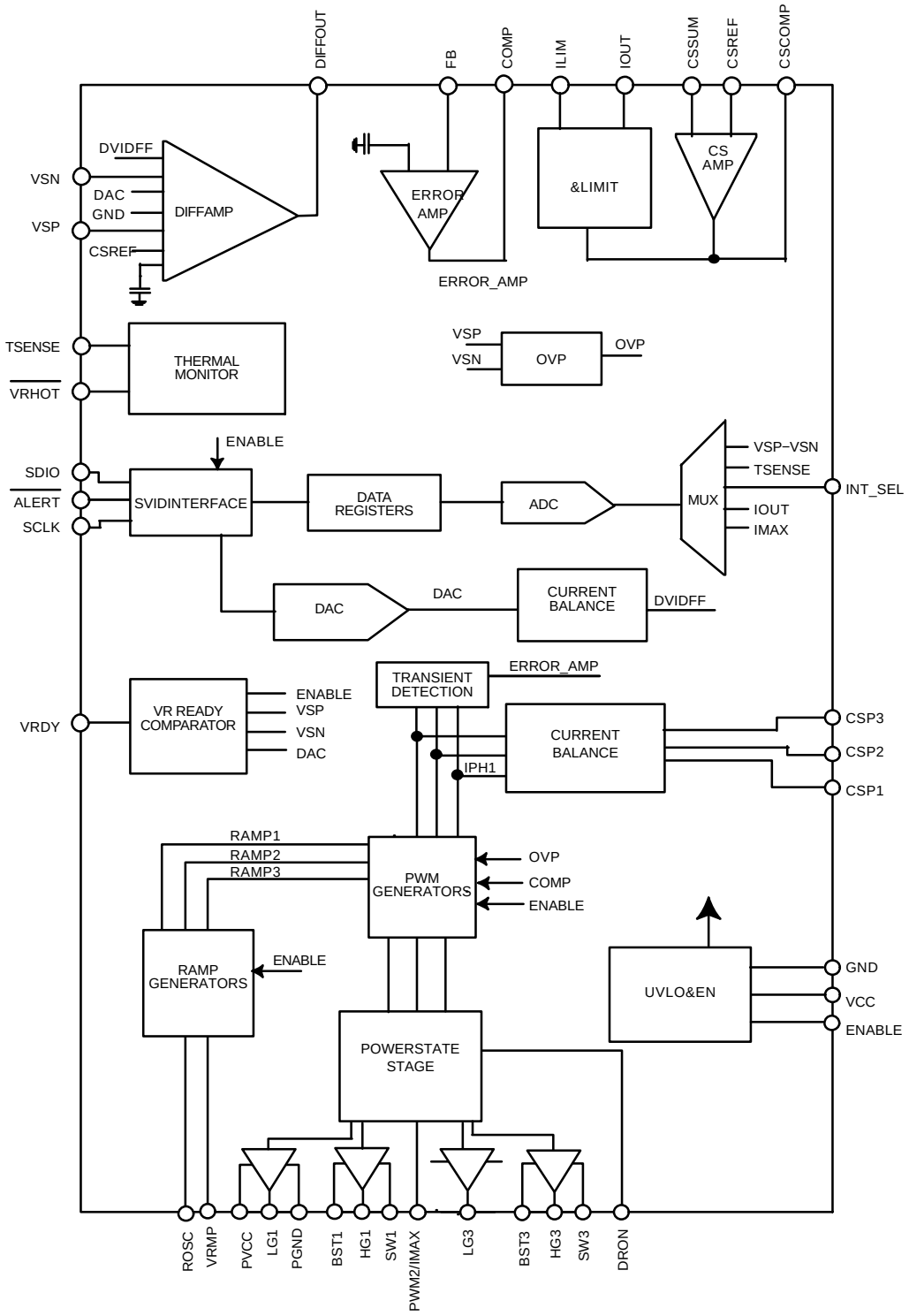


Figure 1. Block Diagram for NCP81143

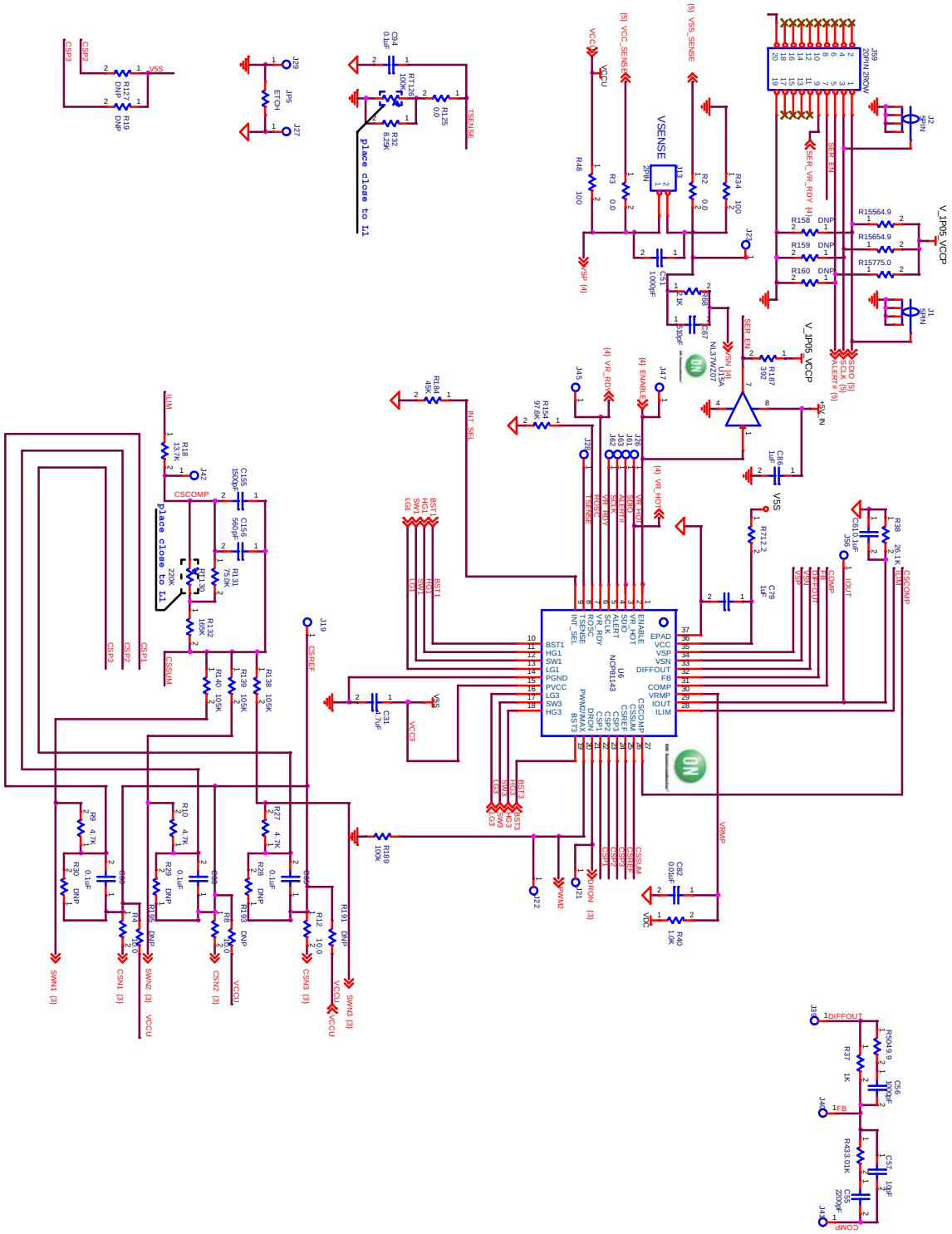


Figure 2. Reference Schematic

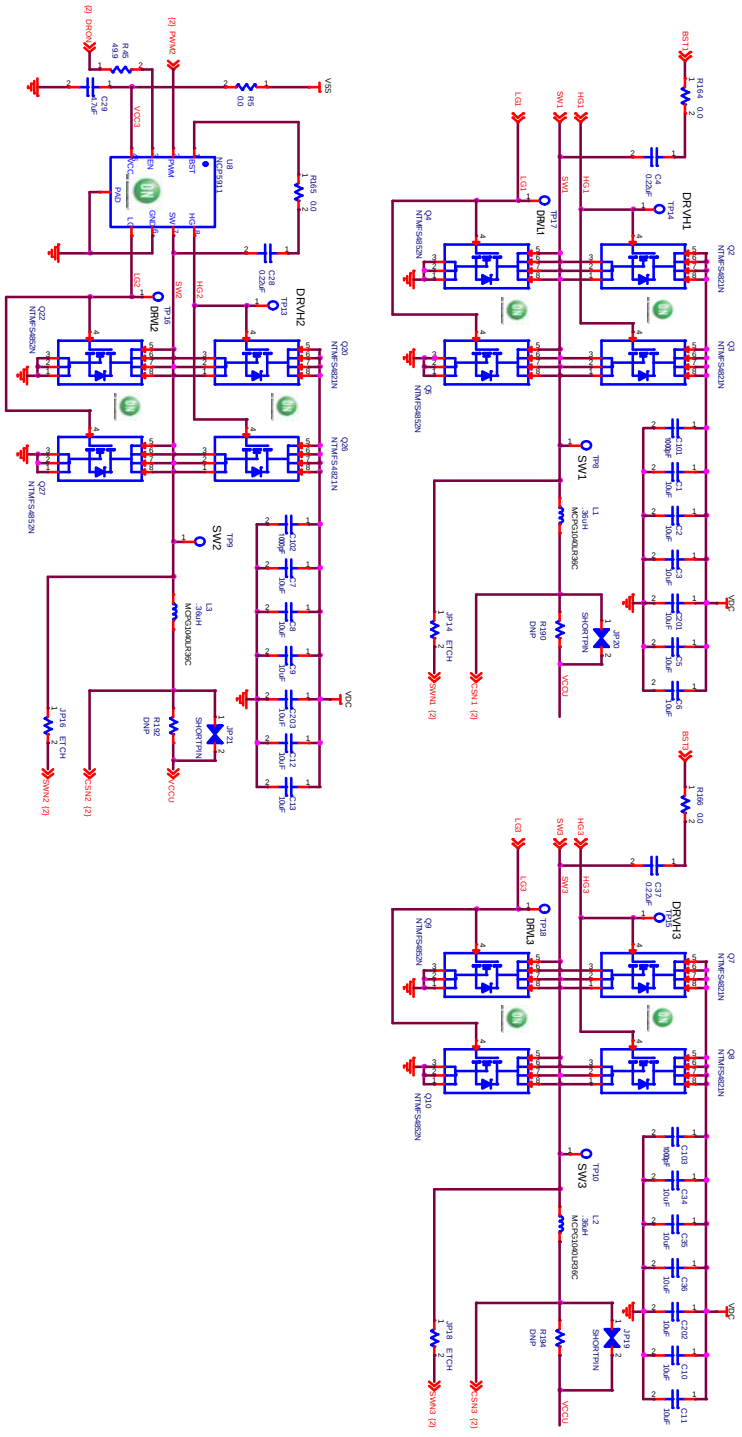


Figure 3. Power Stage Schematic

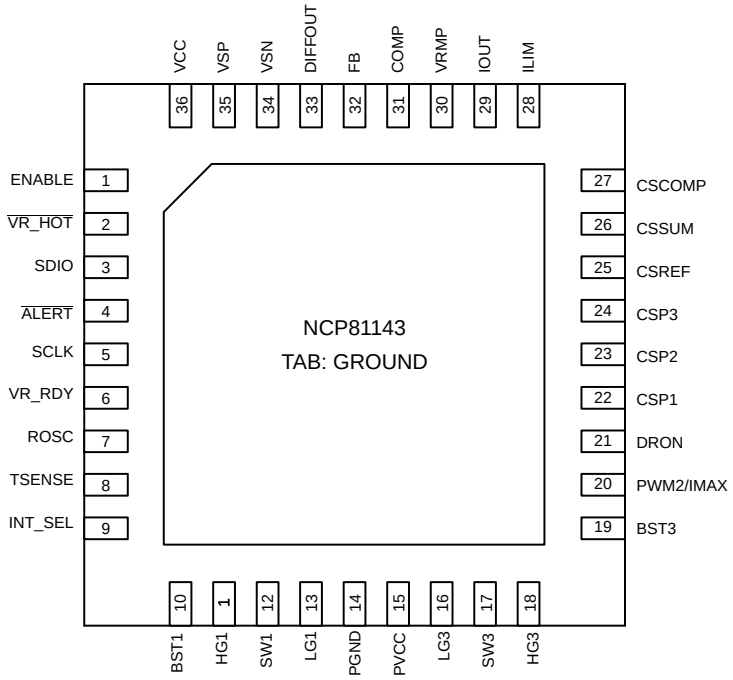


Figure 4. NCP81143 Pin Configuration

NCP81143 SINGLE ROW PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	ENABLE	Logic input. Logic high enables both outputs and logic low disables both outputs
2	VR_HOT#	Thermal logic output for over temperature
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#.
5	SCLK	Serial VID clock
6	VR_RDY	Open drain output. High indicates that the output is regulating
7	ROSC	A resistance from this pin to ground programs the oscillator frequency
8	TSENSE	Temp Sense input for the multiphase converter
9	INT_SEL	An input pin to adjust programmable integrator setting. During start up it is used to program INT_SEL with a resistor to ground
10	BST1	High−Side bootstrap supply for phase 1.
11	HG1	High side gate driver output for phase 1
12	SW1	Current return for high side gate driver 1
13	LG1	Low−Side gate driver output for phase 1
14	PGND	Power Ground for gate drivers
15	PVCC	Power Supply for gate drivers
16	LG3	Low−Side gate driver output for phase 3
17	SW3	Current return for high side gate driver 3
18	HG3	High side gate driver output for phase 3
19	BST3	High−Side bootstrap supply for phase 3
20	PWM2/IMAX	Phase 2 PWM output. Also as ICC_MAX Input Pin. During start up it is used to program ICC_MAX with a resistor to ground
21	DRON	Bidirectional gate drive enable output

NCP81143 SINGLE ROW PIN DESCRIPTIONS

Pin No.	Symbol	Description
22	CSP1	Non−inverting input to current balance sense amplifier for phase 1
23	CSP2	Non−inverting input to current balance sense amplifier for phase 2
24	CSP3	Non−inverting input to current balance sense amplifier for phase 3
25	CSREF	Total output current sense amplifier reference voltage input
26	CSSUM	Inverting input of total current sense amplifier
27	CSCOMP	Output of total current sense amplifier
28	ILIM	Over current shutdown threshold setting. Resistor to CSCOMP to set threshold
29	IOUT	Total output current monitor.
30	VRMP	Feed−forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope
31	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators
32	FB	Error amplifier voltage feedback
33	DIFFOUT	Output of the differential remote sense amplifier
3	VSN	Inverting input to differential remote sense amplifier
35	VSP	Non−inverting input to the differential remote sense amplifier
36	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
37	FLAG /GND	Analog Ground

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Pin Symbol	V_{MAX}	V_{MIN}
COMP	V_{CC} + 0.3 V	−0.3 V
CSCOMP	V_{CC} + 0.3 V	−0.3 V
VSN	GND + 300 mV	GND − 300 mV
DIFFOUT	V_{CC} + 0.3 V	−0.3 V
VR_RDY	V_{CC} + 0.3 V	−0.3 V
VCC	6.5 V	−0.3 V
ROSC	V_{CC} + 0.3 V	−0.3 V
IOUT	2.0 V	−0.3 V
VRMP	+25 V	−0.3 V
SW	35 V 40 V ≤ 50 ns	−5 V −10 V ≤ 200 ns
BST	35 V wrt/ GND 40 V ≤ 50 ns wrt/GND 6.5 V wrt/ SW	−0.3 V wrt/SW
LG	V_{CC} + 0.3 V	−0.3 V −5 V ≤ 200 ns
HG	BST + 0.3 V	−0.3 V wrt/ SW −2 V ≤ 200 ns wrt/SW
All Other Pins	V_{CC} + 0.3 V	−0.3 V

*All signals referenced to GND unless noted otherwise.

THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 1)	$R_{\theta JA}$	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to +125	°C
Operating Ambient Temperature Range		−40 to +100	°C
Maximum Storage Temperature Range	T_{STG}	− 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

NCP81143 ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current	@ 1.3 V	−400		400	nA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 kΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 1.5 V – 2.5 V, CL = 20 pF to GND, DC Load = 10k to GND		20		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5			V
Minimum Output Voltage	I_{SINK} = 2.0 mA			1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current	VSP,VSN = 1.3 V	−25		25	μA
VSP Input Voltage Range		−0.3		3.0	V
VSN Input Voltage Range		−0.3		0.3	V
−3dB Bandwidth	CL = 20 pF to GND, RL = 10 kΩ to GND		10		MHz
Closed Loop DC gain	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos), (Note 3)		−300		300	μV
Input Bias Current	CSSUM = CSREF= 1 V	−5		5	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND		10		MHz
CURRENT BALANCE AMPLIFIER					
Maximum CSCOMP Output Voltage	I_{SOURCE} = 2 mA	3.5			V
Minimum CSCOMP Output Voltage	I_{SINK} = 500 μA			0.1	V
Input Bias Current	$CSP_{1−3}$ = CSREF = 1.2	−50		50	nA
Common Mode Input Voltage Range	CSPx = CSREF	0		2.3	V
Differential Mode Input Voltage Range	CSREF = 1.2 V	−100		100	mV
Input Offset Voltage Matching	CSPx = CSREF = 1.2 V, Measured from the average	−1.5		1.5	mV
Current Sense Amplifier Gain	0 V < CSPx − CSREF < 0.1 V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSREF= CSP = 10 mV to 30 mV	−3		3	%
−3dB Bandwidth			8		MHz
INPUT SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	EN = high, PS0,1,2 Mode		20		mA
	EN = high, PS3 Mode		11		mA
	EN = l ow		50		μA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			V
VCC UVLO Hysteresis			160		mV

3. Guaranteed by design or characterization data, not in production test.

NCP81143 ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT SUPPLY					
UVLO Threshold	VRMP Rising			4.25	V
	VRMP Falling	3			V
DAC SLEW RATE					
Soft start slew rate			2.5		mv/μs
Slew Rate Slow			2.5		mv/μs
Slew Rate Fast			10		mv/μs
ENABLE INPUT					
Enable High Input Leakage Current	External 1k pull−up to 3.3 V			1.0	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.3	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$		90		mV
Enable Delay Time	Measure time from Enable transitioning HI to when DRON goes high			2.5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0			V
Output Low Voltage	Sinking 500 μA			0.1	V
Rise Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%		300		ns
Fall Time			10		
Internal Pull Down Resistance	EN = Low		70		kΩ
IOUT OUTPUT					
Input Referred Offset Voltage	Ilimit to CSREF	−3.5		3.5	mV
Output Source Current	Ilimit sink current = 80 μA			850	μA
Current Gain	($IOUT_{CURRENT}$) / ($ILIMIT_{CURRENT}$), R_{ILIM} = 20k, R_{IOUT} = 5.0k , DAC = 0.8 V, 1.25 V, 1.52 V	9.67	10	10.32	
OSCILLATOR					
Switching Frequency Range		220		1000	KHz
3 Phase Operation				1000	kHz
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Absolute Over Voltage Threshold During Soft Start	CSREF		2.9		V
Over Voltage Threshold Above DAC	VSP rising	350	400	425	mV
Over Voltage Delay	VSP rising to PWMx low		50		ns
Under Voltage	Ckt in development		300		mV
Under−voltage Delay	Ckt in development		5		μs
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS0) Rlim = 20k	9.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	(PS0) Rlim = 20k	13.5	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	(PS1, PS2, PS3) Rlim = 20k, N = number of phases in PS0 mode		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	(PS1, PS2, PS3) Rlim = 20k, N = number of phases in PS0 mode		15/N		μA

3. Guaranteed by design or characterization data, not in production test.

NCP81143 ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
MODULATORS (PWM Comparators)					
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP = 12.0 V		2.5		V
PWM Ramp Duty Cycle Matching	COMP = 2 V, PWM Ton matching		1		%
PWM Phase Angle Error	Between adjacent phases		±5		°
Ramp Feed−forward Voltage range		5		20	V
VR_HOT#					
Output Low Voltage	$I_{\_VRHOT}$ = −4 mA			0.3	V
Output Leakage Current	High Impedance State	−1.0		1.0	μA
TSENSE					
Alert# Assert Threshold	NTC=100k in parallel with 8.2k @ 97C		491		mV
Alert# De−assert Threshold	NTC=100k in parallel with 8.2k = 94C		513		mV
VRHOT Assert Threshold	NTC=100k in parallel with 8.2k = 100C		472		mV
VRHOT Rising Threshold	NTC=100k in parallel with 8.2k = 97C		494		mV
TSENSE Bias Current	−10°C to 85°C −40°C to 100°C	115	120	125	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1		1	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			±1		%
Conversion Time			30		μs
Round Robin			90		μs
VR_RDY, (Power Good) OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA,			0.3	V
Rise Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%		250		ns
Fall Time	External pull−up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%		30		ns
Output Voltage at Power−up	VR_RDY pulled up to 5 V via 2 kΩ			1.0	V
Output Leakage Current When High	VR_RDY = 5.0 V	−1.0		1.0	μA
VR_RDY Delay (rising)	DAC = TARGET to VR_RDY		50		μs
VR_RDY Delay (falling)	From OCP or OVP		5		μs
VR_REDY Delay (falling)	From OCP		50		μs
PWM OUTPUTS					
Output High Voltage	Sourcing 500 μA	V_{CC} − 0.2V			V
Output Mid Voltage	No Load, SetPS = 02	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA			0.7	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo = GND to V_{CC}		10		ns

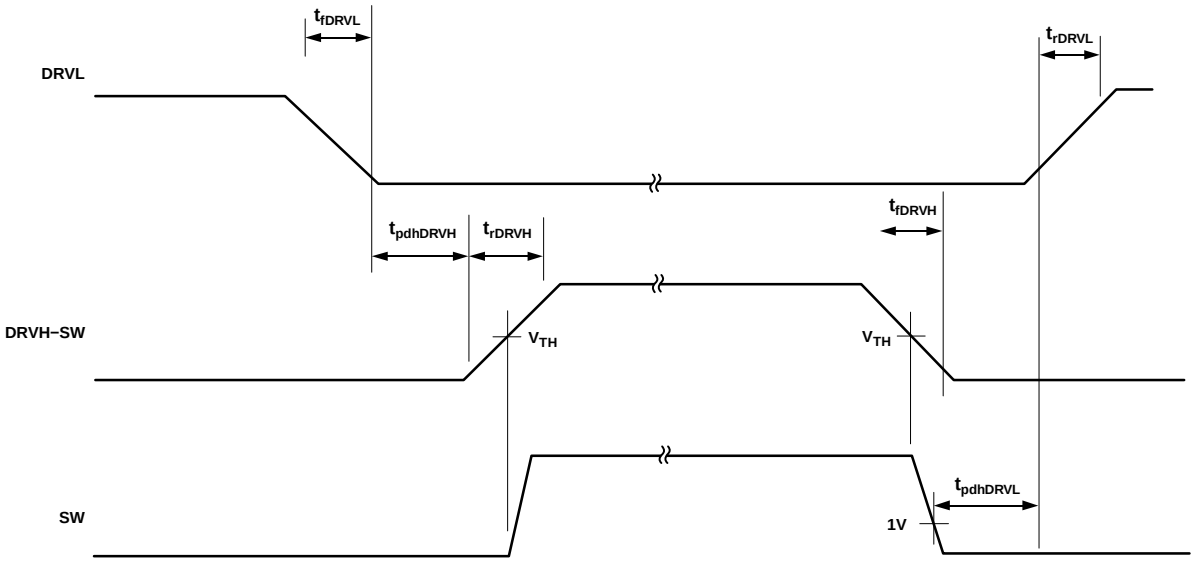
3. Guaranteed by design or characterization data, not in production test.

NCP81143 ELECTRICAL CHARACTERISTICS

Unless otherwise stated: −40°C < T_A < 100°C; V_{CC} = 5 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
PHASE DETECTION					
CSP Pin Threshold voltage		4.5			V
Phase Detect Timer			100		μs
HIGH−SIDE MOSFET DRIVER					
Pull−up Resistance, Sourcing Current	BST = PVCC		1.2	3.1	Ω
High Side Driver Sourcing Current	BST = PVCC		4.17		A
Pull−down Resistance, Sinking Current	BST = PVCC		0.8	2.5	Ω
High Side Driver Sinking Current	BST = PVCC		6.25		A
HGx Rise Time	VCC = 5 V, 3 nF load, BST−SW = 5 V	6	16	30	ns
HGx Fall Time	VCC = 5 V, 3 nF load, BST−SW = 5 V	6	11	30	ns
HGx Turn on Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF	+	30	47	ns
SWx Pull−Down Resistance	SW to PGND		2		kΩ
LOW−SIDE MOSFET DRIVER					
Pull−up Resistance, Sourcing Current			0.9	3.4	Ω
Low Side Driver Sourcing Current			5.56		A
Pull−down Resistance, Sinking Current			0.4	2.0	Ω
Low Side Driver Sinking Current			12.5		A
LGx Rise Time	3 nF load	6	16	30	ns
LGx Fall Time	3 nF load	6	11	30	ns
LGx Turn−On Propagation Delay tpdhDRVL	C_{LOAD} = 3 nF		11	30	ns
PVCC Quiescent Current	EN = L (Shutdown) EN = H, no switching		1.0 490	15	μA
BOOTSTRAP ON RESISTANCE					
ON Resistance	EN = L or EN = H with DRVL = H	5	9	21	Ω

3. Guaranteed by design or characterization data, not in production test.



NOTE: Timing is referenced to the 90% and the 10% points, unless otherwise stated.

Figure 5. Driver Timing Diagram

STATE TRUTH TABLE

State	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	DRON Pin	Method of Reset
POR 0 < VCC < UVLO	N/A	N/A	N/A	Resistive pull down	
Disabled EN < threshold UVLO >threshold	Low	Low	Disabled	Low	
Start up Delay & Calibration EN > threshold UVLO > threshold	Low	Low	Disabled	Low	
DRON Fault EN > threshold UVLO > threshold DRON < threshold	Low	Low	Disabled	Resistive pull up	Driver must release DRON to high
Soft Start EN > threshold UVLO > threshold DRON > High	Low	Operational	Active / No latch	High	
Normal Operation EN > threshold UVLO > threshold DRON > High	High	Operational	Active / Latching	High	N/A
Over Voltage	Low	N/A	DAC + 400 mV	High	
Over Current	Low	Operational	Last DAC Code	Low	
V_{OUT} = 0 V	Low: if Reg34h:bit0 = 0; High:if Reg34h:bit0 = 1;	Clamped at 0.9 V	Disabled	High, PWM outputs in low state	

Figure 6. State Diagram

General

The NCP81143 is a three phase dual edge modulated multiphase PWM controller, with a serial SVID control interface. The NCP81143 is optimized to meet Intel's VR12.5 Specifications. It is designed to work in notebook, desktop, and server applications.

The NCP81143 has two integrated drivers and one external PWM signal. Internally, there are 2 PWM signals: PWM1/3, DRV1 is driven by PWM1, DRV3 is driven by PWM3, and the third phase has a PWM output, PWM2, to dive an external driver such as the NCP81151.

Phase	PWM Output
3	Internal PWM
2	External PWM
1	Internal PWM

Serial VID interface (SVID)

For SVID Interface communication details please contact Intel Inc.

BOOT VOLTAGE PROGRAMMING

The Boot voltage for the NCP81143 is configured to 1.7 V.

INT_SEL

The remote Sense Amplifier output is applied to a Type III compensation network formed by the error amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote sense amplifier output. The integrating function of the Type III feedback compensation is performed internally and does not require external capacitor CF1.

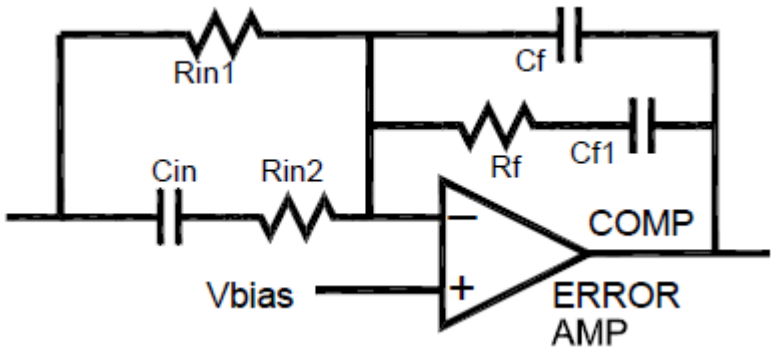


Figure 7. Type III Compensation

Initial tuning should be based on the traditional TYPE III compensation. When ideal Type III component values have been determined, the closest setting for the internal integrator us given by the following equation :

$$INT\_SETTING = 4.83 \times 10^{-12} \times RF \times Rin1 \times CF1$$

RF & Rin1 in ohms

CF1 in nF

Optimization of the traditional Type 3 compensation should be rechecked unin the closest Type 3 CF1 equivalent in order to deternone if readjustment of other component values are required. The Type III CF1 value that is equivalent to the integrator setting is given by the following equation:

$$Cf1(nF) = 2.07 \times 10^{5} \times INT\_Setting/(RF \times Rin1)$$

Table 1. RF = 5k and Rin = 1 kΩ

Resistor Range	Int_select Setting	Phase Count in PS1	Equivalent Cf1 in Type III Compensation	Equivalent Rf in Type III Compensation
0 − 5.08 kΩ	0000	1	43 pF	5 kΩ
5.08 kΩ − 14.1 kΩ	0001	1	82 pF	5 kΩ
14.1 kΩ − 21.9 kΩ	0010	1	160 pF	5 kΩ
21.9 kΩ − 30.1 kΩ	0011	1	330 pF	5 kΩ
30.1 kΩ − 39.1 kΩ	0100	1	430 pF	5 kΩ
39.1 kΩ − 48.4 kΩ	0101	1	510 pF	5 kΩ
48.4 kΩ − 57.8 kΩ	0110	1	680 pF	5 kΩ
57.8 kΩ − 67.6 kΩ	0111	1	1300 pF	5 kΩ
67.6 kΩ − 78.1 kΩ	1000	1	2700 pF	5 kΩ
78.1 kΩ − 89.5 kΩ	0000	2	43 pF	5 kΩ
89.5 kΩ − 101 kΩ	0001	2	82 pF	5 kΩ
101 kΩ − 113 kΩ	0010	2	160 pF	5 kΩ
113 kΩ − 125 kΩ	0011	2	330 pF	5 kΩ
125 kΩ − 138 kΩ	0100	2	430 pF	5 kΩ
138 kΩ − 151 kΩ	0101	2	510 pF	5 kΩ
151 kΩ − 163 kΩ	0110	2	680 pF	5 kΩ
163 kΩ − 177 kΩ	0111	2	1300 pF	5 kΩ
177 kΩ − 193 kΩ	1000	2	2700 pF	5 kΩ

Table 2. RF = 7.5k and Rin = 1 kΩ

Resistor Range	Int_select Setting	Phase Count in PS1	Equivalent Cf1 in Type III Compensation	Equivalent Rf in Type III Compensation
0 − 5.08 kΩ	0000	1	27 pF	7.5 kΩ
5.08 kΩ − 14.1 kΩ	0001	1	56 pF	7.5 kΩ
14.1 kΩ − 21.9 kΩ	0010	1	110 pF	7.5 kΩ
21.9 kΩ − 30.1 kΩ	0011	1	220 pF	7.5 kΩ
30.1 kΩ − 39.1 kΩ	0100	1	270 pF	7.5 kΩ
39.1 kΩ − 48.4 kΩ	0101	1	330 pF	7.5 kΩ
48.4 kΩ − 57.8 kΩ	0110	1	430 pF	7.5 kΩ
57.8 kΩ − 67.6 kΩ	0111	1	910 pF	7.5 kΩ
67.6 kΩ − 78.1 kΩ	1000	1	1800 pF	7.5 kΩ
78.1 kΩ − 89.5 kΩ	0000	2	27 pF	7.5 kΩ
89.5 kΩ − 101 kΩ	0001	2	56 pF	7.5 kΩ
101 kΩ − 113 kΩ	0010	2	110 pF	7.5 kΩ
113 kΩ − 125 kΩ	0011	2	220 pF	7.5 kΩ
125 kΩ − 138 kΩ	0100	2	270 pF	7.5 kΩ
138 kΩ − 151 kΩ	0101	2	330 pF	7.5 kΩ
151 kΩ − 163 kΩ	0110	2	430 pF	7.5 kΩ
163 kΩ − 177 kΩ	0111	2	910 pF	7.5 kΩ
177 kΩ − 193 kΩ	1000	2	1800 pF	7.5 kΩ

Table 3. RF = 10k and Rin = 1 kΩ

Resistor Range	Int_select Setting	Phase Count in PS1	Equivalent Cf1 in Type III Compensation	Equivalent Rf in Type III Compensation
0 − 5.08 kΩ	0000	1	20 pF	10 kΩ
5.08 kΩ − 14.1 kΩ	0001	1	43 pF	10 kΩ
14.1 kΩ − 21.9 kΩ	0010	1	82 pF	10 kΩ
21.9 kΩ − 30.1 kΩ	0011	1	160 pF	10 kΩ
30.1 kΩ − 39.1 kΩ	0100	1	200 pF	10 kΩ
39.1 kΩ − 48.4 kΩ	0101	1	240 pF	10 kΩ
48.4 kΩ − 57.8 kΩ	0110	1	330 pF	10 kΩ
57.8 kΩ − 67.6 kΩ	0111	1	680 pF	10 kΩ
67.6 kΩ − 78.1 kΩ	1000	1	1300 pF	10 kΩ
78.1 kΩ − 89.5 kΩ	0000	2	20 pF	10 kΩ
89.5 kΩ − 101 kΩ	0001	2	43 pF	10 kΩ
101 kΩ − 113 kΩ	0010	2	82 pF	10 kΩ
113 kΩ − 125 kΩ	0011	2	160 pF	10 kΩ
125 kΩ − 138 kΩ	0100	2	200 pF	10 kΩ
138 kΩ − 151 kΩ	0101	2	240 pF	10 kΩ
151 kΩ − 163 kΩ	0110	2	330 pF	10 kΩ
163 kΩ − 177 kΩ	0111	2	680 pF	10 kΩ
177 kΩ − 193 kΩ	1000	2	1300 pF	10 kΩ

For further explanation on the integrator setting and operation please refer to application note.

Boost Capacitor Refresh Mode

The NCP81143 include a boost capacitor refresh mode which aids the correct operation of inactive phase when exiting low power states. The mode is used where phases are shed in PS1,2 and 3 modes; in these cases it is possible that the drivers boost capacitor voltage, Vbst, may drop below 1.7 V. If this occurs the Boost capacitor charge will not be able to meet the gate source requirements for the first firing of the high side MOSFET when returning to PS0 power state. For further information on the operation of the boost capacitor refresh mode please see application note.

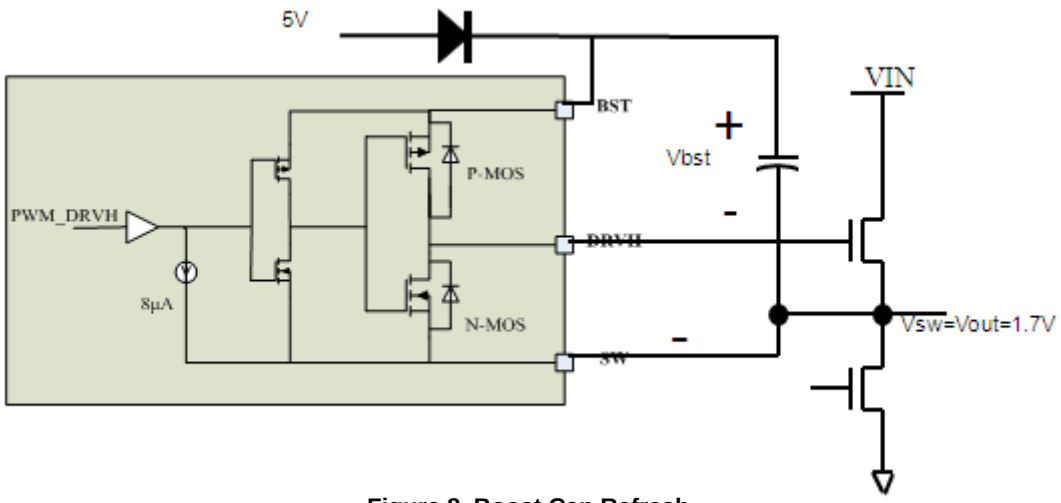


Figure 8. Boost Cap Refresh

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFFOUT} = \left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \left(V_{DROOP} - V_{CSREF}\right)$$

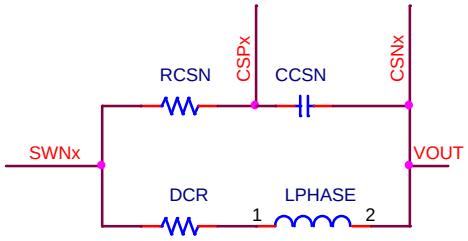
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type II compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

Figure 9. Differential Current Feedback

Total Current Sense Amplifier

The NCP81143 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

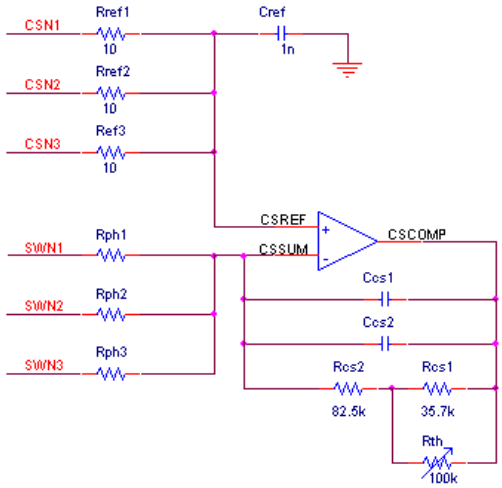


Figure 10. Total Current Sense

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{Total} * DCR\right)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 100k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_z = \frac{DCR@25^\circ C}{2 * PI * L_{Phase}}$$

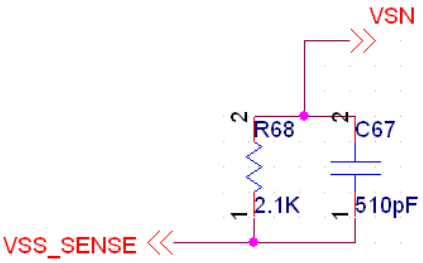
Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth} * \left(Iout_{LIMIT} * DCR\right)}{10\mu} \text{ or } R_{LIMIT} = \frac{V_{CSCOMP-CSREF@ILIMIT}}{10\mu}$$

Programming DAC Feed−Forward Filter

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.



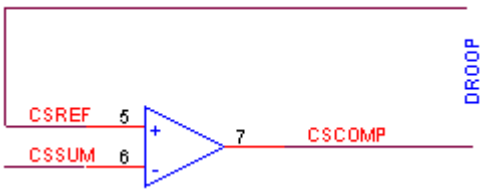
$$Rvsn = Cout * Rout * 453.6 \times 10^6$$

$$Cvsn = \frac{Rout * Cout}{Rvsn}$$

Figure 11. DAC Feed−Forward

Programming DROOP

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



$$Droop = DCR * \left(R_{CS}/R_{ph}\right)$$

Figure 12. Droop

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V V_{CC} can be used to offset the IOUT signal positive if needed.
Below equation relates to the NCP81143 only:

$$R_{IOUT} = \frac{2.0\ V * R_{LIMIT}}{10 * \frac{Rcs2 + \frac{Rcs1*Rth}{Rcs1+Rth}}{Rph} * \left(Iout_{ICC\_MAX} * DCR\right)}$$

Programming ICC_MAX

A resistor to Ground is monitored on startup and this sets the ICC_MAX value. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10k.

$$ICC\_MAX = \frac{R * 10\ \mu A * 256\ A}{2\ V}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.

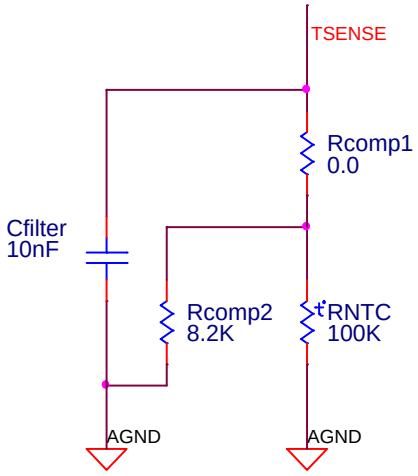


Figure 13. T_{SENSE}

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 220 kHz/phase to 1 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

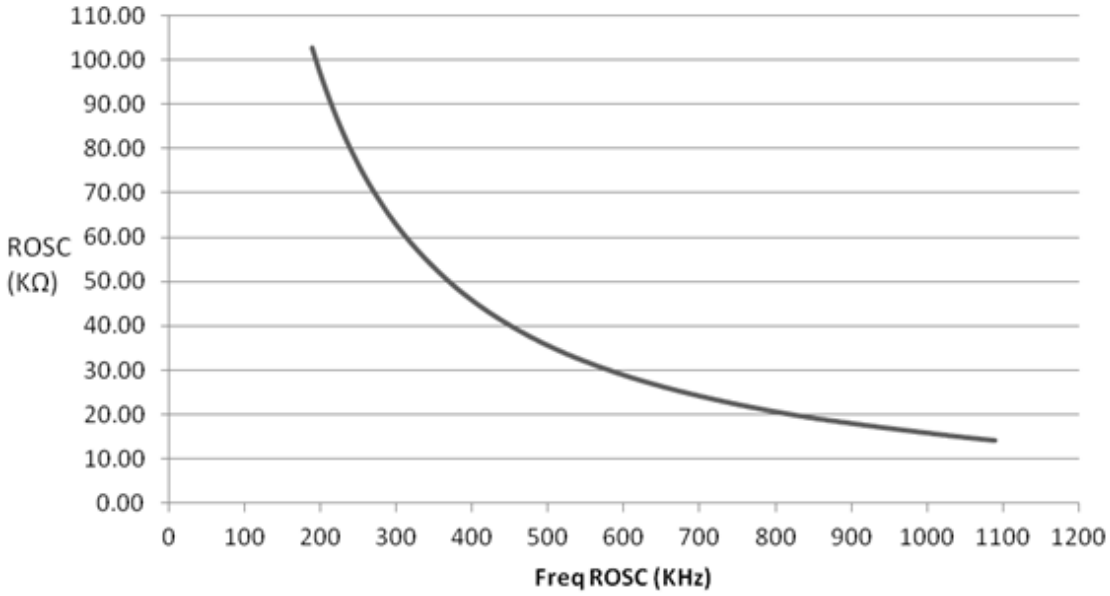


Figure 14. NCP81143 Operating Frequency vs. Rosc

The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following,

$$V_{RAMPpk\Leftarrow pkPP} = 0.1 * V_{VRMP}$$

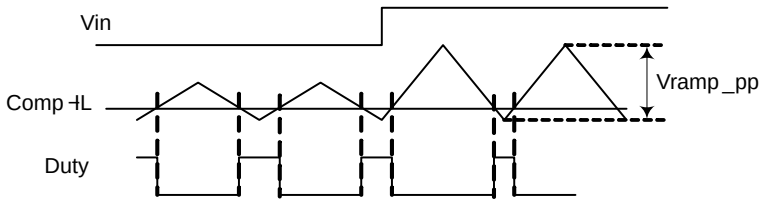


Figure 15. Ramp Feed−Forward

PWM Comparators

The noninverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (I_L*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

Phase Detection Sequence

During start−up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the CSP outputs. Normally, NCP81143 operates as a 3−phase VCORE PWM controller.

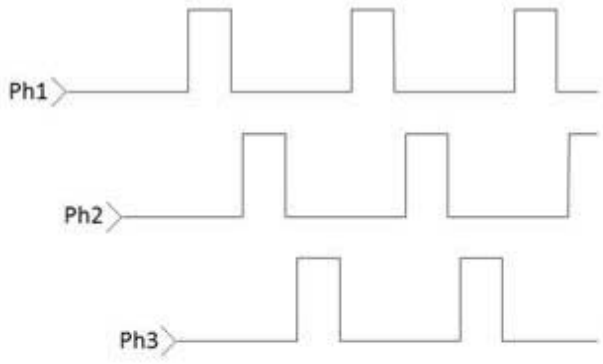


Figure 16. 3 Phase Mode

Pulling CSP2 high to VCC configures the NCP81143 to operate in 2 phase mode.

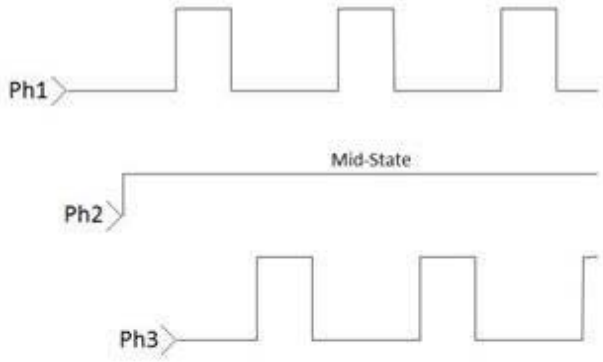


Figure 17. 2 Phase Mode

Pulling CSP3 and CSP2 high to VCC configures the NCP81143 to operate in 1 phase mode.

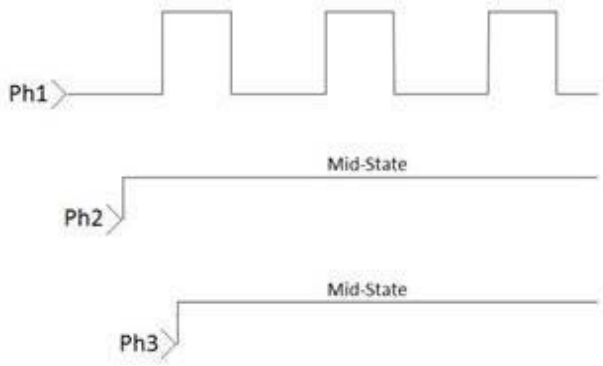


Figure 18. 1 Phase Mode

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the NCP81151. As each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

PROTECTION FEATURES

Under voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81143 monitors the 5 V V_{CC} supply. The gate driver monitors both the gate driver V_{CC} and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off it's startup sequence. In this case the PWM is set to the MID state to begin soft start.

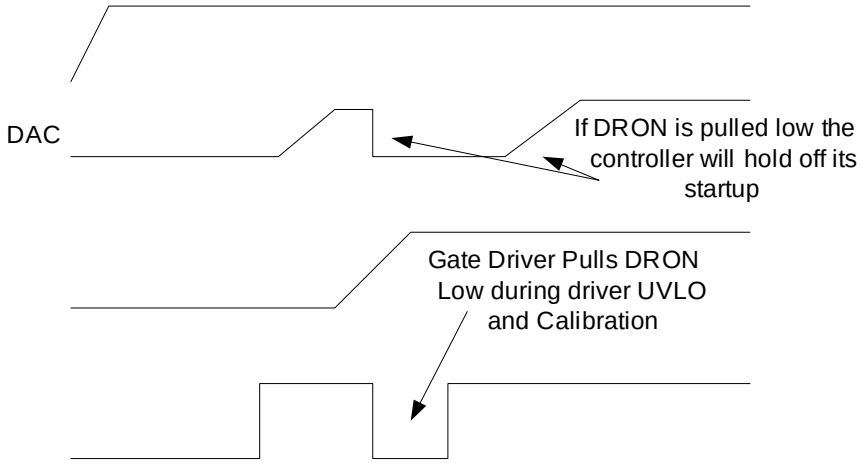


Figure 19. Gate Driver UVLO Restart

Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected, if the controller is enabled the PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state.

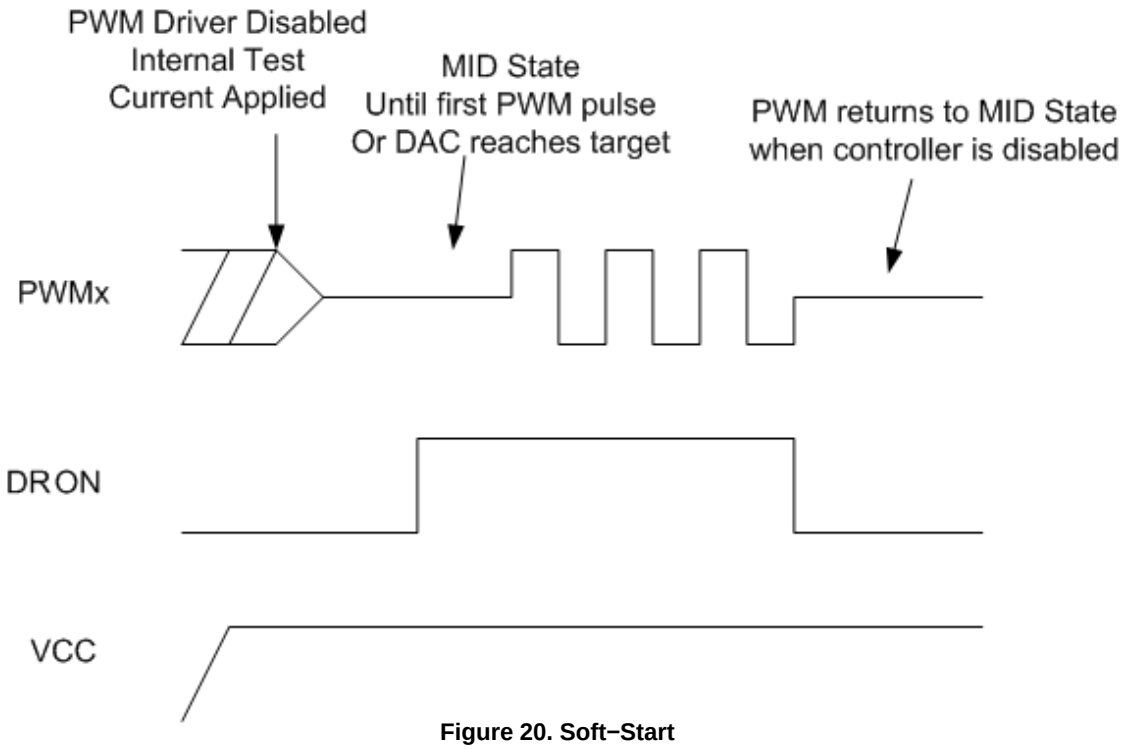


Figure 20. Soft−Start

Over Current Latch− Off Protection

The NCP81143 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs (shut down immediately for 150% load current) after which the outputs will remain disabled until the V_{CC} voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations,

Equation related to the NCP81143:

$$R_{ILIM} = \frac{I_{LIM} * DCR * R_{CS}/R_{PH}}{I_{CL}}$$

Where I_{CL} = 10 μA

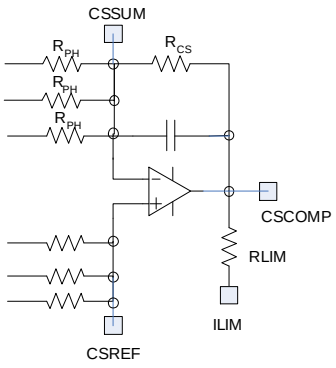


Figure 21. I_{lim} Resistor

Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low. The 300 mV limit can be reprogrammed using the VR_Ready_Low Limit register.

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V. At the same time, the high side gate drivers are all turned off and the low side gate drivers are all turned on. The part will stay in this mode until the V_{CC} voltage or EN is toggled. The part will stay in the mode until the V_{CC} voltage or EN is toggled.

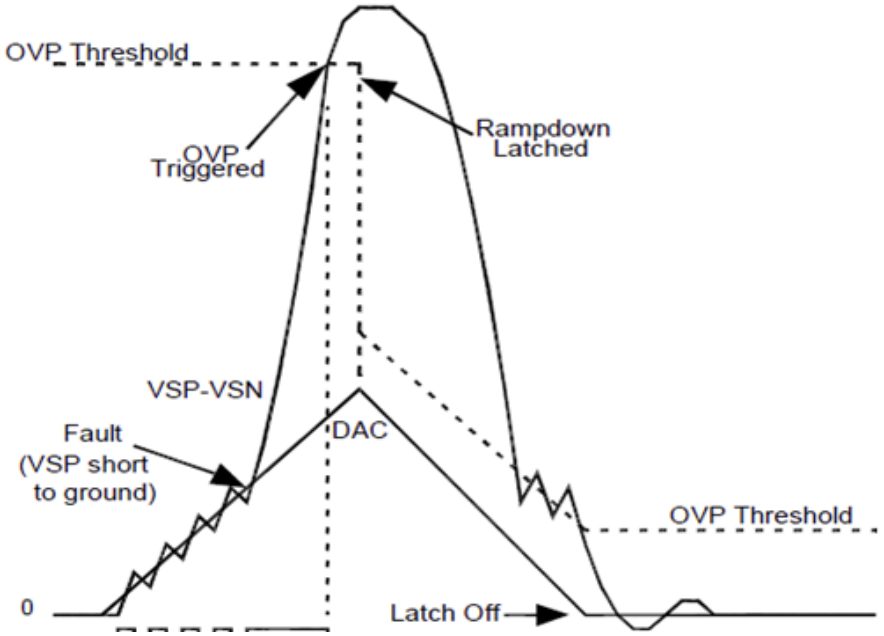


Figure 22. OVP Behavior at Startup

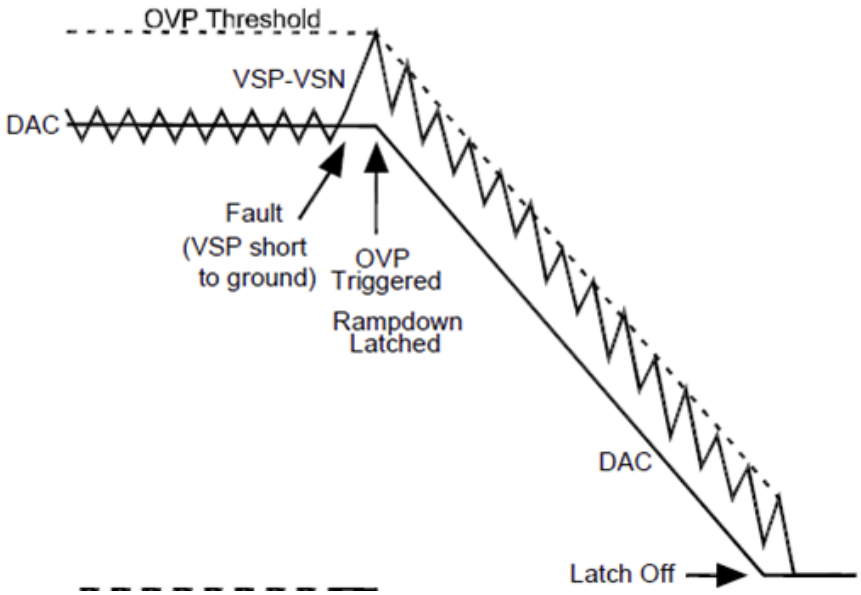


Figure 23. OVP During Normal Operation Mode

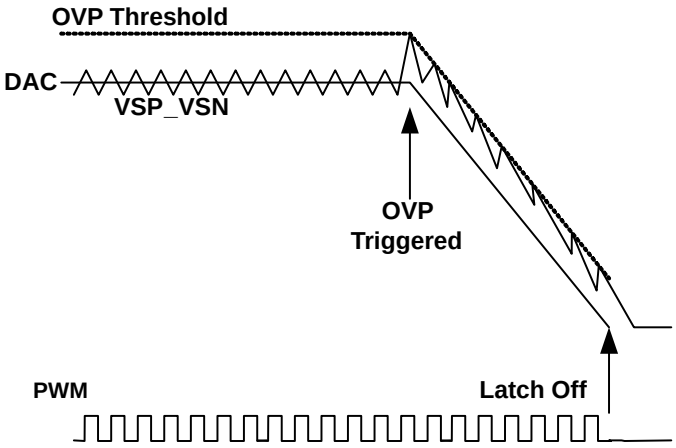


Figure 24. OVP During Normal Operation Mode

During start up, the OVP threshold is set to 2.9 V. This allows the controller to start up without false triggering the OVP

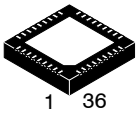
ORDERING INFORMATION

Device	Package	Shipping†
NCP81143MNTXG	QFN36 (Pb−Free)	5000 / Tape & Reel

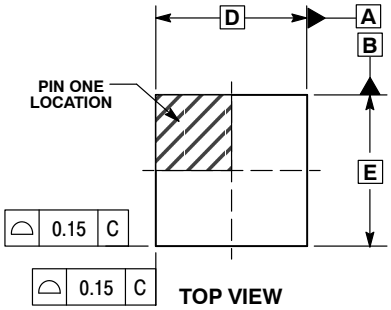
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

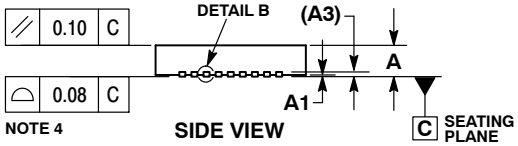
QFN36 5x5, 0.4P
CASE 485CC
ISSUE O

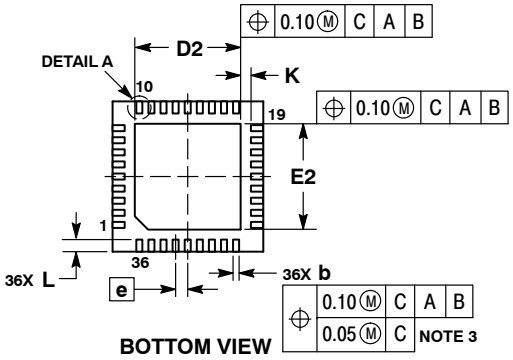
DATE 29 NOV 2011

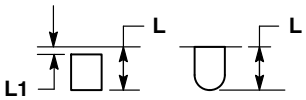


SCALE 2:1

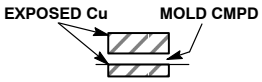








DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

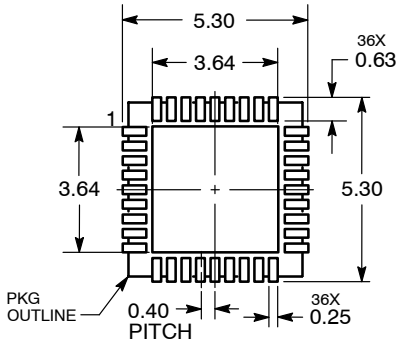
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.40 BSC	
K	0.35 REF	
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON65654E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN36, 5x5, 0.4P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales