

# NLSX4302E

## 2-Bit 20 Mb/s Dual-Supply Level Translator

The NLSX4302E is a 2-bit configurable dual-supply bidirectional auto sensing translator that does not require a directional control pin. The  $V_{CC}$  I/O and  $V_L$  I/O ports are designed to track two different power supply rails,  $V_{CC}$  and  $V_L$  respectively. Both the  $V_{CC}$  and  $V_L$  supply rails are configurable from 1.5 V to 5.5 V. This allows voltage logic signals on the  $V_L$  side to be translated into lower, higher or equal value voltage logic signals on the  $V_{CC}$  side, and vice-versa.

The NLSX4302E translator uses external pull-up resistors on the I/O lines. The external pull-up resistors are used to pull up the I/O lines to either  $V_L$  or  $V_{CC}$ . The NLSX4302E is an excellent match for open-drain applications such as the I<sup>2</sup>C communication bus.

### Features

- $V_L$  can be Less than, Greater than or Equal to  $V_{CC}$
- Wide  $V_{CC}$  Operating Range: 1.5 V to 5.5 V  
Wide  $V_L$  Operating Range: 1.5 V to 5.5 V
- High-Speed with 20 Mb/s Guaranteed Data Rate
- Low Bit-to-Bit Skew
- Enable Input and I/O Pins are Overvoltage Tolerant (OVT) to 5.5 V
- Non-preferential Powerup Sequencing
- Power-Off Protection
- Small Space Saving Package: 1.4 mm x 1.2 mm UQFN8 Package
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- I<sup>2</sup>C, SMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

### Important Information

- ESD Protection for All Pins
  - Human Body Model (HBM) > 6000 V
  - Machine Model (MM) > 400 V



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS

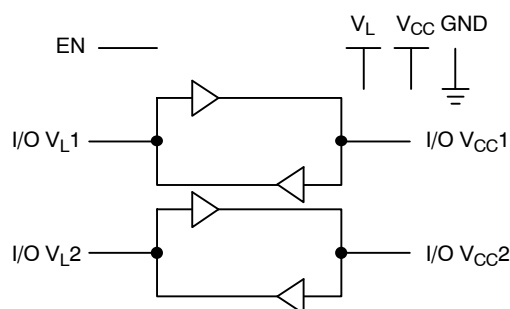


UQFN8  
MU SUFFIX  
CASE 523AS



E = Specific Device Code  
M = Date Code

### LOGIC DIAGRAM



### ORDERING INFORMATION

Device	Package	Shipping†
NLSX4302EBMUTCG	UQFN8 (Pb-Free)	3000/Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLSX4302E

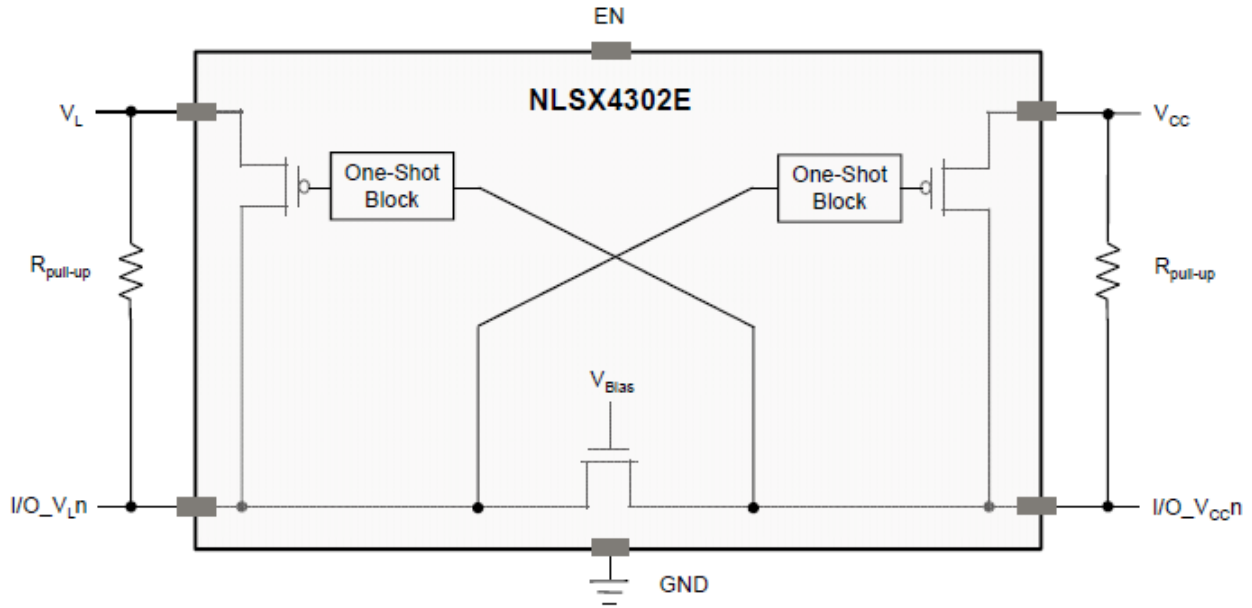


Figure 1. Block Diagram (1 I/O Line)

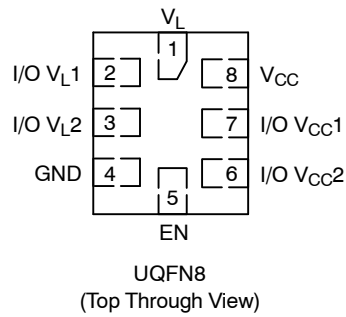


Figure 2. Pin-out Diagram

## PIN ASSIGNMENT

Pins	Description
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage
V <sub>L</sub>	V <sub>L</sub> Supply Voltage
GND	Ground
EN	Output Enable, Referenced to V <sub>L</sub>
I/O V <sub>CC</sub> n	I/O Port, Referenced to V <sub>CC</sub>
I/O V <sub>L</sub> n	I/O Port, Referenced to V <sub>L</sub>

## FUNCTION TABLE

EN	Operating Mode
L	Hi-Z
H	I/O Buses Connected

# NLSX4302E

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	High-side DC Supply Voltage	-0.3 to +7.0		V
V <sub>L</sub>	High-side DC Supply Voltage	-0.3 to +7.0		V
I/O V <sub>CC</sub>	V <sub>CC</sub> -Referenced DC Input/Output Voltage	-0.3 to (V <sub>CC</sub> + 0.3)		V
I/O V <sub>L</sub>	V <sub>L</sub> -Referenced DC Input/Output Voltage	-0.3 to (V <sub>L</sub> + 0.3)		V
V <sub>EN</sub>	Enable Control Pin DC Input Voltage	-0.3 to +7.0		V
I <sub>I/O_SC</sub>	Short-Circuit Duration (I/O V <sub>L</sub> and I/O V <sub>CC</sub> to GND)	40	Continuous	mA
T <sub>STG</sub>	Storage Temperature	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	High-side Positive DC Supply Voltage	1.5	5.5	V
V <sub>L</sub>	High-side Positive DC Supply Voltage	1.5	5.5	V
V <sub>EN</sub>	Enable Control Pin Voltage	GND	5.5	V
V <sub>IO_VCC</sub>	I/O Pin Voltage (Side referred to V <sub>CC</sub> )	GND	V <sub>CC</sub>	V
V <sub>IO_VL</sub>	I/O Pin Voltage (Side referred to V <sub>L</sub> )	GND	V <sub>L</sub>	V
Δt/ΔV	Input Transition Rise and Fall Rate I/O V <sub>L</sub> - or I/O V <sub>L</sub> - Ports, Push-Pull Driving Control Input		10 10	ns/V
T <sub>A</sub>	Operating Temperature Range	-40	+85	°C

# NLSX4302E

## DC ELECTRICAL CHARACTERISTICS ( $V_L = 1.5\text{ V to }5.5\text{ V}$ and $V_{CC} = 1.5\text{ V to }5.5\text{ V}$ , unless otherwise specified) (Note 1)

Symbol	Parameter	Test Conditions (Note 2)	$V_L$ (V)	$V_{CC}$ (V)	-40°C to +85°C			Unit	
					Min	Typ	Max		
$V_{IH\_VL}$	I/O High Level I/O_VL	Data Inputs I/O_VL <sub>n</sub>	1.65–5.50	1.65–5.50	$V_L - 0.4$			V	
		Control Input EN	1.65–5.50	1.65–5.50	$V_L \times 0.7$				
$V_{IH\_VCC}$	I/O High Level I/O_VCC	Data Inputs I/O_VCC <sub>n</sub>	1.65–5.50	1.65–5.50	$V_{CC} - 0.4$			V	
$V_{IL\_VL}$	I/O Low Level I/O_VL	Data Inputs I/O_VL <sub>n</sub>	1.65–5.50	1.65–5.50			0.4	V	
		Control Input EN	1.65–5.50	1.65–5.50			$V_L \times 0.3$		
$V_{IL\_VCC}$	I/O Low Level I/O_VCC	Data Inputs I/O_VCC <sub>n</sub>	1.65–5.50	1.65–5.50			0.4	V	
$V_{OL}$	Low Level Output Voltage	$V_{IL} = 0.15\text{ V}$ , $I_{OL} = 6\text{ mA}$	1.65–5.50	1.65–5.50			0.4	V	
$I_L$	Input Leakage Current	Control Input EN, $V_{IN} = V_L$ or GND	1.65–5.50	1.65–5.50			$\pm 1$	$\mu\text{A}$	
$I_{OFF}$	Power-Off Leakage Current	I/O_VL <sub>n</sub> , I/O_VCC <sub>n</sub>	$V_{IN}$ or $V_O = 0$ to 5.5 V	0	0			$\pm 2$	$\mu\text{A}$
		I/O_VL <sub>n</sub>		0	5.50				
		I/O_VCC <sub>n</sub>		5.50	0				
$I_{OZ}$	Tristate Output Mode Leakage Current (Note 3)	I/O_VL <sub>n</sub> , I/O_VCC <sub>n</sub>	$V_O = 0$ to 5.5 V, EN = $V_{IL}$	5.50	5.50			$\pm 2$	$\mu\text{A}$
		I/O_VL <sub>n</sub>	$V_O = 0$ to 5.5 V, EN = Don't Care	5.50	0				
		I/O_VCC <sub>n</sub>	$V_O = 0$ to 5.5 V, EN = Don't Care	0	5.50				
$I_{CC}$	Quiescent Supply Current, Active Mode (Notes 4, 5)	$V_L$	$V_{IN} = V_{CCI}$ or GND, $I_O = 0$ , EN = $V_{IH\_VL}$	1.65–5.50	1.65–5.50			5.0	$\mu\text{A}$
		$V_{CC}$							
$I_{CCZ}$	Quiescent Supply Current, Standby Mode (Notes 4, 5)	$V_L$	$V_{IN} = V_{CCI}$ or GND, $I_O = 0$ , EN = $V_{IL\_VL}$	1.65–5.50	1.65–5.50			5.0	$\mu\text{A}$
		$V_{CC}$							
$I_{CC\_OFF}$	Quiescent Supply Current, Power-Off (Notes 3, 5)	$V_L$	$V_{IN} = 5.5\text{ V}$ or GND, $I_O = 0$ , EN = Don't Care, I/O_VCC to I/O_VL	0	1.65–5.50			2.0	$\mu\text{A}$
				1.65–5.50	0				
		$V_{CC}$	$V_{IN} = 5.5\text{ V}$ or GND, $I_O = 0$ , EN = Don't Care, I/O_VL to I/O_VCC	1.65–5.50	0				
				0	1.65–5.50				

1. Typical values are for  $V_L = +1.8\text{ V}$ ,  $V_{CC} = +3.3\text{ V}$  and  $T_A = +25^\circ\text{C}$ .
2. All units are production tested at  $T_A = +25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed by design.
3. "Don't care" indicates any valid logic level.
4.  $V_{CCI}$  is the power supply associated with the input side.
5. Reflects current per supply,  $V_L$  or  $V_{CC}$ .

# NLSX4302E

## DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

**OUTPUT RISE / FALL TIMES** (Output Load:  $C_L = 50$  pF,  $R_{PU} = 2.2$  k $\Omega$ , push/pull driver,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 6)

Symbol	Parameter	$V_{CC0}$ (Note 7)				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Typ	Typ	Typ	Typ	
$t_{RISE}$	Output Rise Time, I/O_VL <sub>n</sub> , I/O_VCC <sub>n</sub>	6.4	5	6.5	10.7	ns
$t_{FALL}$	Output Fall Time, I/O_VL <sub>n</sub> , I/O_VCC <sub>n</sub>	10	9.5	8.6	9.5	ns

6. Output rise and fall times guaranteed by design and are not production tested.

7.  $V_{CC0}$  is the  $V_L$  or  $V_{CC}$  power supply associated with the output side.

**MAXIMUM DATA RATE** (Output Load:  $C_L = 50$  pF,  $R_{PU} = 2.2$  k $\Omega$ , push/pull driver,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 8)

$V_L$	Parameter	$V_{CC}$				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Min	Min	Min	Min	
4.5 to 5.5 V	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> or I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	50	41	31	17	MHz
3.0 to 3.6 V		34	35	36	23	MHz
2.3 to 2.7 V		25	27	30	24	MHz
1.65 to 1.95 V		14	16	22	21	MHz

8. Maximum frequency guaranteed by design and is not production tested.

# NLSX4302E

**AC ELECTRICAL CHARACTERISTICS** (Output Load:  $C_L = 50$  pF,  $R_{PU} = 2.2$  k $\Omega$ , push/pull driver,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 9)

Symbol	Parameter	V <sub>CC</sub>								Unit
		4.5 to 5.5 V		3.0 to 3.6 V		2.3 to 2.7 V		1.65 to 1.95 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	

**V<sub>L</sub> = 4.5 to 5.5 V**

t <sub>PLH</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	2.5	4.3	3	5	3	6.4	4	8.6	ns
t <sub>PHL</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	5	8.1	8	13	8	17.3	15	28.5	ns
t <sub>PZL</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	14	19.6	16	20	22	26.5	33	44	ns
t <sub>PLZ</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	24	31.4	25	32	24	31.8	28	36.2	ns
t <sub>skew</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub> (Note 10)	0.3	0.3	0.5	0.6	0.8	0.8	1.2	1.9	ns

**V<sub>L</sub> = 3.0 to 3.6 V**

t <sub>PLH</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	2.5	4.7	3	5.4	3	6.5	5	9.3	ns
t <sub>PHL</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	7	14.2	6	10.1	8	14.6	15	27	ns
t <sub>PZL</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	15	18.8	18	22.3	19	23.5	29	38.3	ns
t <sub>PLZ</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	25	34.9	22	27.6	22	27.9	23	28.8	ns
t <sub>skew</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub> (Note 10)	0.4	0.5	0.5	0.6	0.6	0.7	2.5	3.0	ns

**V<sub>L</sub> = 2.3 to 2.7 V**

t <sub>PLH</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	3	5.6	4	6	4	7.3	6	10.3	ns
t <sub>PHL</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	12	18.1	11	14.1	8	11.9	15	22.1	ns
t <sub>PZL</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	16	23.7	17	21.5	25	30	31	36.6	ns
t <sub>PLZ</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	28	33.8	26	31	25	30.8	25	30	ns
t <sub>skew</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub> (Note 10)	0.5	0.7	0.8	1	0.6	0.6	2.3	2.7	ns

**V<sub>L</sub> = 1.65 to 1.95 V**

t <sub>PLH</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	5	9	5	9.2	6	9.2	7	12.7	ns
t <sub>PHL</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub>	19	28.3	15	25.5	12	17.3	14	19	ns
t <sub>PZL</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	23	32.2	22	26.5	25	32	40	72	ns
t <sub>PLZ</sub>	OE to I/O_VI <sub>n</sub> , OE to I/O_VCC <sub>n</sub>	35	44	32	38.7	33	36.7	30	36.5	ns
t <sub>skew</sub>	I/O_VL <sub>n</sub> to I/O_VCC <sub>n</sub> , I/O_VCC <sub>n</sub> to I/O_VL <sub>n</sub> (Note 10)	0.5	1.1	1.4	1.5	0.8	1.1	2.0	2.5	ns

9. AC characteristics are guaranteed by design and are not production tested.

10. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (I/O\_VL<sub>n</sub> or I/O\_VCC<sub>n</sub>) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW). Skew is defined by applying a single input to the two input channels and measuring the difference in propagation delays between the output channels.

# NLSX4302E

## CAPACITANCE ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Test Condition	Typical	Unit
$C_{IN}$	Input Capacitance, Control Pin (EN)	$V_L = V_{CC} = \text{GND}$	2	pF
$C_{IO}$	Input / Output Capacitance (I/O_VL <sub>n</sub> , I/O_VCC <sub>n</sub> )	$V_L = V_{CC} = 5\text{ V}, \text{EN} = \text{GND}, \text{I/O\_VL}_n = \text{I/O\_VCC}_n = 5\text{ V}$	3	pF
$C_{PD}$	Power Dissipation Capacitance (Note 11)	$V_L = V_{CC} = 5\text{ V}, \text{EN} = 5\text{ V}, V_{IN} = 5\text{ V or GND}, f = 400\text{ KHz}$	17	pF

11.  $C_{PD}$  is defined as the value of the internal equivalent capacitance per channel.

## TEST SETUP AND TIMING DEFINITIONS

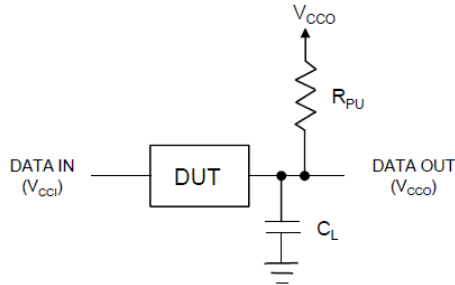


Figure 3. AC Test Circuit

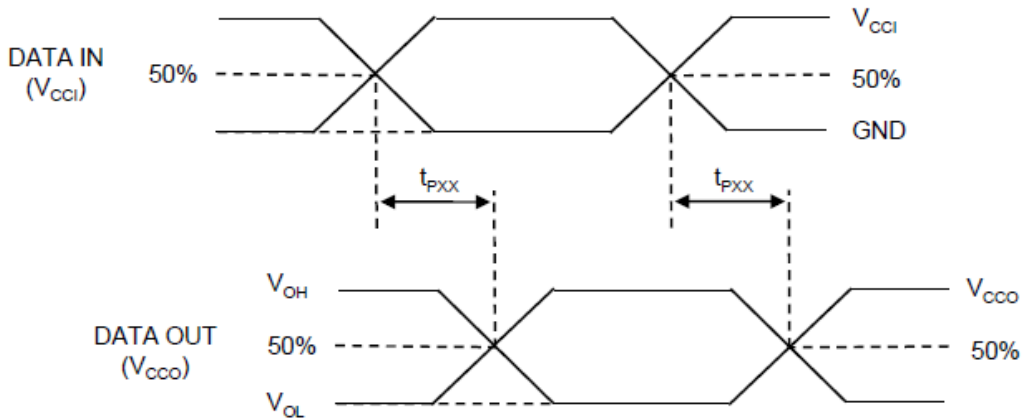


Figure 4. Propagation Delays and Tri-State Measurements

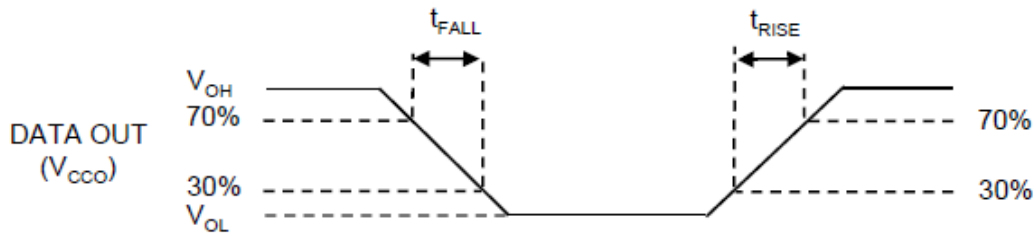


Figure 5. Definition of Rise and Fall Times

# NLSX4302E

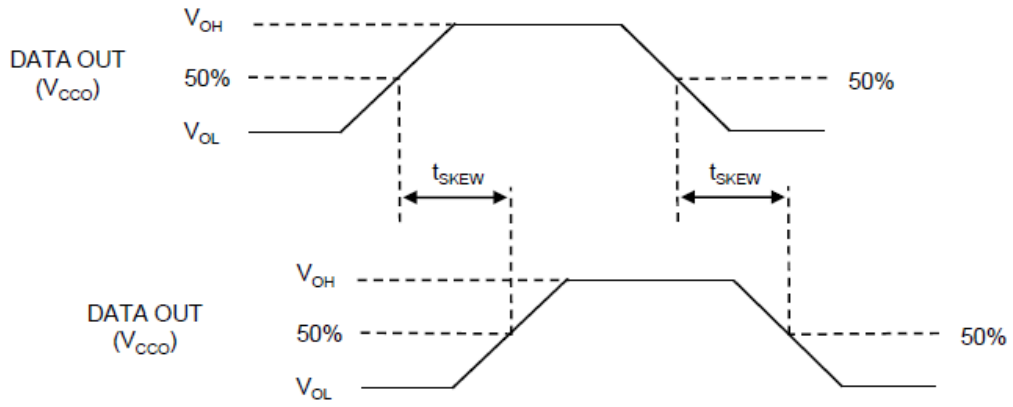


Figure 6. Definition of Output Skew

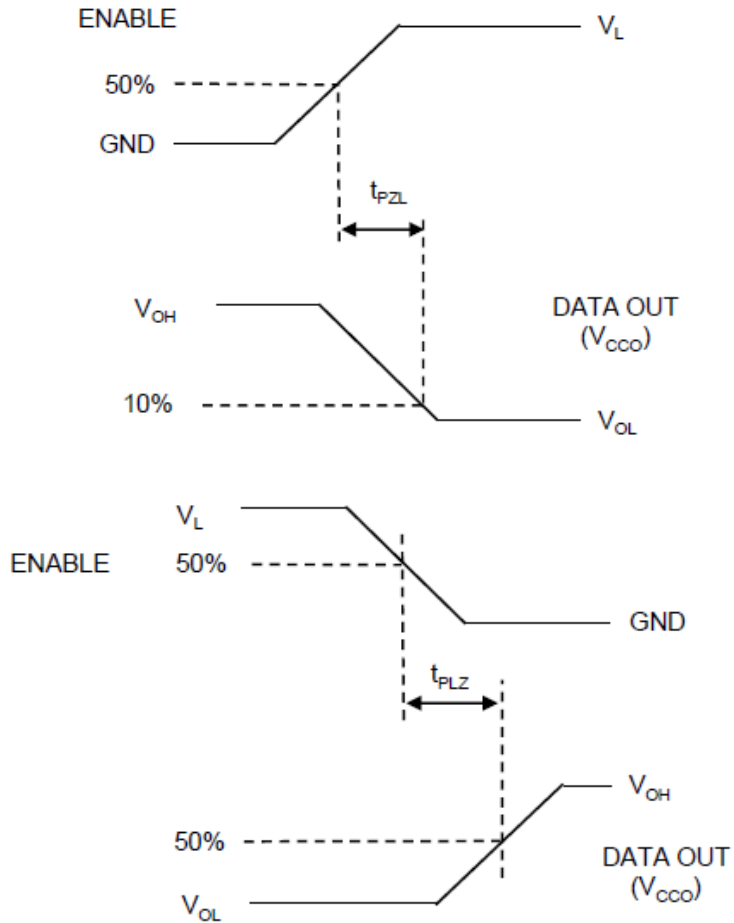


Figure 7. Definition of Output Tri-State Times



## APPLICATIONS INFORMATION

### Level Translator Architecture

The NLSX4302E auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages,  $V_L$  and  $V_{CC}$ , which set the logic levels on the input and output sides of the translator. When used to transfer data from the  $V_L$  to the  $V_{CC}$  ports, input signals referenced to the  $V_L$  supply are translated to output signals with a logic level matched to  $V_{CC}$ . In a similar manner, the  $V_{CC}$  to  $V_L$  translation shifts input signals with a logic level compatible to  $V_{CC}$  to an output signal matched to  $V_L$ .

The NLSX4302E consists of two bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions. Each input/output channel requires external pullup resistors.

### Enable Input (EN)

The NLSX4302E has an Enable pin (EN) that can be used to minimize the power consumption of the device

when the transmitter is not transmitting data. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the  $V_L$  supply and has Overvoltage Tolerant (OVT) protection.

### Power Supply Guidelines

The sequencing of the power supplies will not damage the device during the power up operation. In addition, the I/O  $V_{CC}$  and I/O  $V_L$  pins are in the high impedance state if either supply voltage is equal to 0 V. For optimal performance, 0.01  $\mu$ F to 0.1  $\mu$ F decoupling capacitors should be used on the  $V_L$  and  $V_{CC}$  power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

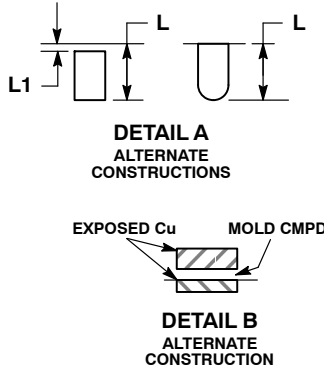
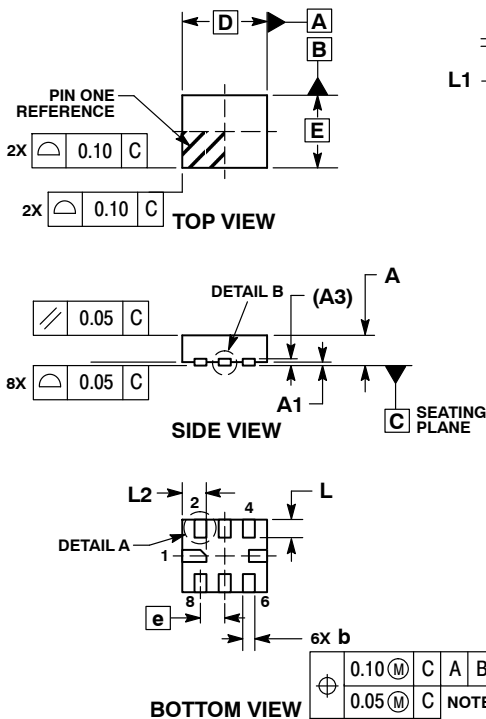
ON Semiconductor®



SCALE 4:1

UQFN8, 1.4x1.2, 0.4P  
CASE 523AS  
ISSUE A

DATE 20 JAN 2012



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.40 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.20	0.40
L1	---	0.15
L2	0.30	0.50

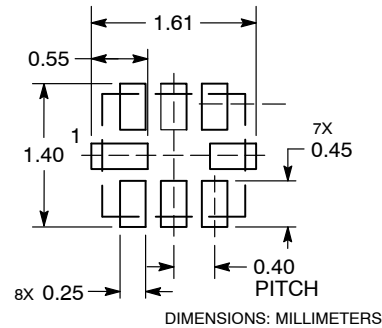
**GENERIC MARKING DIAGRAM\***



X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON58906E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UQFN8, 1.4X1.2, 0.4P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative