

NLSX4373

2ビット20 Mb/sデュアル電源レベル変換器

NLSX4373は、2ビットの構成可能なデュアル電源双方向自動センス変換器で、方向制御ピンは不要です。V_{CC} I/OおよびV_L I/Oポートは、それぞれ2種類の電源レールV_{CC}およびV_Lを追跡するように設計されています。V_{CC}電源レールは1.5 V~5.5 Vの範囲で構成可能で、V_L電源レールは1.5 V~5.5 Vの範囲で構成可能です。これによって、V_L側の電圧ロジック信号をV_{CC}側で、より低い電圧、高い電圧、または同じ値の電圧ロジック信号に変換したり、その逆に変換することができます。

NLSX4373変換器は、オープンドレイン出力を備えており、I/Oラインに10 kΩのプルアップ抵抗が内蔵されています。内蔵プルアップ抵抗を使用して、I/OラインをV_LまたはV_{CC}のいずれかにプルアップします。NLSX4373はI²C通信バスなどのオープンドレイン・アプリケーションに最適です。

特長

- V_LをV_{CC}に対して、より低く、高く、等しくすることが可能
- 広いV_{CC}動作範囲：1.5 V~5.5 V
広いV_L動作範囲：1.5 V~5.5 V
- 20 Mb/s保証データ・レートの高速度
- 低ビット間スキュー
- イネーブル入力およびI/Oラインは、5.5 Vまでの過電圧トレラント(OVT)を装備
- 非優先パワーアップ・シーケンス
- 内蔵10 kΩプルアップ抵抗
- 小型パッケージ：UDFN8、SO-8、Micro8
- 車載向け、および場所と制御の変更を必要とする他のアプリケーション向けNLVプリフィックス; AEC-Q100規格、PPAP*
- 鉛フリー・パッケージ

代表的アプリケーション

- I²C、SMBus、PMBus
- 低電圧ASICレベル変換
- 携帯電話、PDA、カメラ

重要情報

- 全ピンにESD保護
- 人体モデル(HBM) > 7000 V



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MARKING DIAGRAMS



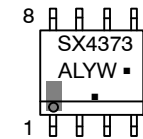
UDFN8
MU SUFFIX
CASE 517AJ



VF = Specific Device Code
M = Date Code
▪ = Pb-Free Package



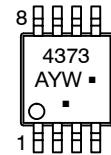
SO-8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package



Micro8™
DM SUFFIX
CASE 846A



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

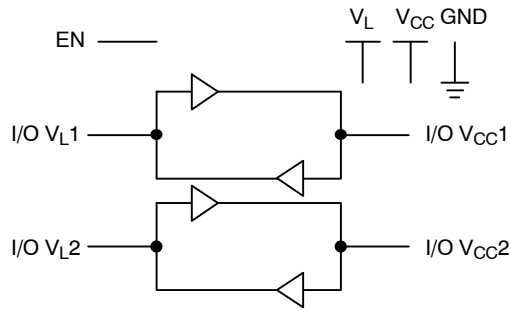
ORDERING INFORMATION

Device	Package	Shipping†
NLSX4373MUTAG	UDFN8 (Pb-Free)	3000/Tape & Reel
NLVSX4373MUTAG*	UDFN8 (Pb-Free)	3000/Tape & Reel
NLSX4373DR2G	SO-8 (Pb-Free)	2500/Tape & Reel
NLVSX4373DR2G*	SO-8 (Pb-Free)	2500/Tape & Reel
NLSX4373DMR2G	Micro8 (Pb-Free)	4000/Tape & Reel

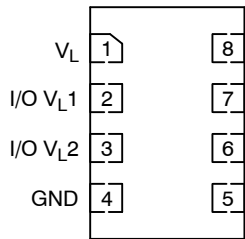
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NLSX4373

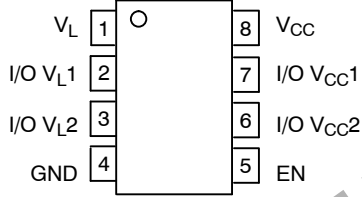
LOGIC DIAGRAM



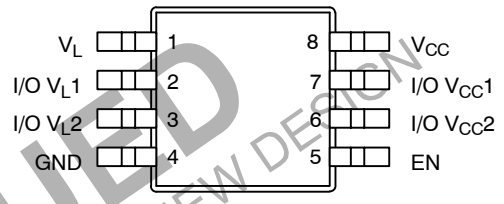
PIN ASSIGNMENTS



UDFN8
(Top View)



SOIC-8
(Top View)



Micro8
(Top View)

PIN ASSIGNMENT

Pins	Description
V _{CC}	V _{CC} Input Voltage
V _L	V _L Input Voltage
GND	Ground
EN	Output Enable
I/O V _{CCn}	V _{CC} I/O Port, Referenced to V _{CC}
I/O V _{Ln}	V _L I/O Port, Referenced to V _L

FUNCTION TABLE

EN	Operating Mode
L	Hi-Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	High-side DC Supply Voltage	-0.3 to +7.0		V
V _L	High-side DC Supply Voltage	-0.3 to +7.0		V
I/O V _{CC}	V _{CC} -Referenced DC Input/Output Voltage	-0.3 to (V _{CC} + 0.3)		V
I/O V _L	V _L -Referenced DC Input/Output Voltage	-0.3 to (V _L + 0.3)		V
V _{EN}	Enable Control Pin DC Input Voltage	-0.3 to +7.0		V
I _{I/O_SC}	Short-Circuit Duration (I/O V _L and I/O V _{CC} to GND)	40	Continuous	mA
T _{STG}	Storage Temperature	-65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

(参考訳)

最大定格を超えるストレスは、デバイスにダメージを与える危険性があります。最大定格は、ストレス印加に対してのみであり、推奨動作条件を超えての機能的動作に関して意図するものではありません。推奨動作条件を超えてのストレス印加は、デバイスの信頼性に影響を与える危険性があります。

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	High-side Positive DC Supply Voltage	1.5	5.5	V
V _L	High-side Positive DC Supply Voltage	1.5	5.5	V
V _{EN}	Enable Control Pin Voltage	GND	5.5	V
V _{IO}	Enable Control Pin Voltage	GND	5.5	V
T _A	Operating Temperature Range	-40	+85	°C

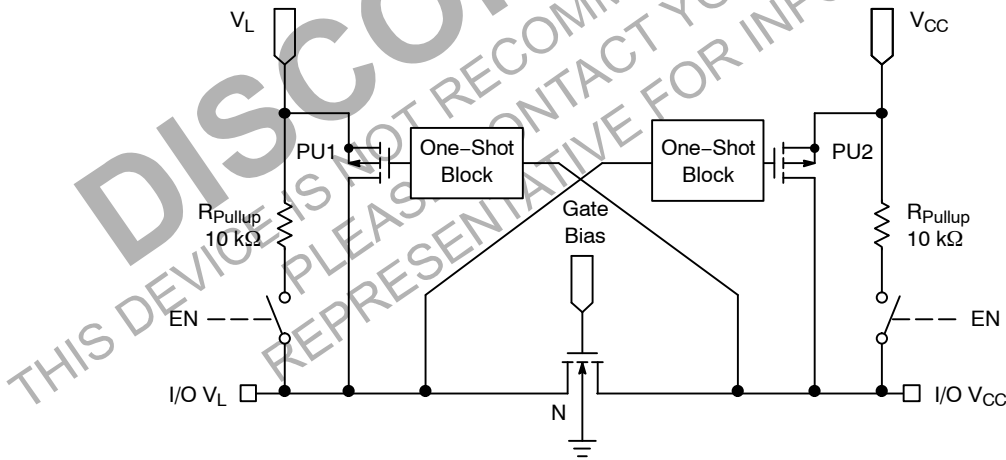


Figure 1. Block Diagram (1 I/O Line)

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 1.5\text{ V to }5.5\text{ V}$ and $V_L = 1.5\text{ V to }5.5\text{ V}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	-40°C to +85°C			Unit
			Min	Typ (Notes 1, 2)	Max	
V_{IHC}	I/O V_{CC} Input HIGH Voltage		$V_{CC} - 0.4$	-	-	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		-	-	0.15	V
V_{IHL}	I/O V_L Input HIGH Voltage		$V_L - 0.2$	-	-	V
V_{ILL}	I/O V_L Input LOW Voltage		-	-	0.15	V
V_{IH}	Control Pin Input HIGH Voltage		$V_L - 0.2$	-	-	V
V_{IL}	Control Pin Input LOW Voltage		-	-	0.15	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} Source Current = 20 μA	$2/3 * V_{CC}$	-	-	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} Sink Current = 20 μA	-	-	$1/3 * V_{CC}$	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L Source Current = 20 μA	$2/3 * V_L$	-	-	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L Sink Current = 20 μA	-	-	$1/3 * V_L$	V
I_{QVCC}	V_{CC} Supply Current	I/O V_{CC} and I/O V_L Unconnected, $V_{EN} = V_L$	-	0.5	2.0	μA
I_{QVL}	V_L Supply Current	I/O V_{CC} and I/O V_L Unconnected, $V_{EN} = V_L$	-	0.3	1.5	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, $V_{EN} = \text{GND}$	-	0.1	1.0	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, $V_{EN} = \text{GND}$	-	0.1	1.0	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	$T_A = +25^\circ\text{C}$	-	0.1	1.0	μA
R_{PU}	Pullup Resistor I/O V_L and V_{CC}	$T_A = +25^\circ\text{C}$	-	10	-	$\text{k}\Omega$

1. Typical values are for $V_{CC} = +2.8\text{ V}$, $V_L = +1.8\text{ V}$ and $T_A = +25^\circ\text{C}$.

2. All units are production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

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TIMING CHARACTERISTICS – RAIL-TO-RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$)

Symbol	Parameter	Test Conditions	-40°C to +85°C (Notes 3 and 4)			Unit
			Min	Typ	Max	

$V_L = 1.5 \text{ V}$, $V_{CC} = 5.5 \text{ V}$

t_{RVCC}	I/O V_{CC} Risettime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				20	ns
t_{RVL}	I/O V_L Risettime				30	ns
t_{FVL}	I/O V_L Falltime				10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				20	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

$V_L = 1.8 \text{ V}$, $V_{CC} = 2.8 \text{ V}$

t_{RVCC}	I/O V_{CC} Risettime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				15	ns
t_{RVL}	I/O V_L Risettime				25	ns
t_{FVL}	I/O V_L Falltime				10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

$V_L = 2.5 \text{ V}$, $V_{CC} = 3.6 \text{ V}$

t_{RVCC}	I/O V_{CC} Risettime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				10	ns
t_{RVL}	I/O V_L Risettime				15	ns
t_{FVL}	I/O V_L Falltime				10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

$V_L = 2.8 \text{ V}$, $V_{CC} = 1.8 \text{ V}$

t_{RVCC}	I/O V_{CC} Risettime				25	ns
t_{FVCC}	I/O V_{CC} Falltime				10	ns
t_{RVL}	I/O V_L Risettime				20	ns
t_{FVL}	I/O V_L Falltime				15	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

3. Typical values are for $V_{CC} = +3.3 \text{ V}$, $V_L = +1.8 \text{ V}$ and $T_A = +25^\circ\text{C}$.

4. All units are production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

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TIMING CHARACTERISTICS – RAIL-TO-RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$)

Symbol	Parameter	Test Conditions	-40°C to +85°C (Notes 3 and 4)			Unit
			Min	Typ	Max	
$V_L = 3.6 \text{ V}$, $V_{CC} = 2.5 \text{ V}$						
t_{RVCC}	I/O V_{CC} Risetime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				10	ns
t_{RVL}	I/O V_L Risetime				15	ns
t_{FVL}	I/O V_L Falltime				15	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

$V_L = 5.5 \text{ V}$, $V_{CC} = 1.5 \text{ V}$

t_{RVCC}	I/O V_{CC} Risetime				30	ns
t_{FVCC}	I/O V_{CC} Falltime				10	ns
t_{RVL}	I/O V_L Risetime				15	ns
t_{FVL}	I/O V_L Falltime				20	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				20	ns
t_{PPSKEW}	Part-to-Part Skew				5	nS
	Maximum Data Rate		20			Mb/s

3. Typical values are for $V_{CC} = +3.3 \text{ V}$, $V_L = +1.8 \text{ V}$ and $T_A = +25^\circ\text{C}$.

4. All units are production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS – OPEN DRAIN DRIVING CONFIGURATIONS

(I/O test circuit of Figures 4 and 5, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$)

Symbol	Parameter	Test Conditions	-40°C to +85°C (Notes 5 and 6)			Unit
			Min	Typ	Max	
$+1.5 \leq V_L \leq V_{CC} \leq +5.5 \text{ V}$						
t_{RVCC}	I/O V_{CC} Risetime				400	ns
t_{FVCC}	I/O V_{CC} Falltime				50	ns
t_{RVL}	I/O V_L Risetime				400	ns
t_{FVL}	I/O V_L Falltime				60	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				1000	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				1000	ns
t_{PPSKEW}	Part-to-Part Skew				50	nS
MDR	Maximum Data Rate		2			Mb/s

5. Typical values are for $V_{CC} = +3.3 \text{ V}$, $V_L = +1.8 \text{ V}$ and $T_A = +25^\circ\text{C}$.

6. All units are production tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range are guaranteed by design.

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TEST SETUPS

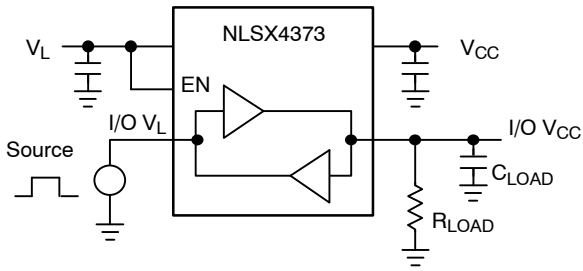


Figure 2. Rail-to-Rail Driving I/O V_L

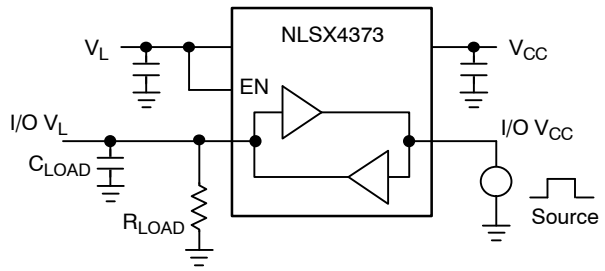


Figure 3. Rail-to-Rail Driving I/O V_{CC}

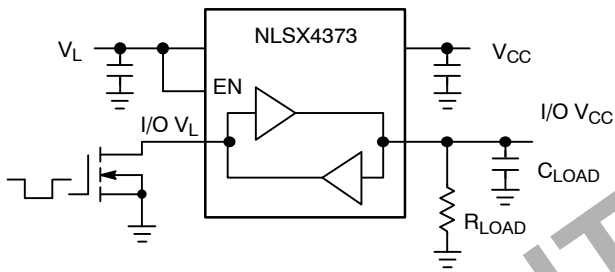


Figure 4. Open-Drain Driving I/O V_L

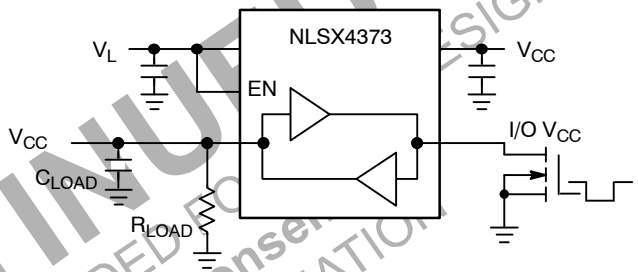


Figure 5. Open-Drain Driving I/O V_{CC}

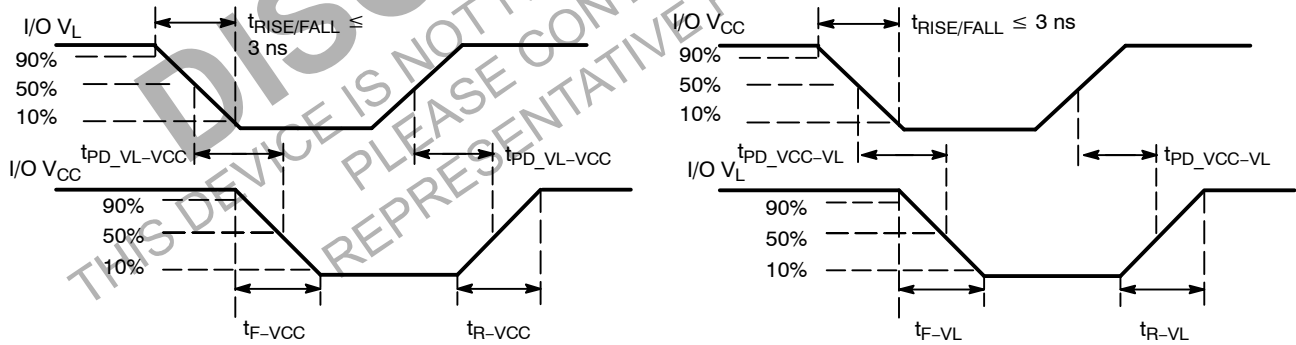
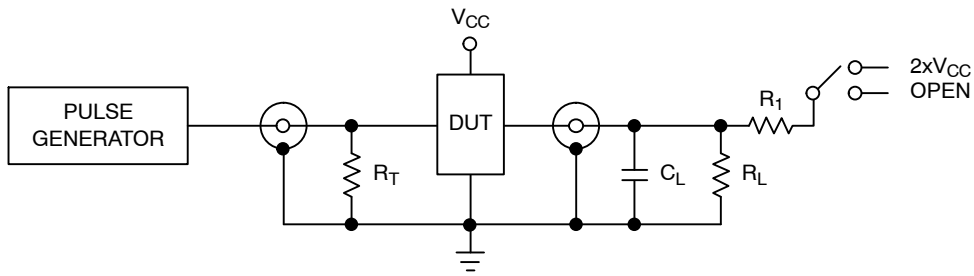


Figure 6. Definition of Timing Specification Parameters

NLSX4373



Test	Switch
t_{PZH} , t_{PHZ}	Open
t_{PZL} , t_{PLZ}	$2 \times V_{CC}$

$C_L = 15 \text{ pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 50 \text{ k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 7. Test Circuit for Enable/Disable Time Measurement

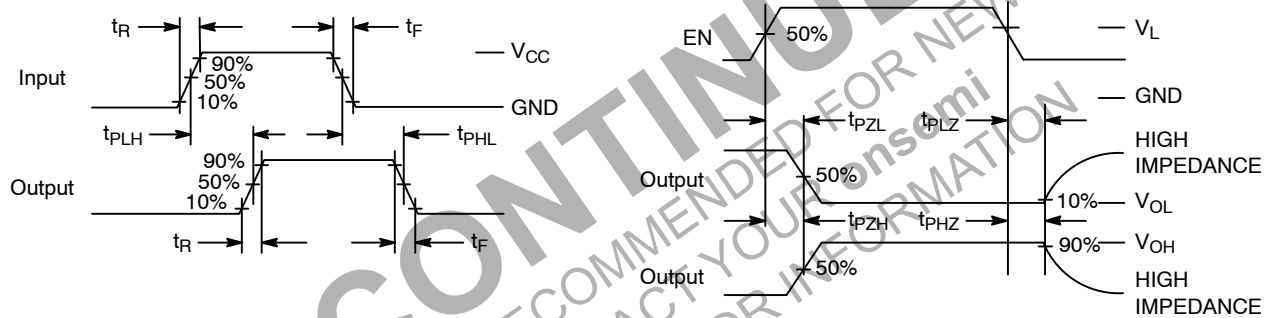


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

アプリケーション情報

レベル変換アーキテクチャ

NLSX4373自動検知変換器は、双方向電圧レベル・シフトを提供し、複数電源電圧システムでデータを転送します。このデバイスには V_L と V_{CC} の2つの電源電圧があり、変換器の入力側と出力側でロジック・レベルを設定します。 V_L ポートから V_{CC} ポートへのデータ転送に使用するとき、 V_L 電源を基準とする入力信号が V_{CC} に一致するロジック・レベルの出力信号に変換されます。同様な方法で、 V_{CC} から V_L への変換によって、 V_{CC} に対応するロジック・レベルの入力信号が V_L に一致する出力信号にシフトされます。

NLSX4373は、方向ピンを必要とせず、データ・フローの方向を単独で決定する2つの双方向チャネルで構成されています。ワンショット回路を使用して、入力信号の立ち上がりまたは立ち下がりを検出します。また、ワンショットによって、ハイからローおよびローからハイへの遷移に対する出力信号の上昇および下降時間を短縮します。

各入力/出力チャネルには、10 k Ω の内部プルアップ抵抗があります。プルアップ抵抗の抵抗値は、内部10 k Ω 抵抗と並列に外付け抵抗を接続して減らすことができます。

入力ドライバ要件

オープン・ドレイン出力の立ち上がり(t_R)および立ち下がり(t_F)タイミング・パラメータは、プルアップ抵抗の大きさによって異なります。また、伝播時間(t_{PD})、スキュー(t_{PSKEW})および最大データ・レートは、変換器に接続されたデバイスのインピーダ

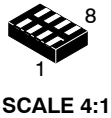
ンスによって決まります。データ・シートに記載されたタイミング・パラメータは、変換器に接続されたドライバの出力インピーダンスが50 k Ω 未満と仮定しています。

イネーブル入力 (EN)

NLSX4373には、I/Oピンでトライ・ステート動作を提供するイネーブル・ピン(EN)があります。イネーブル・ピンをロー・ロジック・レベルにドライブすると、デバイスの消費電力が減少し、I/O V_{CC} ピンとI/O V_L ピンがハイ・インピーダンス状態になります。ENピンがロジック・ハイ信号と等しいとき、通常の変換動作が行われます。ENピンは V_L 電源を基準としており、過電圧トレラント(OVT)保護を備えています。

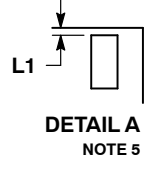
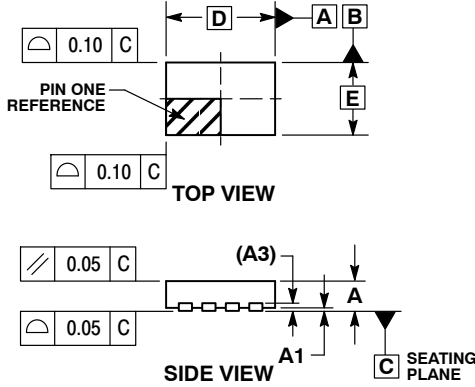
電源ガイドライン

通常動作中、電源電圧 V_L は、 V_{CC} に対して、より高く、より低く、または等しくすることができます。電源シーケンシングが、起動動作中のデバイスに損傷を与えることはありません。最適な性能を得るには、 V_L および V_{CC} 電源ピンに0.01 μ F~0.1 μ Fのデカップリング・コンデンサを使用する必要があります。セラミック・コンデンサは、PCBの電圧ラインからグラウンド・プレーン上のノイズ信号をフィルタおよびバイパスするための設計上の賢明な選択です。コンデンサを電源ピンやグラウンド・ピンのできるだけ近くに配置すると、PCB接続トレースが短くなるのに加えて、ノイズ耐性が大きくなります。



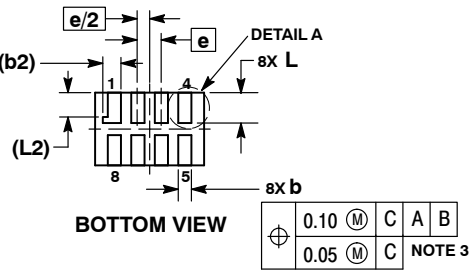
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CASE 517AJ
ISSUE O

DATE 08 NOV 2006

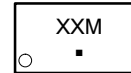


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
 4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
 5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127	REF
b	0.15	0.25
b2	0.30	REF
D	1.80	BSC
E	1.20	BSC
e	0.40	BSC
L	0.45	0.55
L1	0.00	0.03
L2	0.40	REF

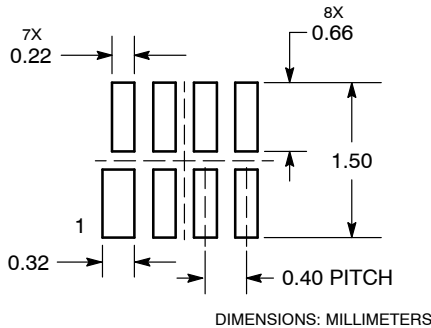


GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

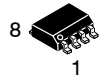
MOUNTING FOOTPRINT SOLDERMASK DEFINED



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	UDFN8 1.8X1.2, 0.4P	PAGE 1 OF 1

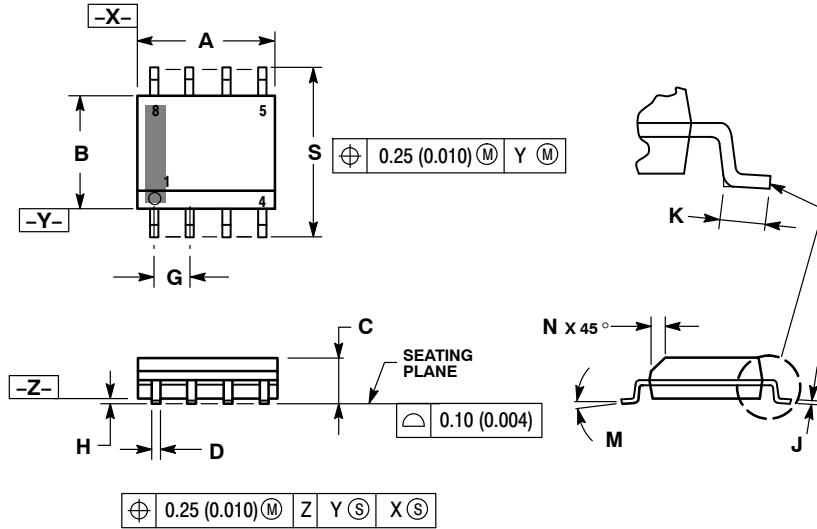
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SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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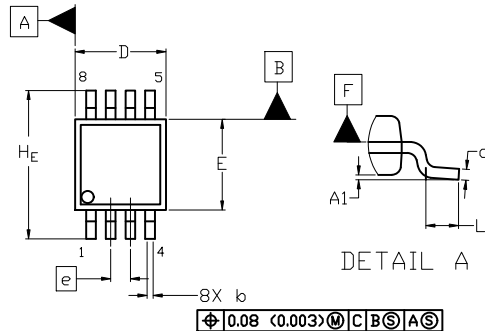
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SCALE 2:1

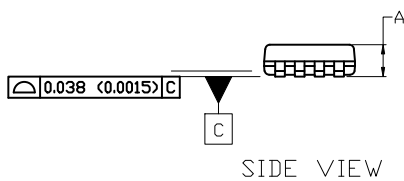
Micro8
CASE 846A-02
ISSUE K

DATE 16 JUL 2020

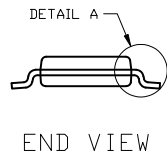


TOP VIEW

NOTE 3



SIDE VIEW

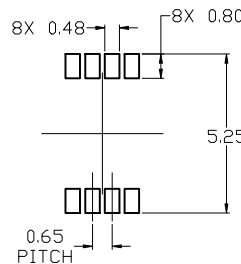


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$ (0.003) M C B S A S

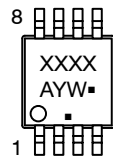


RECOMMENDED MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H_E</i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70

For additional information on our Pb-Free strategy and soldering details, please download the [DN Semiconductor Soldering and Mounting Techniques Reference Manual, SLDERRM/D](#).

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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