

Notes:

- ① Material: UL recognized component ZPMV2, minimum 94V-1, relative permittivity 3.9
- ② Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer $1 \div 4 \text{ } \mu\text{m}$, gold layer $0.076 \div 0.2 \text{ } \mu\text{m}$
- ③ All gerber files generated as a top view
4. Fabricate according IPC-A-600
5. Non-conductive epoxy ink recommended for silkscreen
6. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
7. All holes diameter refer to final diameter after eventual plating

Gerber and drill file extensions table

Gerber files	
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	Top layer
.GBL	Bottom layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Bottom side silkscreen
.GM1	Board outline
Drill files	
.TXT	Round holes; Layer pair: Top layer to Bottom layer
.TXT	Slot holes; Layer pair: Top layer to Bottom layer

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Layer Stack

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.0356mm(1.400mil)		Signal	GTL
Core		0.8000mm(31.496mil)	Isola IS400/SYS1000-2: 0.8mm +/-10%	Dielectric	
Copper	Bottom Layer	0.0356mm(1.400mil)		Signal	GBL
Surface Material	Bottom Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP
Total thickness: 0.8914mm(35.096mil)					

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<i>Layer stack details</i>		Fabrication document	Sheet 2 / 12
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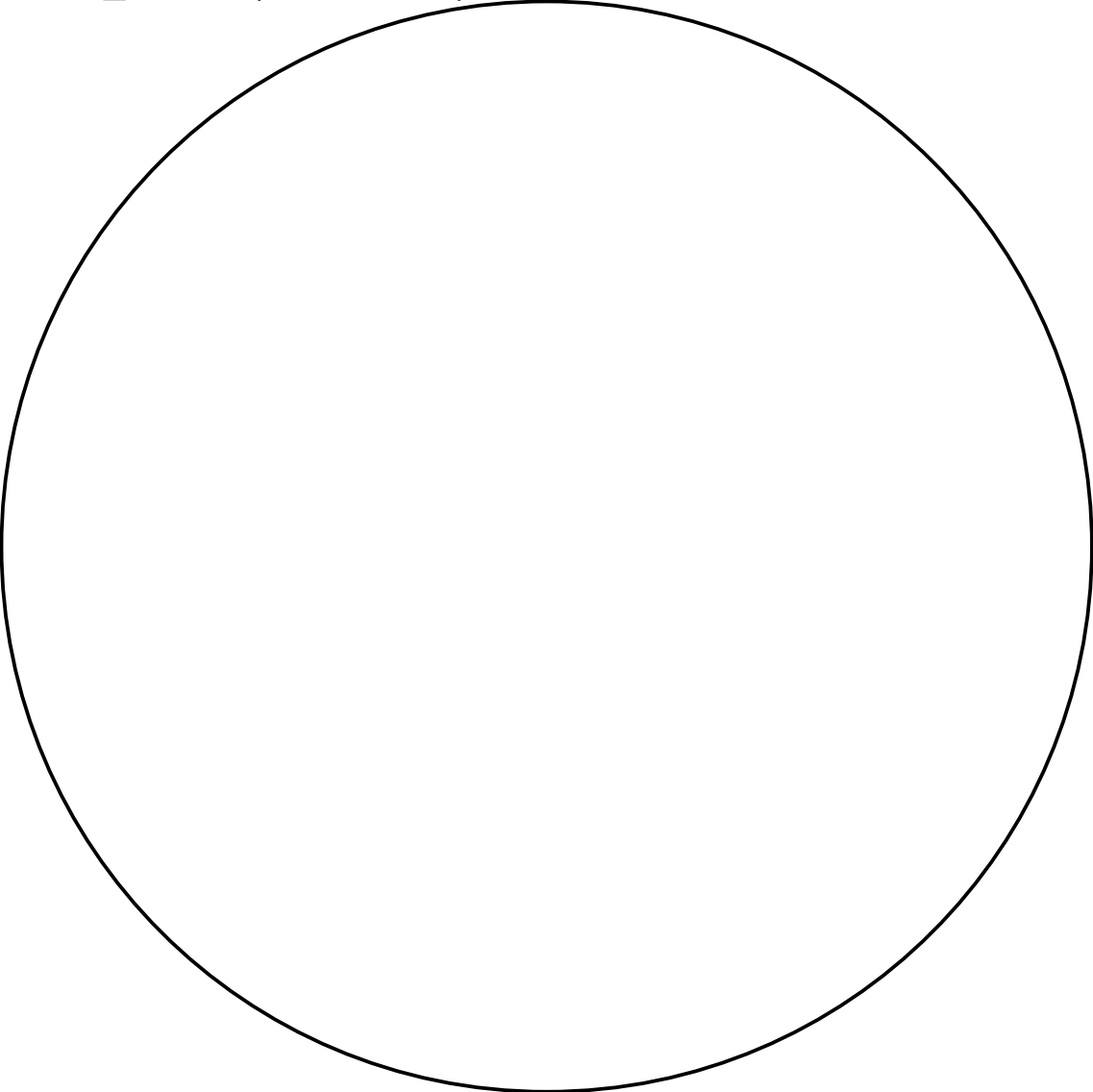
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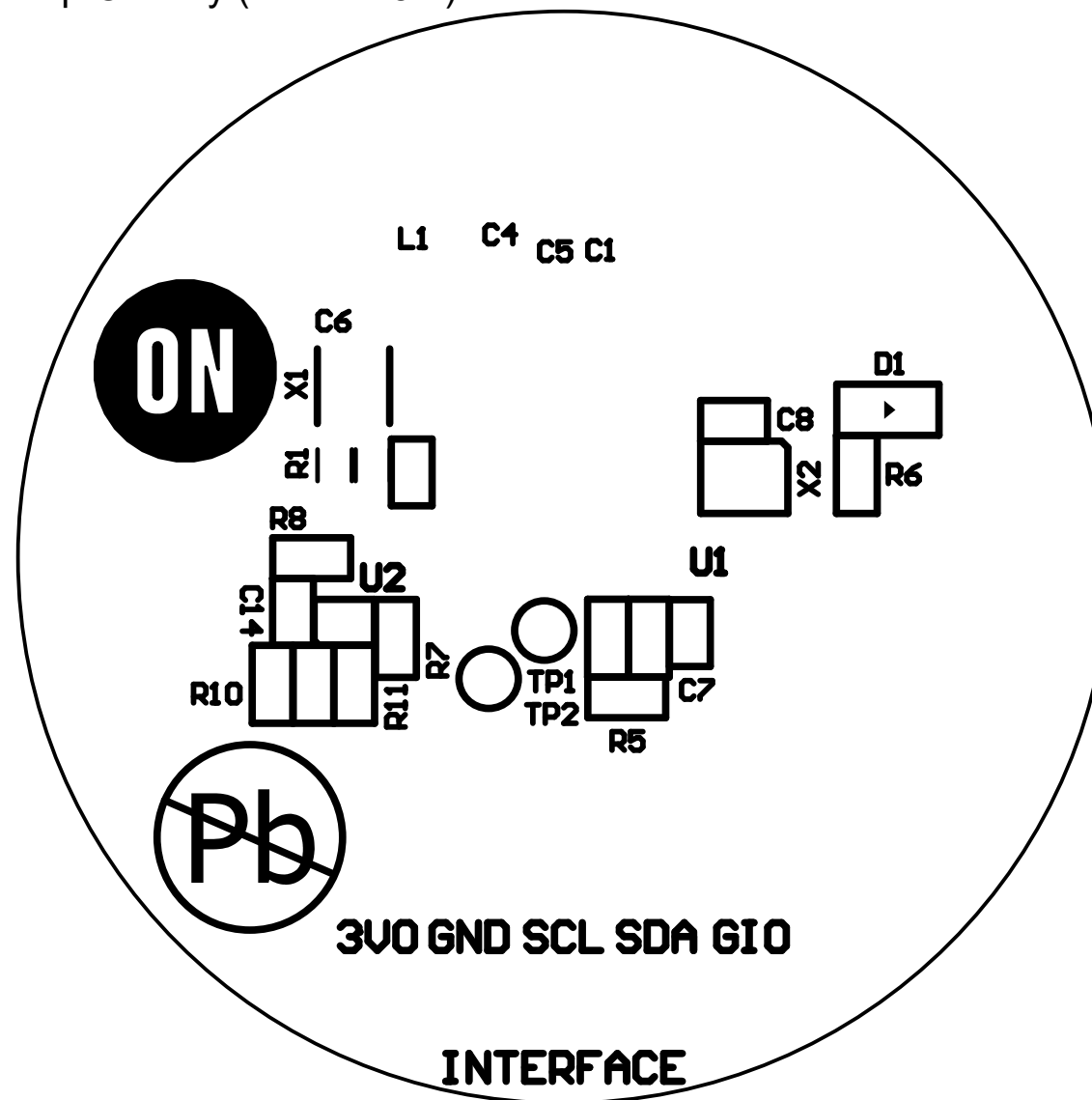
Board_outline (Scale = 5:1)



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<i>Board outline definition - top view 5:1</i>		Fabrication document	Sheet 3 / 12
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Top Overlay (Scale = 5:1)



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Top side silkscreen

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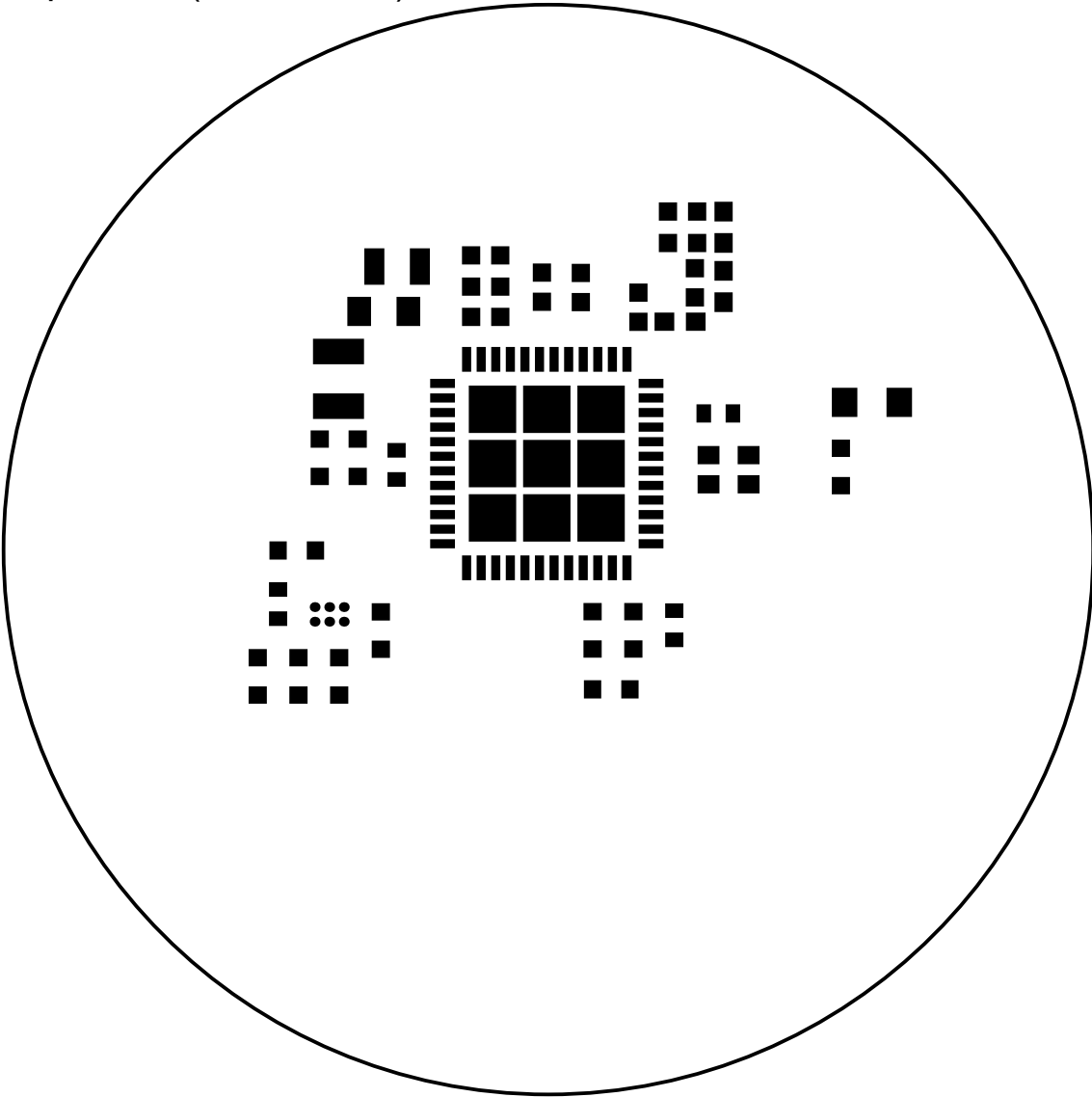
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Top Paste (Scale = 5:1)



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<i>Top side solder paste</i>		Fabrication document	Sheet 5 / 12
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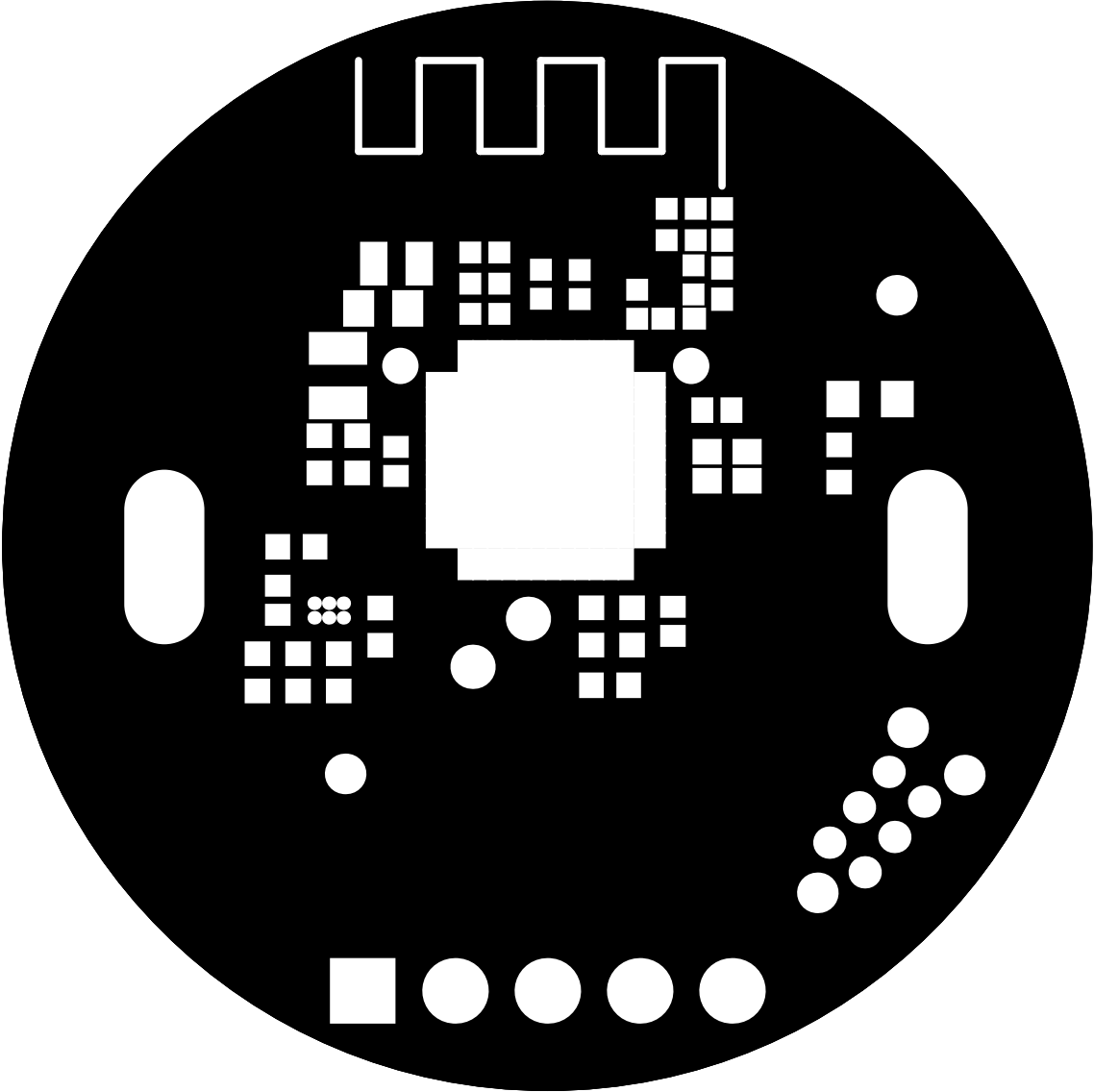
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Top Solder (Scale = 5:1)



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<i>Top side solder mask</i>		Fabrication document	Sheet 6 / 12
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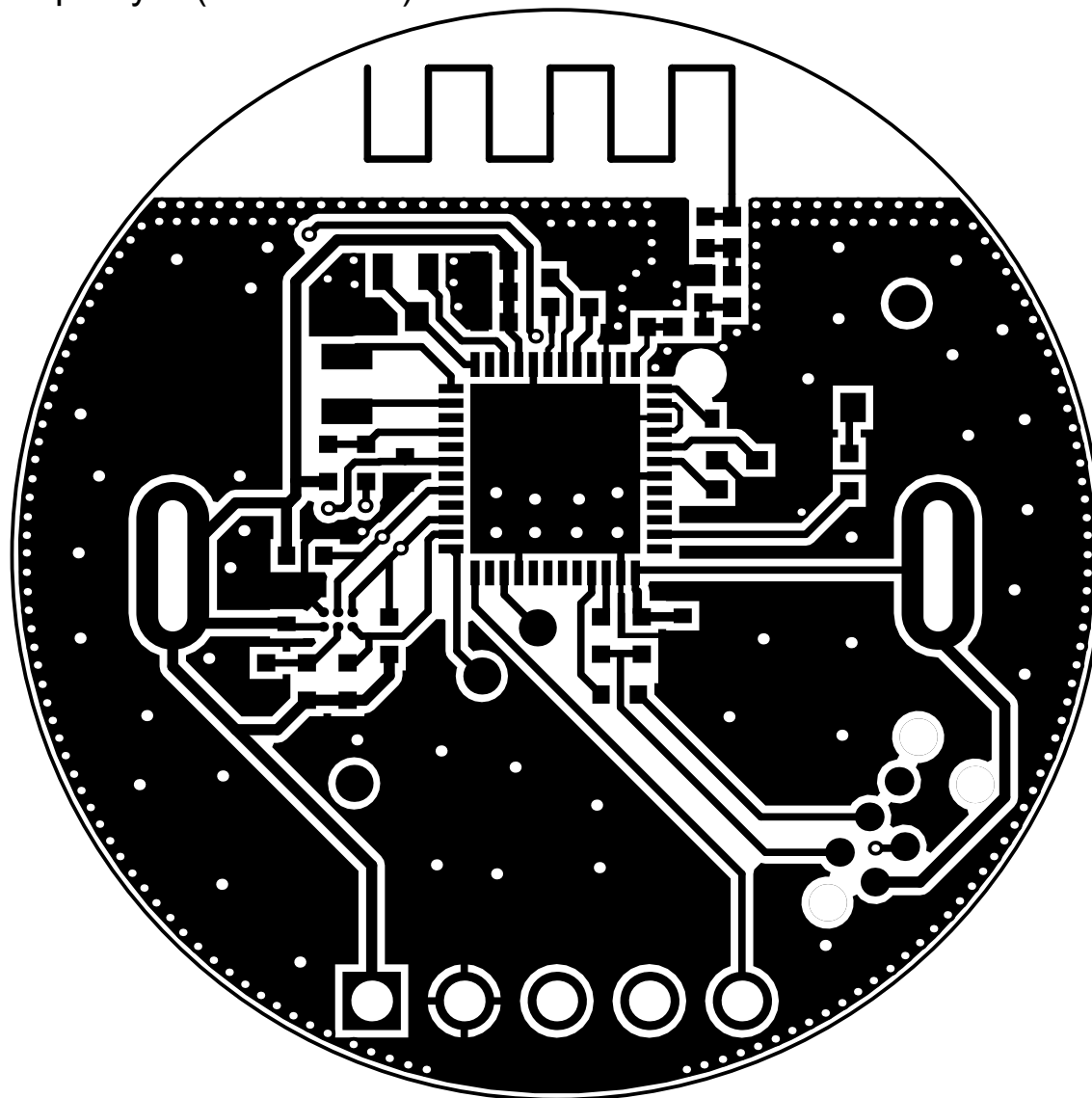
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Top Layer (Scale = 5:1)



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Top layer

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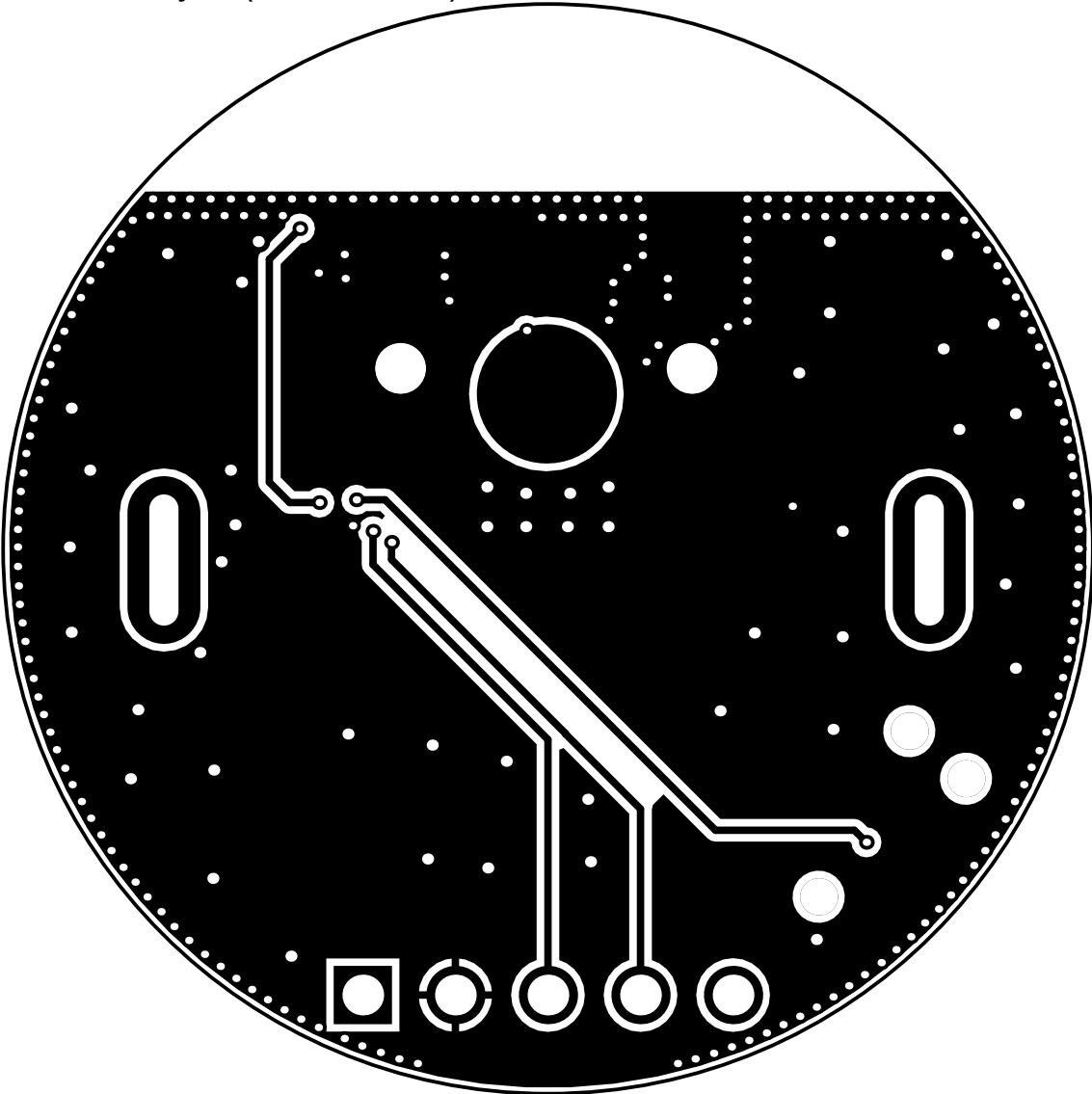
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Bottom Layer (Scale = 5:1)



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Bottom layer		Fabrication document	Sheet 8 / 12
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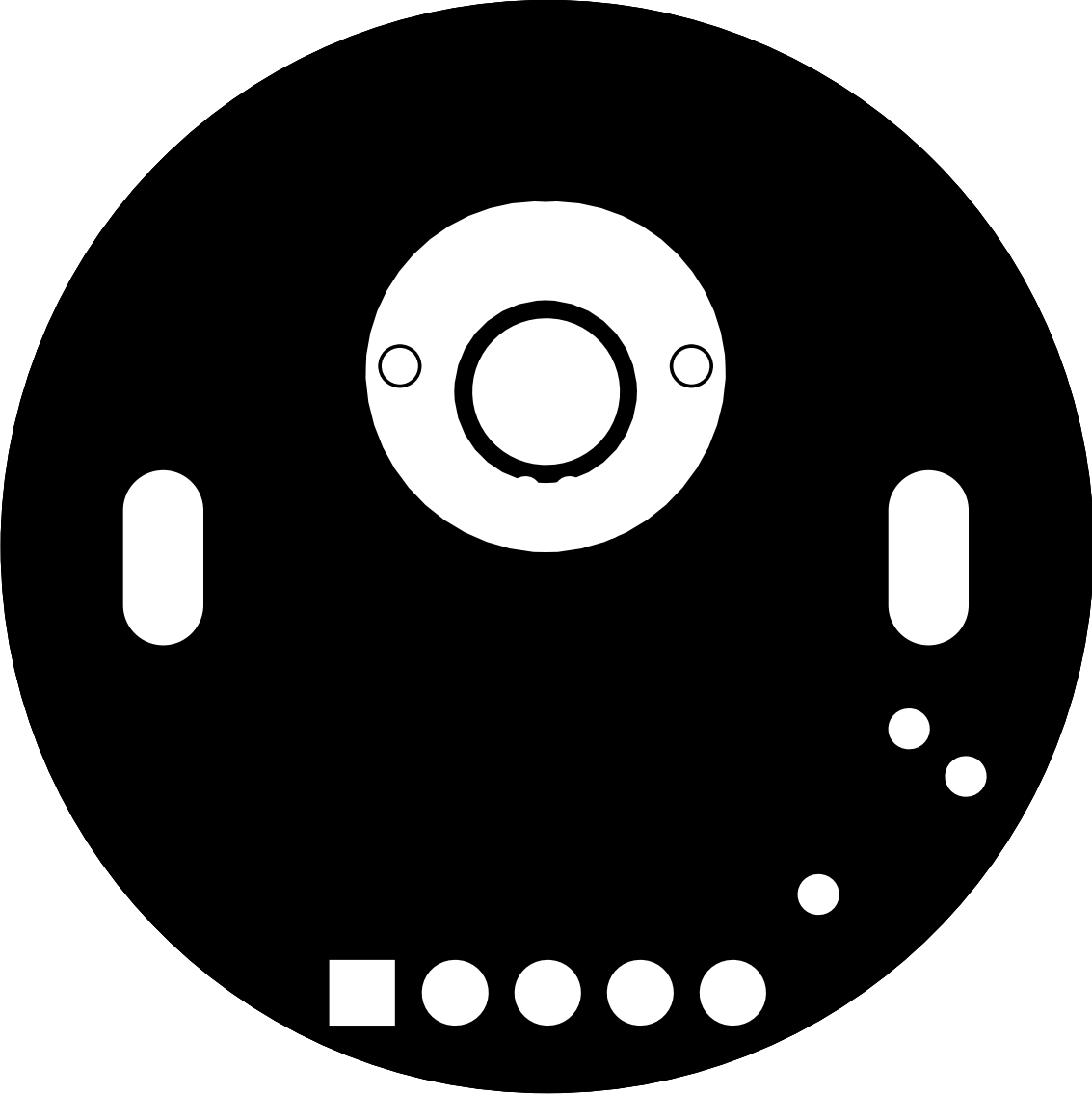
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Bottom Solder (Scale = 5:1)



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<i>Bottom side solder mask</i>		Fabrication document	Sheet 9 / 12
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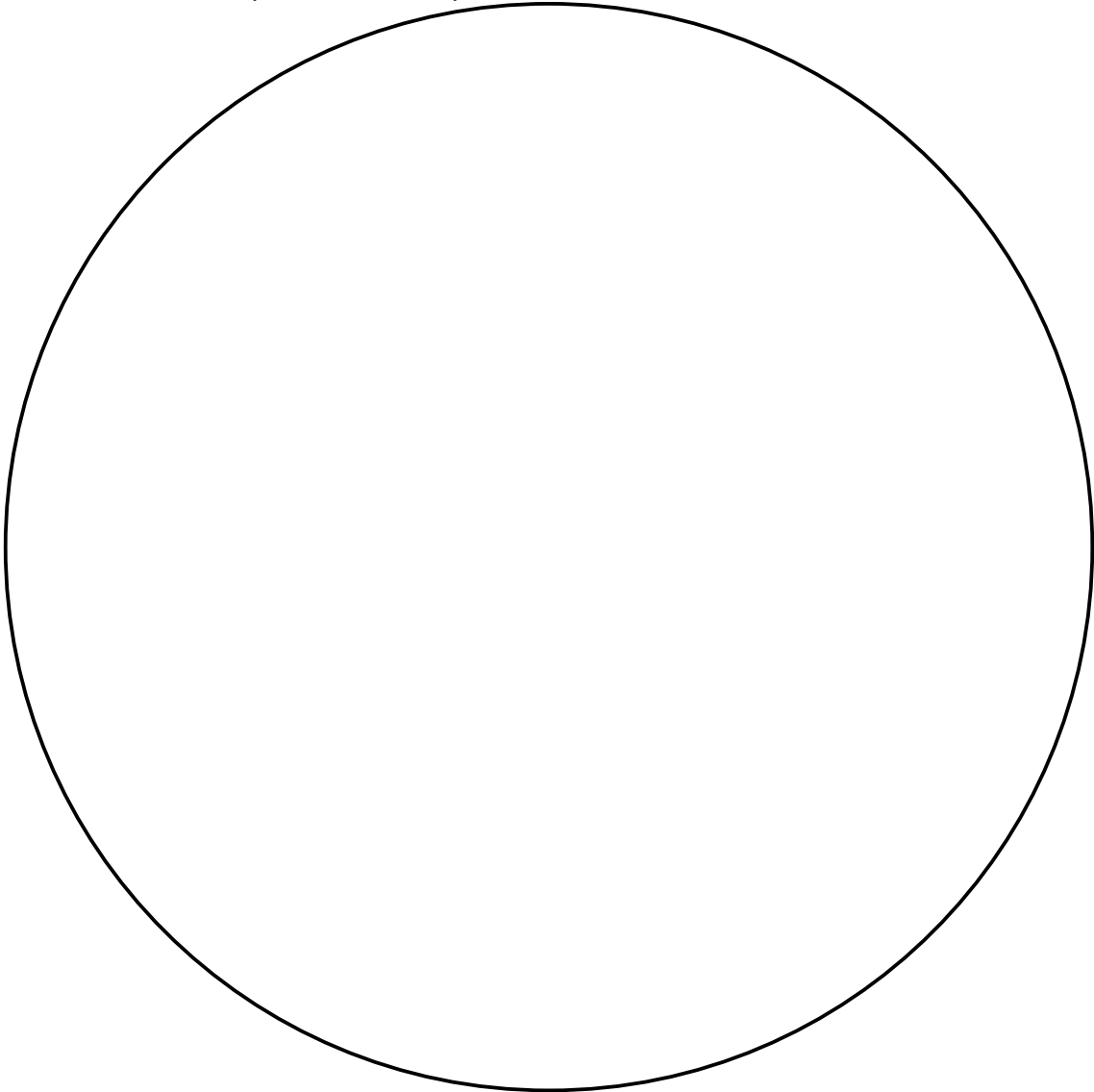
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Bottom Paste (Scale = 5:1)



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<i>Bottom side solder paste</i>		Fabrication document	Sheet 10 / 12
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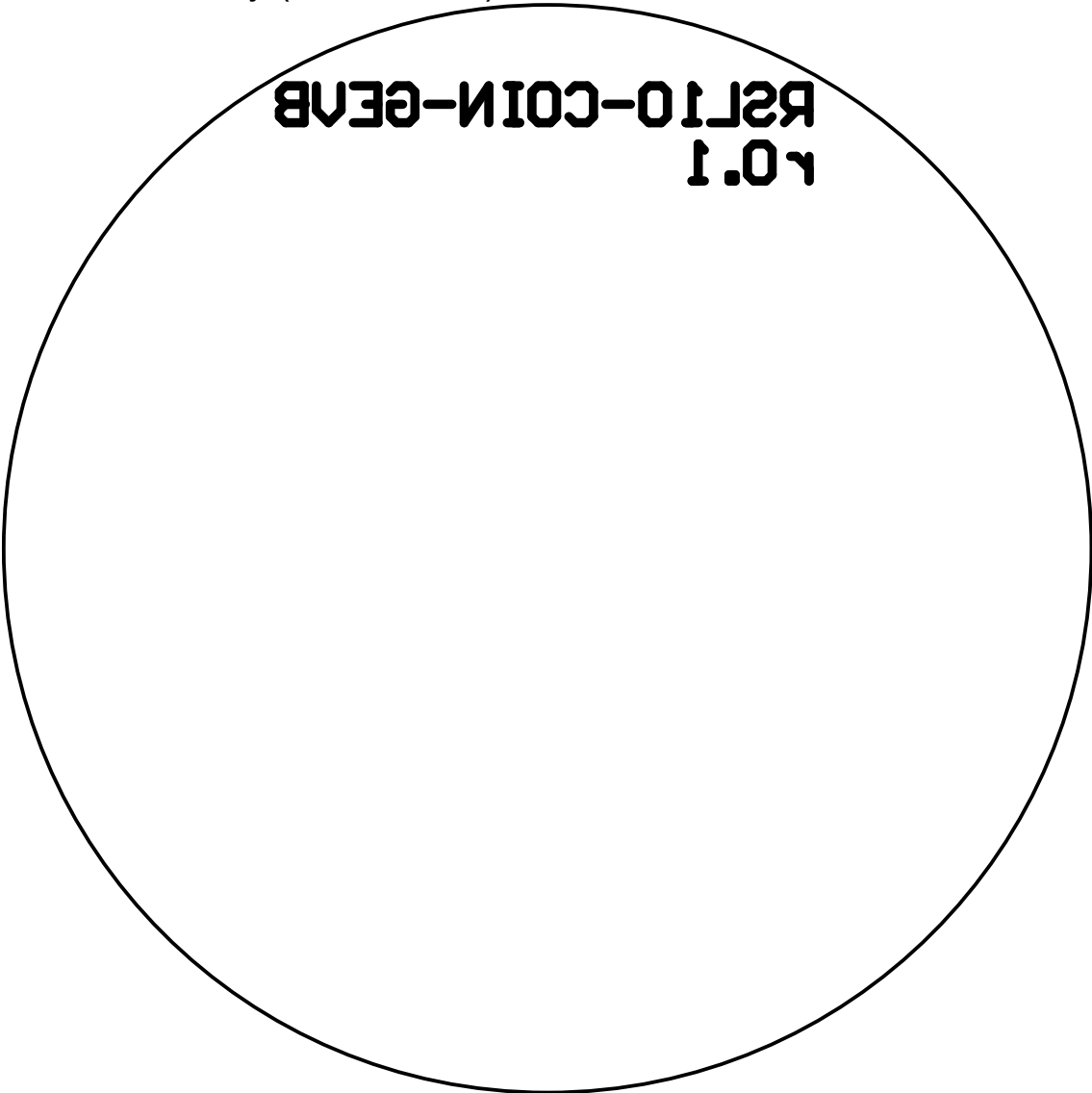
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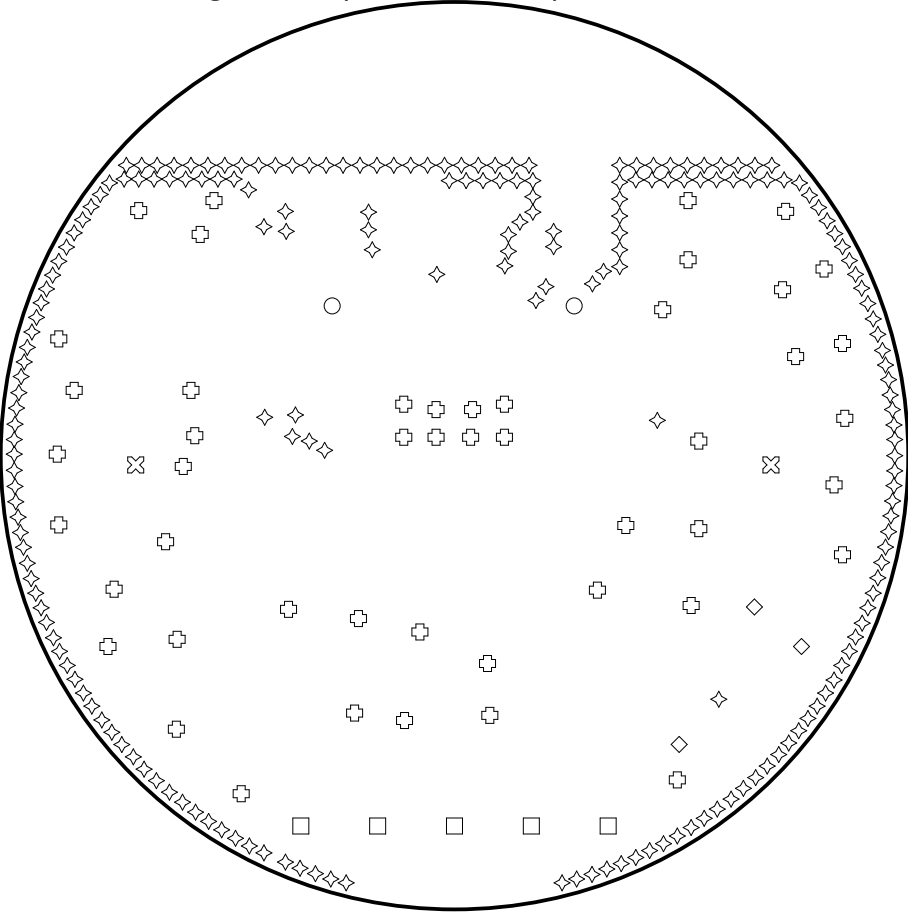
Bottom Overlay (Scale = 5:1)



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<i>Bottom side silkscreen</i>		Fabrication document	Sheet 11 / 12
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Drill Drawing View (Scale = 4:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
◇	205	0.203mm(8mil)	Plated	Top Layer - Bottom Layer	Via	v16h8_t
⊕	48	0.305mm(12mil)	Plated	Top Layer - Bottom Layer	Via	(Mixed)
⊗	2	0.800mm(31mil)	Plated	Top Layer - Bottom Layer	Pad	r200_460h80_360r100
○	2	1.000mm(39mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c0hn100
◇	3	1.016mm(40mil)	Non-Plated	Top Layer - Bottom Layer	Pad	c102hn102m107
□	5	1.118mm(44mil)	Plated	Top Layer - Bottom Layer	Pad	(Mixed)
265 Total						

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<i>Drill drawing</i>		Fabrication document	Sheet 12 / 12
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