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Designing Asymmetric PWM Half-Bridge Converters with a Current Doubler and Synchronous Rectifier using FSFA-Series Fairchild Power Switches (FPS™)

Introduction

In general, high-frequency operation allows the use of small-sized passive components in switch-mode power supplies (SMPS), though it causes the switching losses to increase in a hard-switching mode. To reduce switching losses at high switching frequencies, many soft-switching techniques have been developed, including load-resonant and zero-voltage-transition techniques.

Load-resonant techniques use a resonant feature of capacitors and inductors during the entire switching period to vary the switching frequency, depending on the input voltage and load current. The change of the switching frequency, i.e. pulse frequency modulation (PFM), makes it difficult to design an SMPS including input filters. Since there is no output inductor for filtering, the clamped voltage across output-rectifying diodes allows designers to select low-voltage-rating diodes. However, the absence of the output inductor burdens the output capacitors when the load current increases, making load-resonant techniques unsuitable for applications with high output current and low output voltage.

On the other hand, zero-voltage-transition techniques use a resonant feature between parasitic components during turn-on and/or turn-off transitions of the switching period. One of the advantages of these techniques is to use the parasitic components, such as the leakage inductance of the main transformer and the output capacitances of the switches, so there is no need to add more external components to achieve soft switching. In addition, these techniques take pulse-width modulation (PWM) up with fixed-switching frequency. Therefore, these are easier to understand, analyze, and design than load-resonant techniques.

Due to its simple configuration and zero-voltage switching (ZVS) characteristic, an asymmetric PWM half-bridge converter is one of the most popular topologies using the zero-voltage-transition technique. In addition, the ripple component of the output current due to an output inductor becomes small enough to be handled by an appropriate output capacitor. Being easy to analyze and design and having an output inductor, it is generally used for applications with high output current and low output voltage (e.g. game console power supplies). To handle the large output current, using a synchronous rectifier in the secondary side is popular to obtain the conduction losses as ohmic losses instead of diode losses. In addition, a current doubler increases the utilization of the main transformer when the output current is high.

Fairchild's FSFA-series of green power switches (FPS™) integrates a PWM controller and MOSFETs specifically designed for asymmetric-controlled topologies with minimal external components. Compared with discrete-PWM-controller-and-MOSFETs solutions, FSFA-series switches can reduce total cost, bill of materials (BOM) list, size, and weight, while simultaneously increasing efficiency, productivity, and system reliability.

This application note describes design considerations of an asymmetric PWM half-bridge converter with current doubler and synchronous rectifier employing FSFA-series switches. It includes a step-by-step design procedure as well as the general features and operational principles of the proposed topology.

1. Operational Principles of a Conventional Asymmetric PWM Half-Bridge Converter

Figure 1 shows a conventional asymmetric PWM half-bridge converter with a center-tapped transformer. While the switch S_1 operates with a duty D, depending on the input voltage and load current, the switch S_2 operates with $1\text{-}D$. During DT_S, $V_{in}\text{-}V_{Cb}$ is applied on the primary side of the transformer and the secondary diode D_1 turns on. The primary current i_{pri} increases since the magnetizing current i_m of the transformer (not illustrated) and the output inductor current i_{Lo} increase together. During $(1\text{-}D)T_S$, V_{Cb} is applied on the transformer and D_2 turns on. The capacitor C_b is not only a voltage source during $(1\text{-}D)T_S$ but also a DC-blocking capacitor to prevent transformer saturation. When the volt·sec balance for the magnetizing inductance of the transformer is applied, the following is obtained:

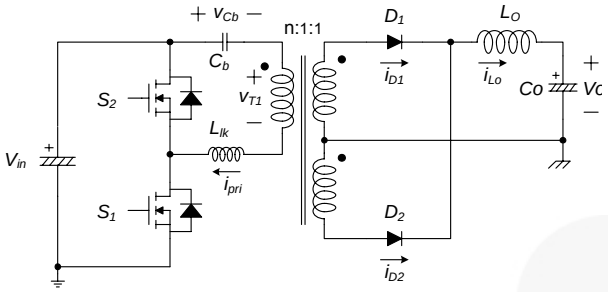


Figure 1. Conventional Asymmetric PWM Half-Bridge Converter with a Center-Tapped Transformer

$$(V_{in} - V_{Cb}) \times D = V_{Cb} \times (1 - D) \quad (1)$$
$$\Rightarrow \quad V_{Cb} = DV_{in}$$

The volt·sec balance for the output inductor yields:

$$\left(\frac{V_{in} - V_{Cb}}{n} - V_O\right) \times D = \left(V_O - \frac{V_{Cb}}{n}\right) \times (1 - D) \quad (2)$$

where n is the turns ratio of the transformer.

Combining Equations (1) and (2), the output voltage is obtained as:

$$V_O = \left(\frac{2D(1-D)}{n}\right) \times V_{in} \quad (3)$$

As can be seen in Figure 2 (the gain curve according to the duty cycle using Equation (3) ignoring turns ratio n), the gain is proportional to the duty cycle up to 50% and inversely proportional to it above 50%. Because of this symmetry, the maximum duty cycle should be restricted up to 50% to regulate the output voltage.

The loss parts of the duty cycle by the leakage inductance are not considered in Equation (3). Figure 3 shows the key waveforms of the conventional asymmetric PWM half-bridge converter illustrated in Figure 1. Since both secondary rectifying diodes conduct, the voltage across the primary side of the transformer becomes zero during $D_{loss1}T_S$ and $D_{loss2}T_S$. As a result, the output voltage is not as high as in Equation (3), which is obtained by averaging, rectifying,

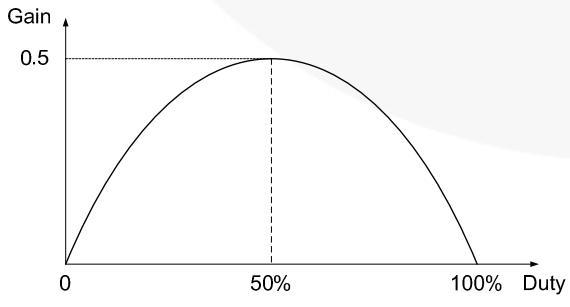


Figure 2. Normalized Gain Curve

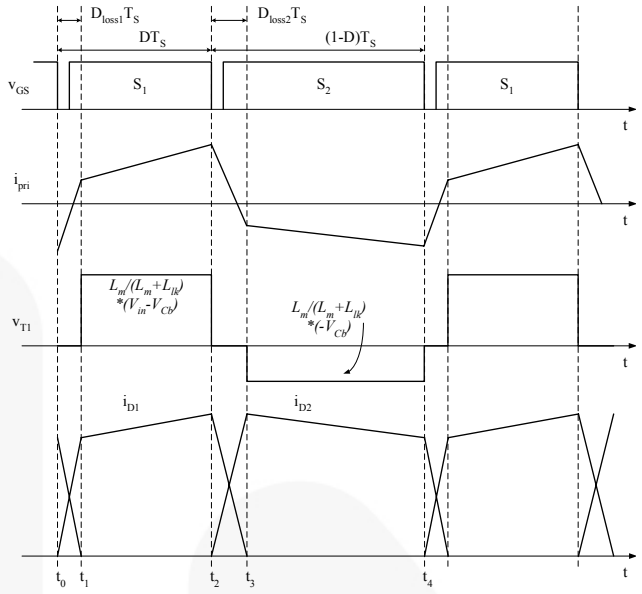


Figure 3. Key Waveforms of the Conventional Asymmetric PWM Half-Bridge Converter

and scaling down v_{T1} by n. In addition, the applied voltage on the primary side of the transformer during powering modes (t_1~t_2 and t_3~t_4) is slightly less than V_{in}–V_{Cb} or –V_{Cb} due to the leakage inductance L_{lk} as shown in Figure 3. Therefore, the output voltage equation could be obtained as:

$$V_O = \left(\frac{L_m}{L_m + L_{lk}}\right)\left(\frac{2D(1-D)V_{in}}{n} - \frac{4I_O L_{lk}}{n^2 T_S}\right) - V_F \quad (4)$$

where I_O is the output load current and V_F is the forward voltage drop of the secondary side-rectifying diodes.

To design the transformer, the magnetizing current must be known. Assume that the magnetizing inductance and the output inductance are high enough for the current ripple on them to be ignored and the leakage inductance is low enough for the duty loss parts to be neglected. Then the current waveforms are simplified as shown in Figure 4. To meet the current·sec balance for C_b, the positive part of the primary current i_{pri} is equivalent to the negative part such that the magnetizing current is obtained as:

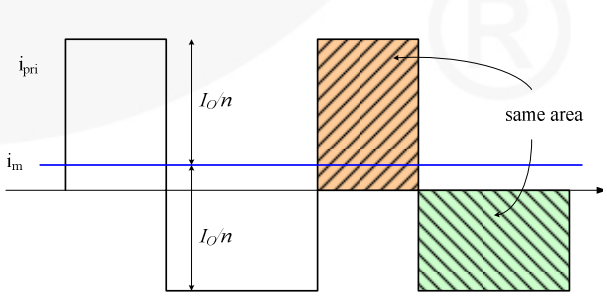


Figure 4. Simplified Current Waveforms in the Primary Side

$$\left(I_m + \frac{I_O}{n}\right) \times D = \left(-I_m + \frac{I_O}{n}\right) \times (1-D)$$
$$\Rightarrow \quad I_m = (1-2D)\frac{I_O}{n} \tag{5}$$

where I_m is the DC component of i_m. As can be seen in Equation (5), I_m could be zero when the duty cycle is 50%. Generally i_m has a DC offset, so the core saturation has to be taken into account when the transformer is designed.

2. Operational Principles of an Asymmetric PWM Half-Bridge Converter with Current Doubler and Synchronous Rectifier

For low-output-voltage and high-output-current applications, the current doubler is widely used. Figure 5 illustrates the asymmetric PWM half-bridge converter with the current doubler on the secondary side. The secondary winding is a single-ended configuration, while the output inductors are divided into two smaller inductors. To increase the total efficiency, a synchronous rectifier (SR) comprised of MOSFETs with low $R_{ds(on)}$ is used. The current doubler has several advantages compared to the conventional center-tapped configuration. First, the DC component of the magnetizing current is lower than or equal to that of the center-tapped configuration, which makes it possible to use the smaller core for the transformer. The amount of the magnetizing current is the same as that of the center-tapped configuration when each output inductor carries half the load current. The amount of the magnetizing current is reduced when the output inductors carry the load current unevenly. Second, the root-mean-square (rms) value of the secondary winding current is smaller than that of the center-tapped configuration, since almost half of the load current flows through each output inductor. As a result, the low current density for the secondary winding could be used with the same core and the same gauge of wire. Third, the winding itself is easier than the center-tapped configuration. This is notable especially for multi-output applications because of the limitation of the pin number of the bobbin of the transformer. Fourth, the gate signals for SR are obtained easily and effectively from the output inductors, as shown in Figure 6(b). An appropriate gate voltage (e.g., between 10 V and 20 V) could be easily obtained from the output inductors due to an enough number of turns, while the secondary side number of turns of the transformer is only a few. Additionally, the separated output inductors reduce the burden of the cost of the bigger core. These advantages make the current doubler one of the most popular topologies for high-output-current applications.

2.1. Operational Principles

Figure 7 shows the mode analysis for the asymmetric PWM half-bridge converter with the current doubler and corresponding key waveforms. Assume ZVS is achieved sufficiently with very short duration. The ZVS modes can be ignored in the mode analysis. The ZVS operation is discussed in detail in the next section. Other assumptions are:

(1) The DC-blocking capacitor C_b is large enough to neglect the voltage ripple on it, and

(2) All elements in the circuit are ideal.

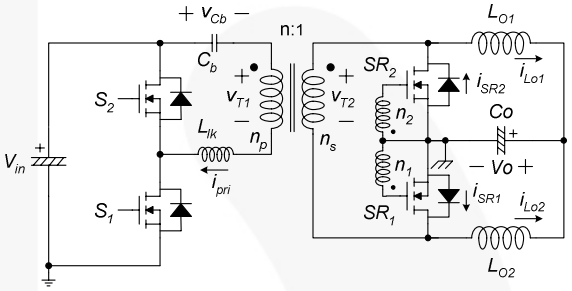


Figure 5. Asymmetric PWM Half-Bridge Converter with the Current Doubler

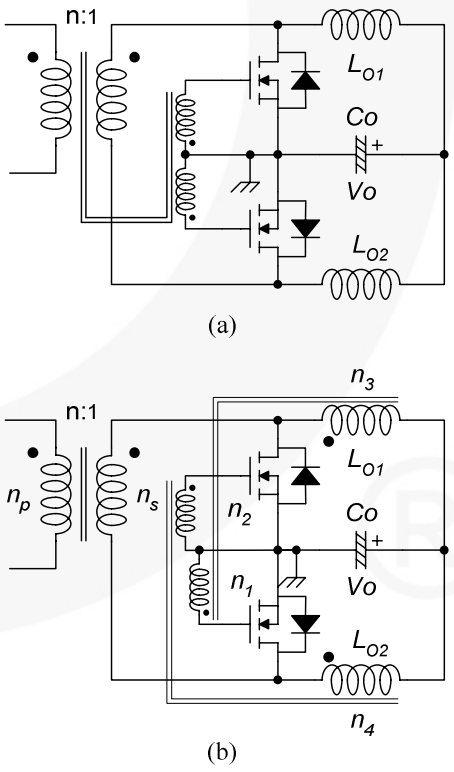


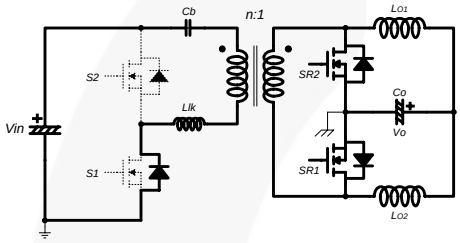
Figure 6. Methods for Producing the Gate Driver Signal Using; (a) the Transformer; (b) the Output Inductor

Let's start with Mode 2, a powering mode. When S_1 turns on, V_{in}-V_{Cb} is applied on the primary side of the transformer. The magnetizing current i_m increases with the slope of (V_{in}-V_{Cb})/L_m. The slope of the current of L_{O1} is determined by subtracting the output voltage from (V_{in}-V_{Cb})/n because SR_2 turns off. On the other hand, the current of L_{O2} decreases with the slope of $-V_O/L_{O2}$, which is free-wheeling through SR_1. While two output inductors share the load current, SR_1 carries the whole load current. The secondary winding of the transformer handles only i_{LO1} so that i_{LO1}/n is the reflected current to the primary side of the transformer and it is superimposed on the magnetizing current, which constitutes the primary current i_{pri}. In fact, v_{T2} is slightly lower than the value illustrated in Figure 7 due to leakage inductance (see Chapter 1.) It is ignored in this section to simplify analysis.

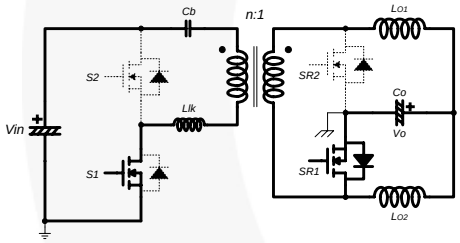
When S_1 turns off, Mode 3 begins. As the output capacitance of S_2 is discharged, v_{T1} decreases. It becomes zero when the output capacitance voltage of S_2 equals V_{Cb}. At this time, the body diode of SR_2 turns on since its reverse-biased voltage is eliminated. Subsequently, both *SRs* turn on together during this mode. The body diode of S_2 turns on after the S_2 output capacitance is wholly discharged and that of S_1 is entirely charged. Since both *SRs* turn on, i_{LO1} and i_{LO2} are free-wheeling with the slope of $-V_O/L_{O1}$ and $-V_O/L_{O2}$, respectively, and v_{T1} and v_{T2} are zero, V_{Cb} is applied only on the leakage inductance, causing the primary current's polarity to change rapidly. When S_2 turns on after the S_2 body diode conducts, the S_2 ZVS condition is achieved. The duration of this mode is obtained as:

$$D_{loss2} = \frac{I_O}{n} \times \frac{L_{lk}}{DV_{in} \times T_S} \quad (6)$$

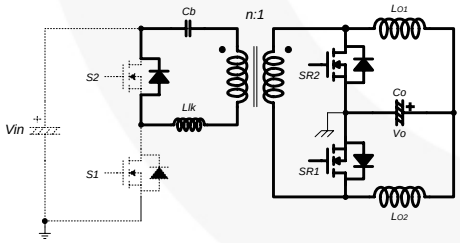
Mode 4, another powering mode, starts with the end of commutation between *SRs*. The applied voltage on the primary side of the transformer is $-V_{Cb}$ so that the magnetizing current decreases with the slope of $-V_{Cb}/L_m$ and



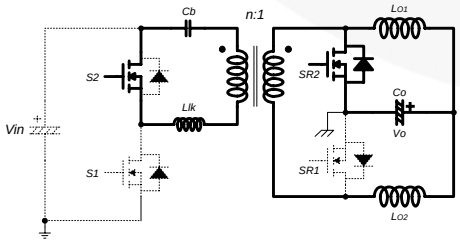
(a) Mode 1 (t_0~t_1)



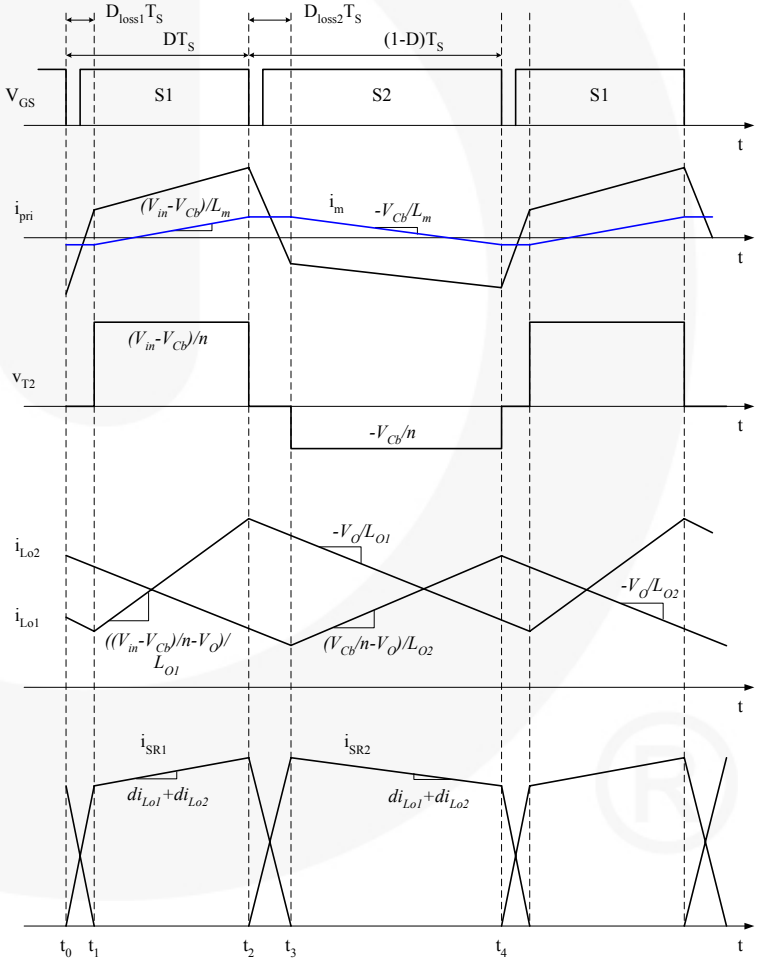
(b) Mode 2 (t_1~t_2)



(c) Mode 3 (t_2~t_3)



(d) Mode 4 (t_3~t_4)



(e) Key waveforms

Figure 7. Mode Analysis and Waveforms for Asymmetric PWM Half-Bridge Converter with the Current Doubler

the slope of i_{LO2} is $(V_{Cb}/n-V_O)/L_{O2}$. The other inductor current is free-wheeling through SR_2. As can be seen in Figure 7, the large ripple on each output inductor is cancelled because of the out-of-phase. Therefore, two smaller inductors can be used in the current doubler configurations compared with the center-tapped or bridge rectifying configurations.

When S_2 turns off, Mode 1 starts as another regenerating mode. The operating principle of Mode 1 is almost the same as Mode 3, except for a ZVS condition. In Mode 1, v_{T1} becomes zero at the instant when the output capacitance voltage of S_1 is equivalent to V_{in}-V_{Cb}. Before this instant, the load current on the output inductor L_{O2} is reflected to the primary side of the transformer and helps to meet the ZVS condition of the switches. The energy stored in the leakage inductance only has to discharge and charge the output capacitance of the switches after this instant. Therefore, the ZVS condition for S_1 is harder than S_2 since V_{in}-V_{Cb} is higher than V_{Cb} in general. In all other respects, Mode 1 can be analyzed in the same way as Mode 3. The duration of Mode 1 is obtained as:

$$D_{loss1} = \frac{I_O}{n} \times \frac{L_{lk}}{(1-D)V_{in} \times T_S} \tag{7}$$

The detailed output voltage is calculated with Equations (6) and (7) as:

$$V_O = \frac{L_m}{L_m + L_{lk}} \left(\frac{D(1-D)V_{in}}{n} - \frac{I_O L_{lk}}{n^2 T_S} \right) - V_{SR} \tag{8}$$

where V_{SR} is the voltage across the MOSFET as an SR during powering modes. It is similar to Equation (4) except for the turns ratio, which is half that of the conventional converter.

By modifying Equation (5), the DC and ripple components of i_m are obtained as:

$$I_m = (1-D)\frac{I_{LO2}}{n} - D\frac{I_{LO1}}{n} \tag{9}$$

$$\Delta i_m = (DT_S - D_{loss1}T_S) \times \frac{(1-D)V_{in}}{L_m + L_{lk}} \tag{10}$$

where I_{LO1} and I_{LO2} are the DC components of the output inductor currents.

2.2. ZVS Conditions

In the previous section, the duration for ZVS operation was omitted to simplify mode analysis. More detailed analysis for ZVS operation is given in this section to discover an exact ZVS condition for each switch. Figure 8 shows the detailed modes for Mode 1.

From t_0, the primary current starts to charge and discharge the output capacitance of the switches. Before the drain voltage of S_1, v_{DS1} reaches to V_{in}-V_{Cb}, the dotted terminal of the transformer is negative so that SR_1 is still reverse-biased. Therefore, not only the energy in the leakage inductance, but also the energy of the load current, helps S_1 be discharged from V_{in} to V_{in}-V_{Cb}. After v_{DS1} is reduced more than V_{in}-V_{Cb}, the dotted terminal of the transformer changes its polarity, which allows the body diode of SR_1 to turn on. Therefore, the magnetizing inductance is short-circuited so that the switches are charged and discharged by the energy in the leakage inductance only from t_a. Finally, v_{DS1} is fully discharged at t_b, so the primary current flows through the body diode of S_1, as can be seen in Figure 8(c). After t_c, the primary current flows through both the channel and the body diode since the gate signal of S_1 is applied. Mode 2 begins with the end of the commutation between *SRs* from t_1.

For the ZVS operation of S_1 there are three conditions in Figure 8, as follows:

(1) The energy in the leakage inductance should be sufficient to discharge S_1 from V_{in}-V_{Cb} to zero and charge S_2 from V_{Cb} to V_{in}.

(2) The instant t_b must be earlier than when the primary current changes its polarity. Otherwise, the drain voltages of S_1 and S_2 are again charged and discharged, respectively.

(3) The gate signal of S_1 must be applied before the primary current changes its polarity.

Figure 9 shows the detailed modes in Mode 3. While the detailed mode analysis is similar to the case of Figure 8, three conditions for the ZVS operation of S_2 are different from those of Figure 8:

(1') Since the polarity of the transformer terminals changes when v_{DS2} reaches V_{Cb}, the portion of discharging S_2 by the load current, t_2~t_d, is much larger than t_0~t_a in Figure 8. Therefore, the remaining portion of discharging S_2 by the energy in the leakage inductance only is shortened; the ZVS of S_2 is easier to achieve compared with the ZVS of S_1. Therefore, the energy in the leakage inductance should be sufficient to discharge S_2 from V_{Cb} to zero and charge S_1 from V_{in}-V_{Cb} to V_{in}.

(2') The commutation between *SRs* begins with the change of polarity of the transformer terminals so that it takes longer from t_e to the instant when the currents in *SRs* are equal. In addition, the commutation slope is more sluggish than the case in Figure 8, since the applied voltage on the leakage inductance is reduced to V_{Cb} from V_{in}-V_{Cb}.

(3') The gate signal of S_2 must be applied before the primary current changes its polarity if Condition (3) is satisfied due to the same dead time and the reason mentioned in (2').

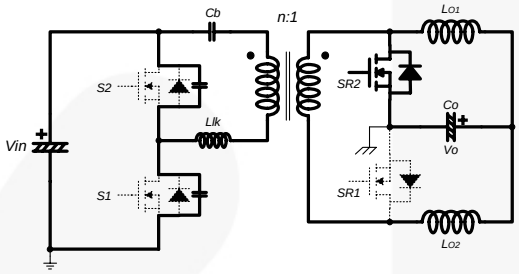
With respect to both energy ((1) and (1')) and timing ((2 & 3) and (2' & 3')), the ZVS condition of S_1 is more difficult to achieve than that of S_2. Therefore, the ZVS condition should be considered with S_1 only. In general, the condition for timing is easily satisfied if the condition for energy is

satisfied. Therefore, the required leakage inductance for the ZVS of both switches at special load condition can be calculated as:

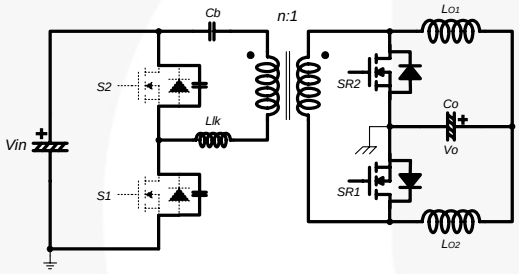
$$L_{lk} > \frac{2C_{OSS}\left[(1-D)V_{in}\right]^2}{\left\{\frac{D(1-D)V_{in}\times T_S}{2(L_m+L_{lk})} - \frac{I_{O,tar}}{2n}\left(1-\frac{L_m}{L_m+L_{lk}}\right)+\frac{DI_{O,tar}}{n}\right\}^2} \quad (11)$$

where C_{OSS} is the output capacitance of the switch and $I_{O,tar}$ is the target load condition where a designer wants the system to operate in ZVS condition with the leakage inductance.

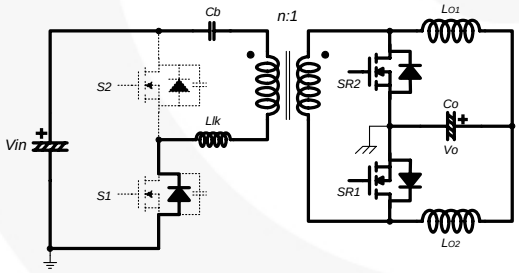
An easy way to achieve ZVS for both switches even at light load conditions is to increase L_{lk}. However, the increased L_{lk} increases duty loss parts by reducing the slope of the primary current in Modes 1 and 3. This results in the increase of conduction loss for the reduced effective duty cycle. Therefore, it is not recommended as a method to increase L_{lk} for ZVS at very light load. According to Equation (9), as the load current decreases, the DC component of the magnetizing current decreases as well. If the DC component of i_m is less than half the ripple component of i_m, the ZVS operation is performed by the magnetizing inductance with the leakage inductance. In Equation (11), ignoring the second term in the denominator,



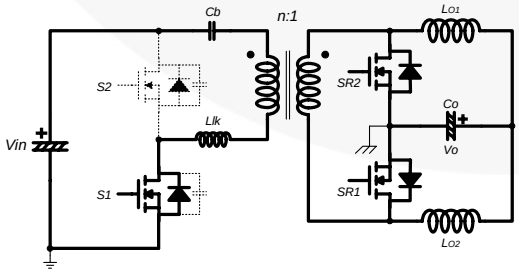
(a) Mode 1_1 (t_0~t_a)



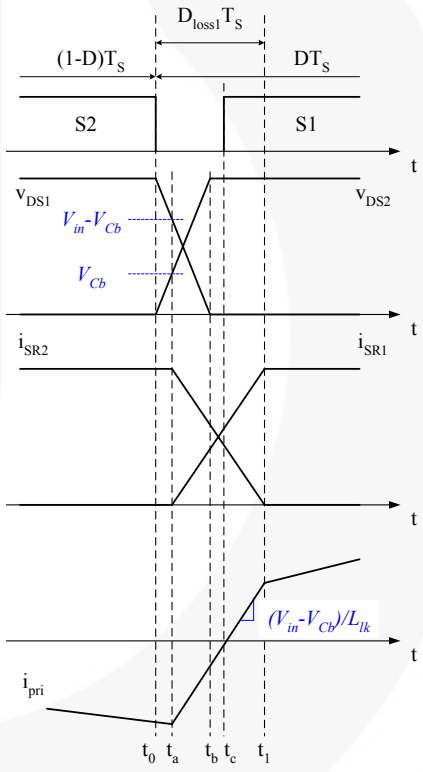
(b) Mode 1_2 (t_a~t_b)



(c) Mode 1_3 (t_b~t_c)



(d) Mode 1_4 (t_c~t_1)



(e) Key waveforms

Figure 8. Detailed Mode Analysis During Mode 1

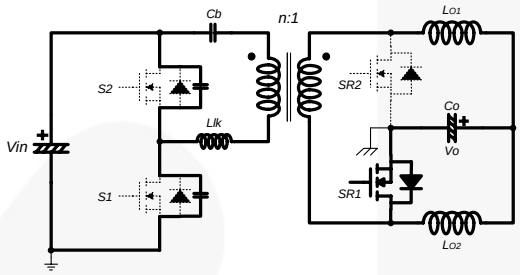
rearrangement for L_m yields:

$$L_m + L_{lk} < \frac{D(1-D)V_{in} \times T_S}{2 \times \left\{ \sqrt{\frac{2C_{OSS}}{L_{lk}}}(1-D)V_{in} - \frac{DI_{O,tar}}{n} \right\}} \quad (12)$$

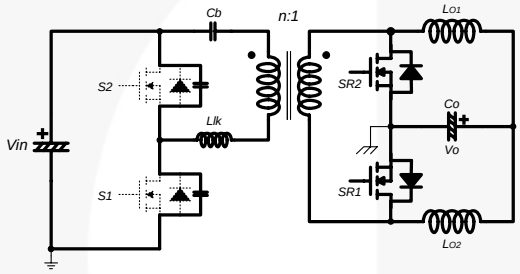
To obtain appropriate L_m and L_{lk} using Equations (11) and (12), iterations are necessary. An example of this is given in the next section.

2.3. Synchronous Rectifier

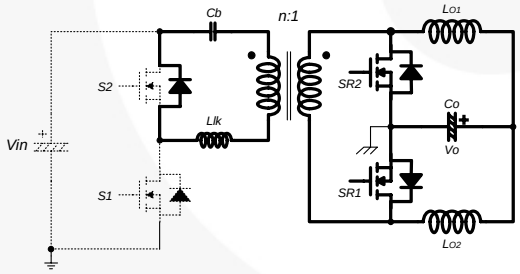
It is more profitable that the conduction losses on the secondary rectifying stage are composed of ohmic losses instead of diode losses when the output current is high. Since most of load current flow through the channel, conduction losses can be reduced dramatically if synchronous MOSFETs with very low $R_{ds(on)}$ (less than several mΩ) turn on and off appropriately. In buck-derived topologies such as forward, half-bridge, and full-bridge converters, the gate signal for SR is easily obtained from the



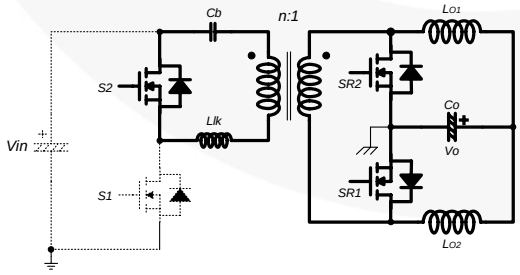
(a) Mode 3_1 (t_2~t_d)



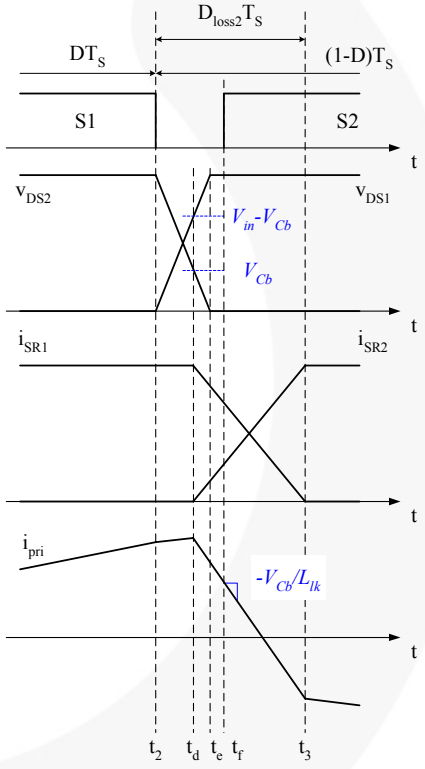
(b) Mode 3_2 (t_d~t_e)



(c) Mode 3_3 (t_e~t_f)



(d) Mode 3_4 (t_f~t_3)



(e) Key waveforms

Figure 9. Detailed Mode Analysis During Mode 3

main transformer (as shown in Figure 6(a)). Unlike flyback or LLC converters, there is no need to add any other special functions, except for the driving circuit. Ease of construction of the SR driver is another reason to use the half-bridge topology for high-output-load-current applications.

Moreover, when using a current doubler, it is more efficient to get the gate signal from the output inductors than from the main transformer (as shown in Figure 6(b)). Figure 10 illustrates the SR gate-signal waveforms from the main transformer and the output inductors. It is difficult to tune up the turns ratio n_a and n_b (where $n_a=n_s/n_1$ and $n_b=n_s/n_2$) to make the sufficient gate voltage (as shown in Figure 10(a)). This is because both positive and negative parts are dependent not only on the turns ratios n_a and n_b but also on V_{Cb}. Additionally, the power loss by the negative part of the gate signal is determined by the turns ratio, V_{Cb}, and V_{in}. On the other hand, the power loss by the negative part of the gate signal does not depend on the load condition (as shown in Figure 10(b), where $n_c=n_3/n_1$ and $n_d=n_4/n_2$). In addition, during the duty loss part, $D_{loss1}T_S$ and $D_{loss2}T_S$, the gate signals change their polarity to a negative value so that the SRs turn off rapidly and definitely. This helps to reduce the turn-off loss of the synchronous MOSFETs.

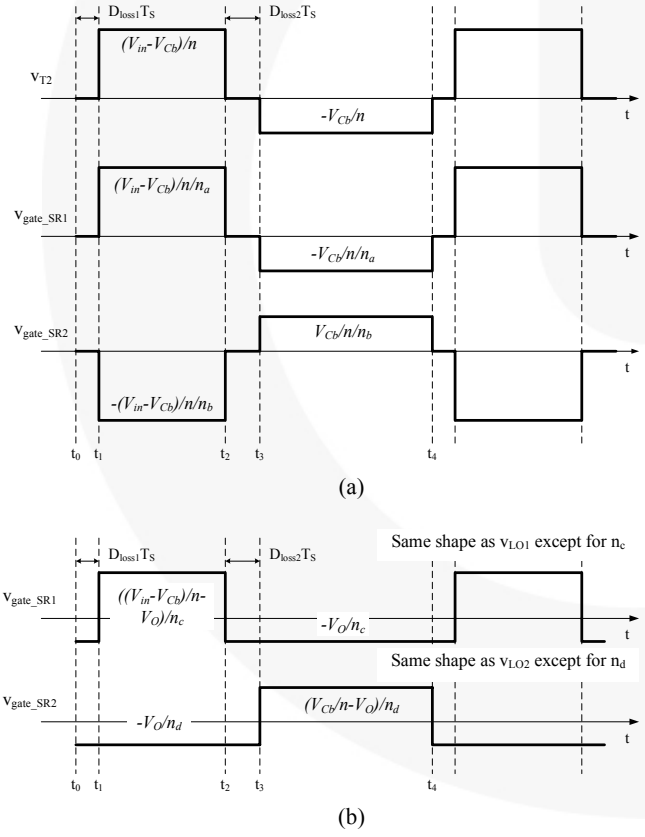


Figure 10. Gate Signals for Synchronous Rectifier; (a) Transformer Coupled; (b) Output Inductor Coupled

3. Design Procedure and Example

In this chapter, a design procedure is shown using the design reference illustrated in Figure 11. The target system for this example is a game console power-supply unit with 12 V of output voltage and 30 A of output load current. To handle the large output-load current, the current doubler with the synchronous rectifier discussed in the previous chapter is used. Since the input comes from a power factor correction (PFC) circuit, the input-voltage range is not wide.

[STEP 1] System Specifications

The first step in designing is to define the system specifications. Generally, a PFC circuit is used for medium- or high-power applications such as LCD/PDP TV systems, game console power supplies, and beam projectors to meet international harmonic regulations. Thus, the input voltage range for the main power stage (i.e. the output voltage of PFC stage) is almost fixed (e.g., 370~410 V_{dc}). However, the input voltage range may be widened to meet special requirements.

In this chapter, the target specifications are:

- Nominal input voltage: 390 V_{dc}
- Input voltage range: 370~410 V_{dc}
- Output voltage: 12 V
- Output current: 30 A
- Switching frequency: 100 kHz

[STEP 2] Turns Ratio and Duty Cycle

The output voltage equation (Equation 8) is used to determine turns ratio n. However, the output voltage equation contains the leakage and magnetizing inductance, which are not yet determined. Therefore, a designer should make assumptions for the following:

- V_{SR} considering $R_{ds(on)}$ of used MOSFETs as an SR;
- α, the ratio between L_m and L_m+L_{lk};
- The leakage inductance that will be changed later by iterations of Equations (11) and (12);
- The nominal duty cycle at the nominal input voltage.

According to Equation (8), the turns ratio is obtained as:

$$n = \frac{D_n(1-D_n)V_{in,n} + \sqrt{(D_n(1-D_n)V_{in,n})^2 - 4(V_O+V_{SR})\frac{I_O L_{lk}}{\alpha T_S}}}{\frac{2(V_O+V_{SR})}{\alpha}} \quad (13)$$

where $V_{in,n}$ and D_n are the nominal input voltage and the nominal duty cycle at $V_{in,n}$, respectively.

For turns ratio n, the duty cycle at an input voltage and a load current is calculated as:

$$D = \frac{1-\sqrt{1-4\left(\frac{n(V_O+V_{SR})}{\alpha V_{in}} + \frac{I_O L_{lk}}{nV_{in}T_S}\right)}}{2} \quad (14)$$

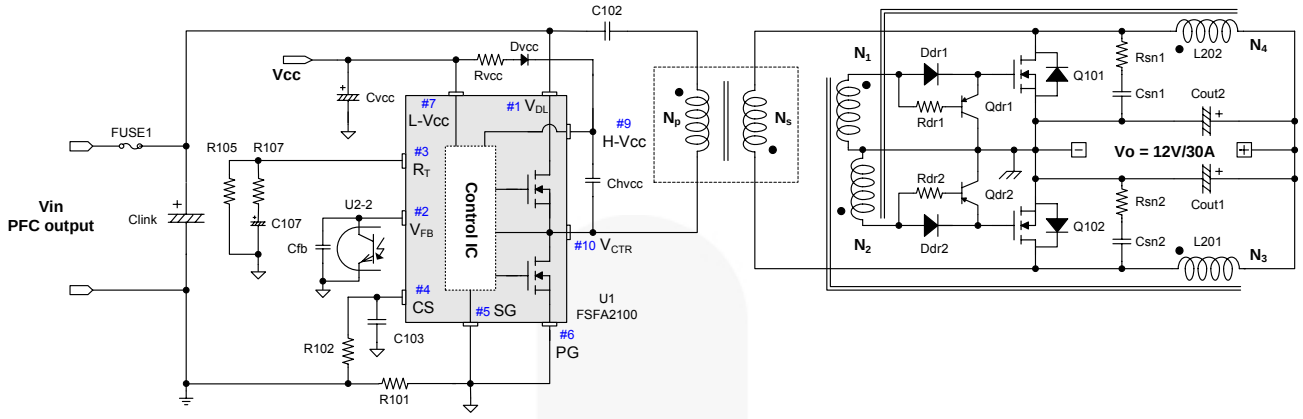


Figure 11. Reference Design Schematic

Design Example

For the example, the following values are assumed:

- $V_{SR} = 0.3\text{V}$
- α is 0.95
- The initial leakage inductance is 20 µH. This may be increased after checking the ZVS condition. Taking the core size for 360W into account, if L_{lk} is less than this value, the productivity is not good.
- The nominal duty cycle at 390 V_{dc} is 0.4.

Using these values, the turns ratio is obtained by Equation (13) as:

$$n = \frac{0.4 \cdot 0.6 \cdot 390 + \sqrt{(0.4 \cdot 0.6 \cdot 390)^2 - 4(12 + 0.3)\dfrac{30 \cdot 20\mu}{0.95 \cdot 10\mu}}}{\dfrac{2(12 + 0.3)}{0.95}}$$

$$= 6.52$$

yielding a turns ratio is 6.5. The nominal duty cycle at the nominal input voltage is recalculated by Equation (14) as:

$$D_n = \frac{1 - \sqrt{1 - 4\left(\dfrac{6.5 \cdot (12 + 0.3)}{0.95 \cdot 390} + \dfrac{30 \cdot 20\mu}{6.5 \cdot 390 \cdot 10\mu}\right)}}{2} = 0.397$$

[STEP 3] Magnetizing and Leakage Inductance

Using the turns ratio obtained in Step 2, the ZVS condition could be checked with Equations (11) and (12).

Design Example

This example is designed to achieve the ZVS operation from full- to 30%-load condition using the leakage inductance and the magnetizing inductance. The duty cycle at 30% load condition and the maximum input voltage is obtained by Equation (14) as:

$$D_{@30\%} = \frac{1 - \sqrt{1 - 4\left(\dfrac{6.5 \cdot (12 + 0.3)}{0.95 \cdot 410} + \dfrac{9 \cdot 20\mu}{6.5 \cdot 410 \cdot 10\mu}\right)}}{2}$$

$$= 0.305.$$

Since C_{OSS} of the FSFA2100 MOSFETs is 150 pF, the required leakage inductance is obtained with $D_{@30\%}$=0.305 as:

$$L_{lk} > \frac{2C_{OSS}[(1-D)V_{in}]^2}{\left\{\dfrac{D(1-D)V_{in} \times T_S}{2(L_m + L_{lk})} - \dfrac{I_{O,tar}}{2n}\left(1 - \dfrac{L_m}{L_m + L_{lk}}\right) + \dfrac{DI_{O,tar}}{n}\right\}^2}$$

$$= \frac{2 \cdot 150p \cdot [(1-0.305) \cdot 410]^2}{\left\{\dfrac{0.305 \cdot (1-0.305) \cdot 410 \times 10\mu}{2(400\mu + 20\mu)} - \dfrac{9}{2 \times 6.5}\left(1 - \dfrac{400\mu}{400\mu + 20\mu}\right) + \dfrac{0.305 \cdot 9}{6.5}\right\}^2}$$

$$= 12.0\mu H.$$

The required leakage inductance is 12.0 µH, which is too small to control in a mass production. If the obtained value is larger than the assumed value, the obtained value is used, and the SMPS designer must repeat Step 2 to check if the turns ratio is still valid. However, in this design example, the designer chooses the initial value for productivity, and there is no iteration needed.

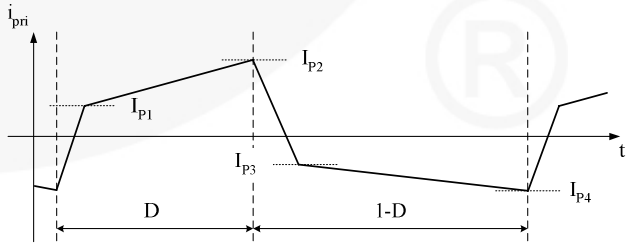


Figure 12. Primary Current Waveform

The magnetizing inductance can be determined using Equation (12) as:

$$L_m + L_{lk} < \frac{D(1-D)V_{in} \times T_S}{2 \times \left\{ \sqrt{\frac{2C_{OSS}}{L_{lk}}}(1-D)V_{in} - \frac{DI_{O,tar}}{n} \right\}}$$
$$= \frac{0.305 \cdot (1-0.305) \cdot 410 \cdot 10\mu}{2 \times \left\{ \sqrt{\frac{2 \cdot 150p}{20\mu}}(1-0.305) \cdot 410 - \frac{0.305 \cdot 9}{6.5} \right\}}$$
$$= 638\mu H.$$

Therefore, L_m is selected as 600 µH.

[STEP 4] Transformer

Using Equations (9) and (10), the peak magnetizing current is obtained as:

$$I_m + \frac{\Delta i_m}{2} = (1-D)\frac{I_{LO2}}{n} - D\frac{I_{LO1}}{n} + (DT_S - D_{loss1}T_S) \times \frac{(1-D)V_{in}}{2(L_m + L_{lk})} \quad (15)$$

The maximum value of the peak magnetizing current occurs when each output inductor carries half the load current for the worst case and the duty cycle is zero during startup or transient instant. Therefore, the maximum i_m is:

$$i_m{}^{\max} = \frac{I_O}{2n} \quad (16)$$

The minimum number of turns for the transformer primary side is given as:

$$N_P{}^{\min} = \frac{L_m i_m{}^{\max}}{A_e B_{\max}} \quad (17)$$

where A_e is the effective cross-sectional area of the used core in mm^2, and B_{max} is the maximum flux density in Tesla. B_{max} = 0.2~0.25 T is recommended if there is no reference data.

The number of turns for the transformer secondary side is obtained as:

$$N_S = \frac{N_P}{n} \quad (18)$$

where N_P is larger than $N_P{}^{min}$ in Equation (17).

The diameter of the wire is selected based on the current density, whose range is generally 4~10 A/mm^2. It is recommended to select the current density as low as possible to reduce conduction losses on the wire. However, try to reduce the winding layers at the same time. The more winding layers, the more circulating current caused by the proximity effect. Sometimes trying to reduce conduction losses by increasing the wire diameter makes conduction losses increase by increasing the circulating current. In addition, it is better to choose a wire with multi-strands of thinner wire, such as Litz wire, to minimize the skin effect.

When the output inductor current ripple is ignored, Figure 12 shows the primary-current waveform. The rms value of this waveform is given as:

$$i_P{}^{rms} = \sqrt{\frac{(I_{P1}{}^2 + I_{P1}I_{P2} + I_{P2}{}^2)}{3}D + \frac{(I_{P3}{}^2 + I_{P3}I_{P4} + I_{P4}{}^2)}{3}(1-D)} \quad (19)$$

$$I_{P1} = \frac{I_{LO1}}{n} + I_m - \frac{\Delta i_m}{2} \quad (20)$$

$$I_{P2} = \frac{I_{LO1}}{n} + I_m + \frac{\Delta i_m}{2} \quad (21)$$

$$I_{P3} = -\frac{I_{LO2}}{n} + I_m + \frac{\Delta i_m}{2} \quad (22)$$

$$I_{P4} = -\frac{I_{LO2}}{n} + I_m - \frac{\Delta i_m}{2} \quad (23)$$

where I_m and Δi_m are defined in Equations (9) and (10).

For the secondary-side winding, half the load current is the rms value when it is assumed that each output inductor carries the load current evenly and the ripple on the output inductor is small enough to be ignored.

Design Example

When the duty cycle is zero, the maximum i_m is obtained as:

$$i_m{}^{\max} = \frac{I_O}{2n} = \frac{30}{2 \cdot 6.5} = 2.31A.$$

The given core is EER4042 (A_e=158 mm^2). The minimum turns number for the transformer primary side is calculated as:

$$N_P{}^{\min} = \frac{L_m i_m{}^{\max}}{A_e B_{\max}} = \frac{600\mu \cdot 2.31}{158\mu \cdot 0.23} = 38.14$$

When N_P is selected as 39, the secondary turns number is obtained as 6.

Use Equations (19)-(23) to get the rms value of the transformer primary side current. Assume each output inductor carries the output load current evenly at the nominal condition (D_n=0.397).

$$I_{P1} = \frac{15}{6.5} + 0.475 - \frac{1.357}{2} = 2.10A$$

$$I_{P2} = \frac{15}{6.5} + 0.475 + \frac{1.357}{2} = 3.46A$$

$$I_{P3} = -\frac{15}{6.5} + 0.475 + \frac{1.357}{2} = -1.15A$$

$$I_{P4} = -\frac{15}{6.5} + 0.475 - \frac{1.357}{2} = -2.51A$$

Therefore, the rms value of the transformer primary side current is obtained by Equation (19) as:

$$i_P^{rms} = \sqrt{\frac{(2.1^2 + 2.1 \cdot 3.46 + 3.46^2)}{3} 0.397 + \frac{((-1.15)^2 + (-1.15)(-2.51) + (-2.51)^2)}{3}(1 - 0.397)} = 2.29A.$$

The rms value of the transformer secondary side current is half the load current, so i_S^{rms}=15 A.

Since the diameter of the wire becomes too thin, it is not easy to wind 39 turns for the primary side of the transformer in two layers. Choose the biggest wire that can be wound 13 turns in one layer of the bobbin for EER4042. Due to consideration of the skin effect, Litz wire of 100 strands with AWG38 (American wire gauge) is selected as the primary wire. In this case, the current density is around 2.9 A/mm^2. For the secondary side, 250-strand Litz wire with AWG36 is chosen where the current density is around 4.7 A/mm^2.

[STEP 5] Output Inductance

The output inductor current ripple is given as:

$$\Delta i_{LO1} = \frac{(V_O + V_{SR})(1 - D + D_{loss1})T_S}{L_{O1}} \quad (24)$$

$$\Delta i_{LO2} = \frac{(V_O + V_{SR})(D + D_{loss2})T_S}{L_{O2}} \quad (25)$$

In general, the current ripple on the output inductor is set to 10-20% of the rated output load current.

Design Example

In the design example, the ripple on each output inductor is selected to be less than 20% of the rated output load current. The inductances are calculated as:

$$L_{201} = \frac{(V_O + V_{SR})(1 - D + D_{loss1})T_S}{\Delta i_{LO1}} = \frac{(12 + 0.3)(1 - 0.397 + 0.039) \times 10\mu}{6} = 13.2\mu H$$

$$L_{202} = \frac{(V_O + V_{SR})(D + D_{loss2})T_S}{\Delta i_{LO2}} = \frac{(12 + 0.3)(0.397 + 0.060) \times 10\mu}{6} = 9.4\mu H$$

To increase productivity, both output inductors are selected as the same value, 15μH.

[STEP 6] Operating frequency

In Figure 11, the operating frequency f_S is obtained by using the following equation when FSFA-series is used.

$$f_S = \frac{27k\Omega}{R_{105}} \times 100 \quad [kHz] \quad (26)$$

Design Example

For the design example, the frequency setting resistor R_{105} is selected as 27 kΩ for 100 kHz operation.

[STEP 7] DC-Blocking Capacitance

It has been assumed that the DC-blocking capacitor is large enough to neglect the voltage ripple on it. However, too large a DC-blocking capacitor leads to slow dynamic response. Therefore, it is recommended to make the voltage ripple on the DC-blocking capacitor around 10% of the input voltage. The voltage ripple on the DC-blocking capacitor is obtained as:

$$\Delta v_{Cb} \cong \frac{1}{2C_b} \times \left(\frac{D_{loss1} T_S \times I_{P1}}{2} + \frac{D_{loss2} T_S \times I_{P2}}{2} + \frac{(D - D_{loss1}) T_S \times (I_{P1} + I_{P2})}{2} \right) \quad (27)$$

Design Example

When the voltage ripple on the capacitor is 30 V, the DC-blocking capacitance is calculated using Equation (27) as:

$$C_{102} \cong \frac{1}{2\Delta v_{C102}} \times \left(\frac{D_{loss1} T_S \times I_{P1}}{2} + \frac{D_{loss2} T_S \times I_{P2}}{2} + \frac{(D - D_{loss1}) T_S \times (I_{P1} + I_{P2})}{2} \right)$$

$$= \frac{1}{2 \times 30} \times \left(\frac{0.039 \times 10\mu \times 2.1}{2} + \frac{0.06 \times 10\mu \times 3.47}{2} + \frac{(0.397 - 0.039) \times 10\mu \times (2.1 + 3.47)}{2} \right)$$

$$= 190nF$$

Therefore, 220 nF is selected as the DC-blocking capacitor.

[STEP 8] Sensing Resistor

The pulse-by-pulse current limit of the FSFA-series switches can be adjusted by changing R_{101} in Figure 11. It is determined by the peak of the primary current obtained using Equation (21) when the input voltage is maximized. Due to the ripple current of the magnetizing inductance, the maximum peak of the primary current happens when the input voltage is maximized.

Design Example

Continuing with the example, calculate the duty cycle at the maximum input voltage and full-load conditions using Equation (14).

$$D_{@410V,100\%} = \frac{1-\sqrt{1-4\left(\frac{n(V_O+V_{SR})}{\alpha V_{in}}+\frac{I_O L_{lk}}{nV_{in}T_S}\right)}}{2}$$

$$= \frac{1-\sqrt{1-4\left(\frac{6.5\cdot(12+0.3)}{600\mu/620\mu\times 410}+\frac{30\times 20\mu}{6.5\times 410\times 10\mu}\right)}}{2}$$

$$= 0.338.$$

Then, the peak of the primary current is obtained combining Equations (7), (9), (10), and (21) as:

$$I_{P2} = \frac{I_{LO1}}{n} + I_m + \frac{\Delta i_m}{2}$$

$$= \frac{I_{LO1}}{n} + (1-D)\frac{I_{LO2}}{n} - D\frac{I_{LO1}}{n} + \frac{1}{2}\left(DT_S - \frac{I_O L_{lk}}{n(1-D)V_{in}}\right)\times\frac{(1-D)V_{in}}{L_m+L_{lk}}$$

$$= \frac{15}{6.5} + (1-0.338)\frac{15}{6.5} - 0.338\cdot\frac{15}{6.5} + \frac{1}{2}\left(0.338\times 10\mu - \frac{30\times 20\mu}{6.5\cdot(1-0.338)\cdot 410}\right)\times\frac{(1-0.338)\cdot 410}{600\mu+20\mu}$$

$$= 3.72A$$

Since the internal threshold voltage for the pulse-by-pulse current limit is -0.58 V, 0.1 Ω is selected as the sensing resistor, R_{101}.

[STEP 9] Synchronous Rectifier

The voltage stresses on the SRs are calculated as:

$$V_{SR1} = \frac{DV_{in}}{n} \quad (28)$$

$$V_{SR2} = \frac{(1-D)V_{in}}{n} \quad (29)$$

For windings to drive the gate of the SRs, during powering modes the voltages across the output inductors are:

$$V_{LO1} = \frac{(1-D)V_{in}}{n} - V_O \quad (30)$$

$$V_{LO2} = \frac{DV_{in}}{n} - V_O \quad (31)$$

Design Example

Considering the worst case for each SR, the voltage stresses on them are:

$$V_{Q101} = \frac{DV_{in}}{n} = \frac{0.5\times 410}{6.5} = 32$$

$$V_{Q102} = \frac{(1-D)V_{in}}{n} = \frac{(1-0)\times 410}{6.5} = 64$$

An N-channel power MOSFET with 8mΩ of $R_{ds(on)}$ and 100V of the voltage rating, HUF75652G3, is selected for both SRs with consideration of the voltage ringing and overshoot.

The voltages across the output inductors during powering modes are:

$$V_{L201}^{\min} = \frac{(1-D_{@370V,100\%})\cdot 370}{n} - V_O = \frac{(1-0.458)\cdot 370}{6.5} - 12 = 19$$

$$V_{L201}^{\max} = \frac{(1-0)\cdot 410}{n} - V_O = \frac{410}{6.5} - 12 = 51$$

$$V_{L202}^{\min} = \frac{0\times V_{in}}{n} - V_O = -12$$

$$V_{L202}^{\max} = \frac{D_{@370V,100\%}\times 370}{n} - V_O = \frac{0.458\times 370}{6.5} - 12 = 14$$

To protect the SRs, the gate signal has to be restricted ±20 V. The turns ratios between the output inductors and the windings for the gate drivers are:

$$\frac{N_3}{N_1} = 3$$

$$\frac{N_4}{N_2} = 1$$

[STEP 10] External Soft Start

At startup, the duty cycle starts increasing slowly to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. For the FSFA-series, the soft-start time is internally implemented for 15ms when the operating frequency is set to 100 kHz. In addition, to help the soft-start operation, a capacitor and a resistor are connected on the R_T pin externally, as shown in Figure 11. Before the power supply is powered on, the capacitor C_{107} remains fully discharged. After power-on, C_{107} becomes charged gradually by the current through the R_T pin, which determines the operating frequency. The current through the R_T pin is inversely proportional to the total impedance of the connected resistors. The total impedance during startup is lower than that of the normal operation because R_{107} is added on R_{105} in parallel, which means the operating frequency decreases continuously from higher to nominal. Eventually, C_{107} is fully charged to the R_T pin voltage and the operating frequency is determined by R_{105} only.

During C_{107} charging time, the operating frequency is higher than during normal operation. In asymmetric PWM half-bridge converters, a switching period contains powering and commutation periods. The energy cannot be transferred to the output side during the commutation period. Since the DC

link voltage applied to the V_{DL} pin and the leakage inductance of the main transformer are fixed, the powering period over the switching period is shorter in high switching frequencies. As C_{107} is charged, the switching frequency decreases so that the powering period over the switching period increases. It is helpful to start SMPS with the internal soft-start time together.

Design Example

In the design example, 2.2 µF and 12 kΩ are selected as C_{107} and R_{107}, respectively.

4. Design Summary

Figures 13 and 14 show the full schematic of the reference design and its transformer configuration. Table 1 shows the detailed wire information of the transformer. The electrical features of the transformer are described in Table 2.

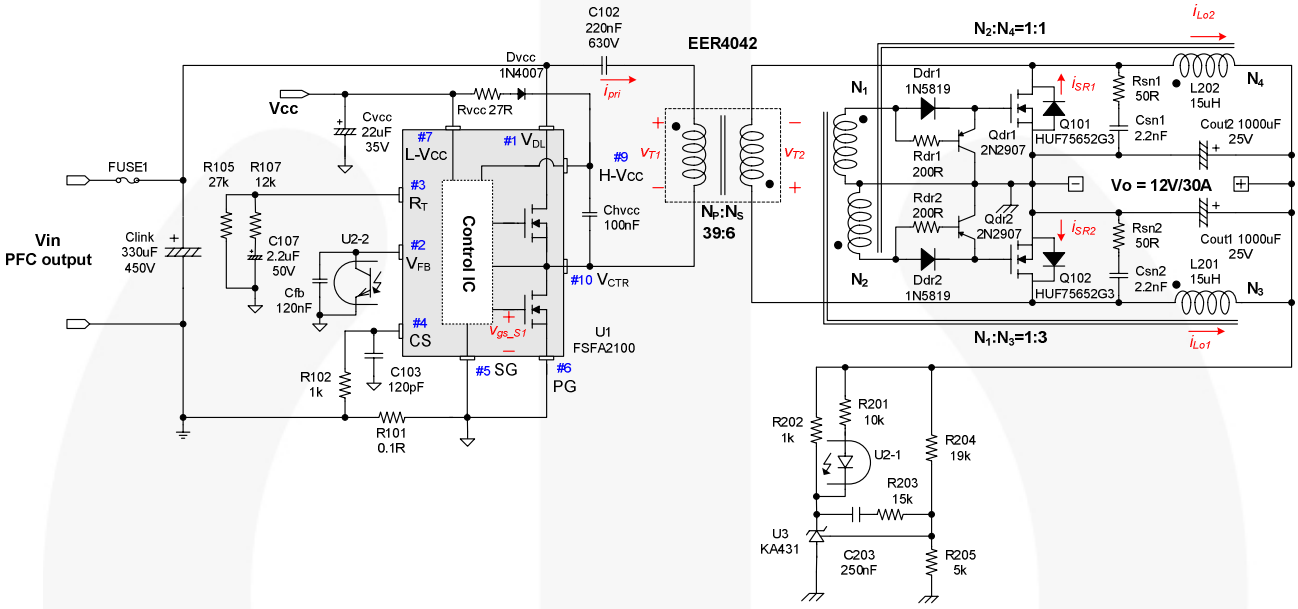


Figure 13. Full Schematic with Components Values of the Reference Design

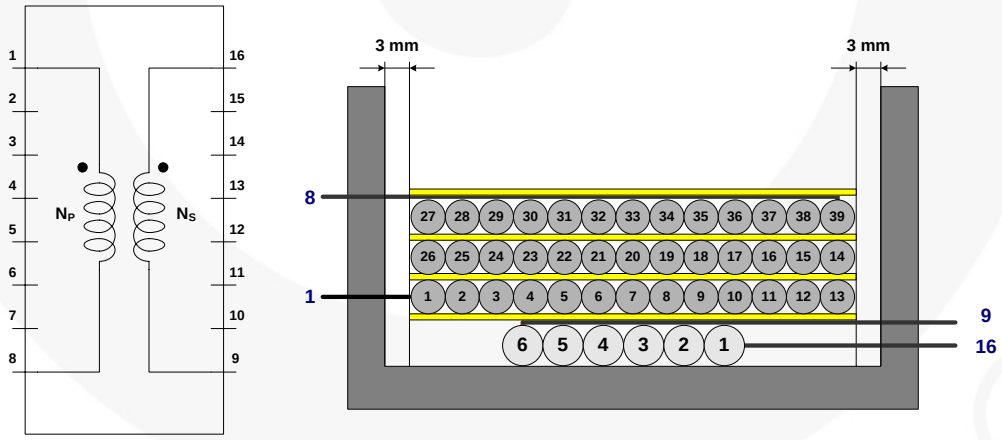


Figure 14. Transformer Construction of the Reference Design

Table 1. Transformer Winding Specifications

No.	Winding	Pin (start → end)	Wire	Turns	Winding Method
	Insulation Tape (25 um) 1T				
2	N_P	1 → 8	Litz wire (AWG38×100 strands) (1)	39 T	Solenoid
	Insulation Tape (25 um) 1T				
1	N_S	16 → 9	Litz wire (AWG36×250 strands)	6 T	Solenoid

NOTE:
1. Insulation tape (25 μm, 1T each) should be inserted between the layers.

Table 2. Transformer Electrical Characteristics

	Pin	Spec.	Remark
Magnetizing Inductance (L_m)	1 − 8	600 μH (typical) (600 μH ± 5%)	100 kHz, 1 V All other pins open
Leakage Inductance (L_{lk})	1 − 8	20 μH ± 10%	100 kHz, 1 V All other pins shorted

5. Experimental Results

Figures 15 and 16 show the experimental waveforms of the converter designed in the previous chapter at the nominal input and the full-load condition. The gate signal of S_1, the primary- and secondary-side voltages across the main transformer, and the primary current are shown in Figure 15. These waveforms are consistent with the theoretical analysis, including the ZVS operation. The output inductor currents and the SRs' currents are shown in Figure 16. The output inductor currents are unbalanced due to the duty cycle and the parasitic components, which means the averaged magnetizing current is smaller than that of the center-tapped configuration.[1]

Figure 17 shows the winding voltages for the gate driver circuits of SRs at the full-load condition. The upper waveforms are for the inductor coupling illustrated in Figure 6(b), while the lower ones are for the transformer coupling illustrated in Figure 6(a). As can be seen in Figure 17, since the winding voltage decreases to the negative at the turn-off transition in the upper waveforms, the SRs are turned off more rapidly and definitely than in the transformer coupling case. In Figure 17, the smaller negative parts in the inductor coupling case are shown compared to the transformer coupling case. The smaller negative parts allow the power losses on the gate driver circuit for SRs to be reduced.

The ZVS operations at various load conditions are shown in Figure 18. The drain voltage and the gate signal of the lower side switch are displayed. As designed in the previous chapter, the converter shows ZVS operation downs to 30% load condition.

The efficiency of the converter is shown in Figure 19. The measured efficiencies are 93.7%, 94.6%, and 93.1% at 20%, 50%, and 100% of the rated load condition, respectively. It shows a marginal performance so that the 85 PLUS program can be achieved with well-designed PFC and DC-DC stages.

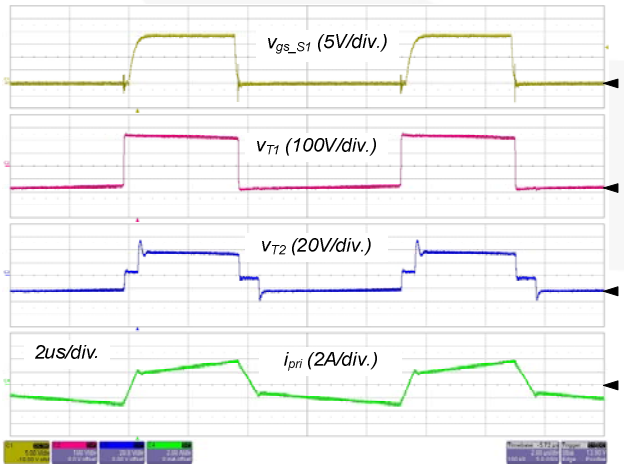


Figure 15. Experimental Waveforms

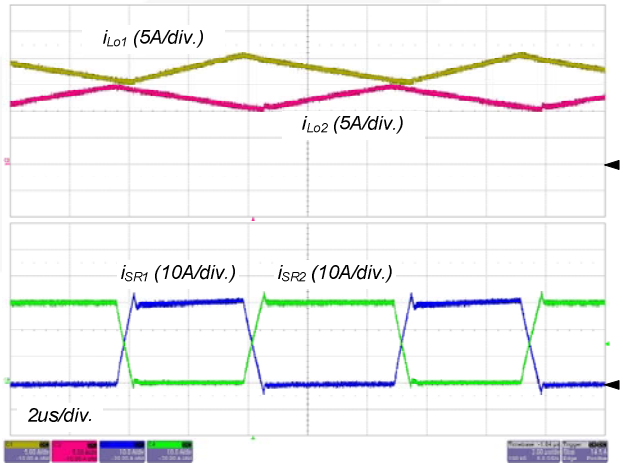


Figure 16. Waveforms for the Secondary Side

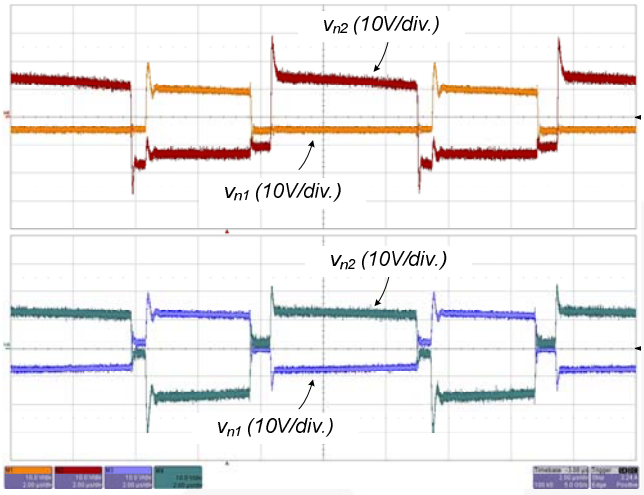
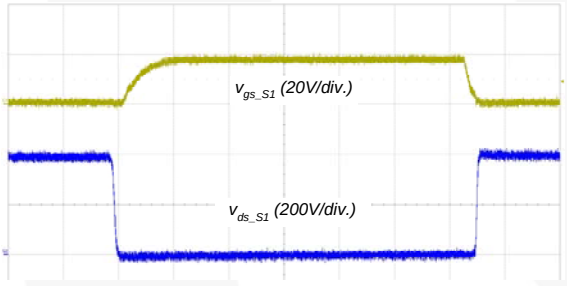
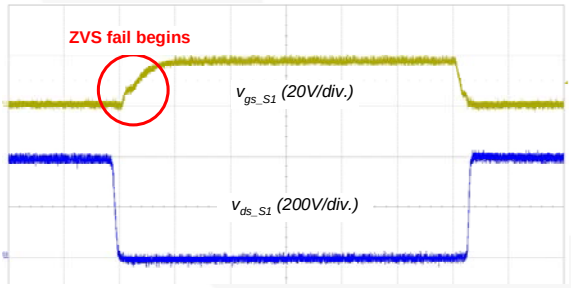


Figure 17. Gate Signals for SR; Upper Waveforms Use Output Inductors; Lower Waveforms Use the Transformer



(a)



(b)

Figure 18. ZVS Verification; (a) at 40% Load; (b) at 30% Load

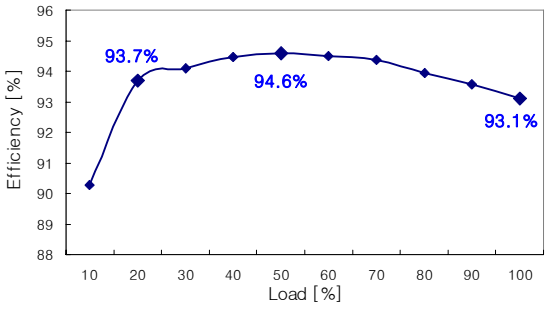


Figure 19. Measured Efficiency of the Designed Converter

6. References

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[3] Panov, Y. and Jovanovic, M.M., "Design and Performance Evaluation of Low-Voltage / High-Current DC/DC On-board Modules," IEEE Transactions on Power Electronics, Vol. 16, Issue 1, Jan. 2001 pp. 26-33.

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