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AN-6602

Low Noise JFET – The Noise Problem Solver

Introduction

The most versatile low noise active device available to the designer today is the Junction Field-Effect Transistor (JFET). JFETs are virtually free of the problems which have plagued bipolar transistors—limited bandwidth, popcorn noise, a complex design procedure to optimize noise performance. In addition, JFETs offer low distortion and very high dynamic range.

Most designers think of JFETs for very high source impedances. However, modern devices offer the designer performance improvements over bipolar transistors in Noise Figure (NF) for all but lowest impedance (<5000Ω) sources and even then may provide improved performance if popcorn noise, bandwidth or circuit component noise is a consideration (see Figure 1).

Therefore, the purpose of this article is to review low noise design procedures and indicate the simplicity of designing high performance low noise amplifiers with low cost JFETs.

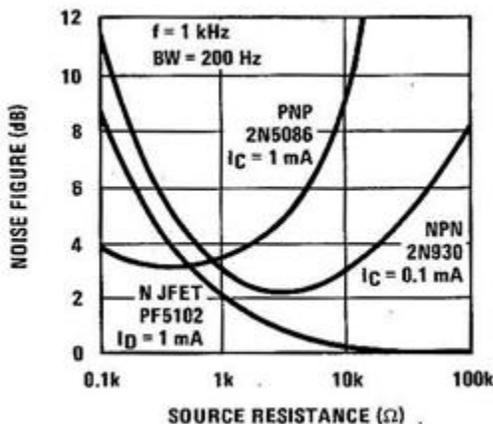


Figure 1. Bipolar and JFET Transistor Noise Comparison

Review of Basics

Before guidelines are established for designing low noise JFET amplifiers, a method of noise characterization must be chosen. Designers are confronted with a multitude of different noise parameters such as Noise Figure (NF), noise voltage and current densities, noise temperature, noise resistance, etc. Designers are primarily concerned with signal to noise (S/N) ratios preferring noise voltage, (e_n) and current (i_n) density.

Noise generally manifests itself in three forms: thermal noise, shot noise and flicker or "1/f" noise. Thermal noise arises from thermal agitation of electrons in a conductor and is given by Nyquist's relation:



$$\overline{V_R^2} = 4kTR\Delta f \quad (1)$$

$$\overline{V_R^2} = \text{mean square noise voltage}$$

$$k = \text{Boltzmann constant} \\ (1.38 \times 10^{-23} \text{ VAS/}^\circ\text{K})$$

$$T = \text{Absolute temperature (}^\circ\text{K)}$$

$$R = \text{Resistance in ohms}$$

$$\Delta f = \text{Noise bandwidth (Hz)}$$

The noise of a resistor may be represented as a spectral density (V^2/Hz) or more commonly in $\mu\text{V}/\sqrt{\text{N Hz}}$ or $\text{nV}/\sqrt{\text{Hz}}$ and is given by:

$$e_{nR} = (\overline{V_R^2}/\Delta f)^{1/2} \quad (2)$$

It is sometimes more convenient to represent thermal noise as noise current instead of a noise voltage. One needs only to consider the Norton equivalent yielding a noise current density.

$$i_{nR} = \frac{e_{nR}}{R} = \left(\frac{4 kT}{R}\right)^{1/2} \tag{3}$$

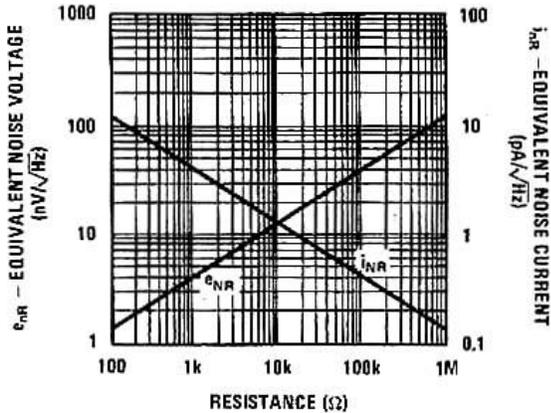


Figure 2. Thermal Noise Voltage and Current Densities vs Resistance.

The second basic form of noise, shot noise, is due to the randomness of current flow (discrete charge particles) in semiconductor P-N junctions.

$$\overline{i^2} = 2 q I_{DC} \Delta f \tag{4}$$

- $\overline{i^2}$ = Mean square noise current
- q = Charge of an electron (1.6×10^{-19} AS)
- I_{DC} = dc current flowing through the junction (A)
- Δf = Noise bandwidth (Hz)

As with thermal noise, shot noise may be represented as a current density (A^2/Hz) or pA/\sqrt{Hz} .

$$i_n = (\overline{i^2}/\Delta f)^{1/2} \tag{5}$$

It should be noted that both thermal noise and shot noise are “white” noise sources, i.e. frequency independent.

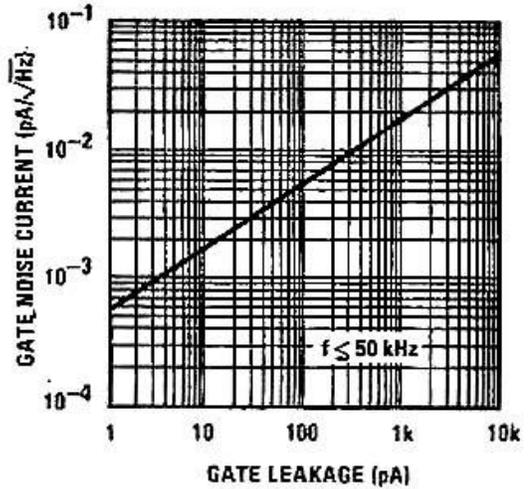


Figure 3. Current Noise vs. Gate Leakage Current

The third basic noise source confronting designers is flicker or “1/f” noise whose density is roughly inversely proportional to frequency starting at about 1 kHz in both JFETs and bipolar transistors and increasing as frequency is decreased. Through careful processing, flicker noise in JFETs has been reduced to levels nearly insignificant to the designer. Flicker noise in JFETs is primarily a noise voltage and is source independent. Flicker noise in bipolar transistors is a function of base and leakage current increasing with increased source impedance or operating currents.

A simple noise model of a JFET or any amplifying device may be constructed using a thermal and shot noise source which would adequately describe its noise performance allowing signal to noise ratios to be calculated directly.

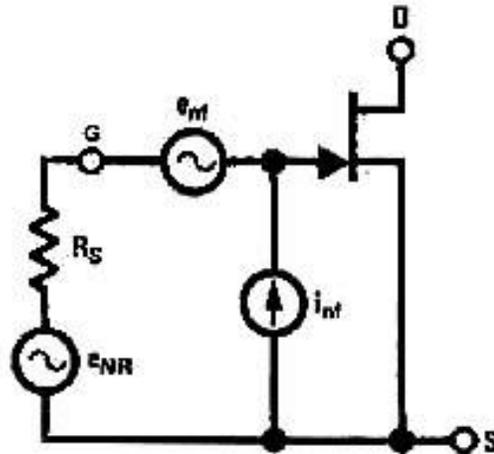


Figure 4. Simple JFET Noise Model

The input noise per unit bandwidth at some frequency may be calculated from the mean square sum of the noise sources (assuming the JFET noise sources are uncorrelated or independent of one another).

$$e_{nt}^2 = e_{nR}^2 + e_{nf}^2 + i_{nf}^2 R_s^2 \quad (6)$$

The total noise in the same bandwidth Δf , where the noise sources are independent of frequency, is simply:

$$V_{NOISE} = (e_{nt}^2 \Delta f)^{1/2} \quad (7)$$

Practically, noise sources are not frequency independent except resistor noise with no dc bias. The total input noise for the non-ideal case may be calculated by breaking the spectrum up into several small bands and calculating the noise in each band where the noise sources are nearly frequency independent. The total input noise would then be the RMS sum of the noise in each of the bands $N_1 \dots N_n$.

$$V_{NOISE} = (V_{N1}^2 + V_{N2}^2 + \dots + V_{Nn}^2)^{1/2} \quad (8)$$

THE DESIGN PROCESS

The final circuit configuration and suitable JFET will be determined by the external circuit constraints.

- 1) Minimum signal to noise ratio (maximum amplifier noise)
- 2) Type and magnitude of source impedance (resistive or reactive)
- 3) Amplifier input impedance requirements
- 4) Bandwidth and maximum frequency of interest
- 5) Maximum operating temperature
- 6) Stage gain
- 7) Power supply voltage and current limitations
- 8) Circuit configuration, single or dual device

The design procedure is dependent on the type of source and each case must be considered separately. Resistive sources will be considered first because they are the least restrictive for the preamplifier.

Resistive Sources

Preamplifiers for resistive sources are typically voltage amplifiers requiring a fixed input resistance and capacitance consistent with the maximum frequency of interest and source resistance. In most cases a resistor of the desired value connected between the gate and ground will satisfy

the input resistance requirement leaving the maximum input capacitance as the major concern.

The maximum amplifier input capacitance is a function of the JFET source resistor, input resistance, source capacitance and maximum frequency. The maximum allowable input capacitance will be used in eliminating unsuitable JFET geometrics and optimizing the circuit configuration. Sometimes the JFET geometry (or type) with the lowest noise may also have an input capacitance that makes it unsuitable. The JFET input capacitance should be considered before noise in high source resistance, wideband amplifier designs.

$$C_{in} \cong C_{rs} \left(1 + \frac{gm R_D}{1 + gm R_s} \right) + \frac{C_{gs}^*}{1 + gm R_s} \quad (9)$$

$$*C_{gs} = C_{is} - C_{rs}$$

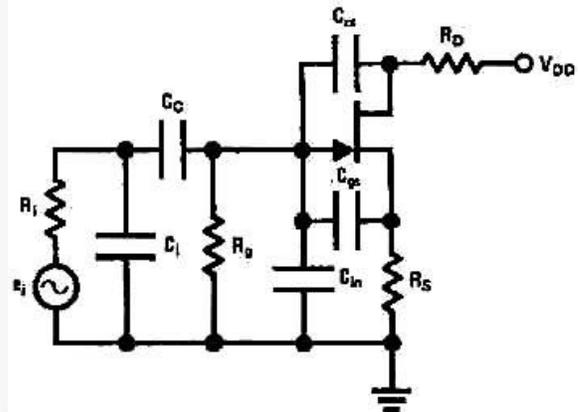


Figure 5. A Typical Resistive Source JFET Amplifier

If low input capacitance is required, a cascade configuration minimizes input capacitance and still allows high gain within a device type. The cascade configuration can also be used to reduce the voltage across a device, reducing device heating (for high current operation) and gate leakage currents when source impedances are very high.

Once the basic circuit configuration has been decided upon or dictated by gain, bandwidth and power supply limitations, the final JFET selection will be on noise. Redrawing the amplifier in Figure 4 with all of the noise sources, the total amplifier noise per unit bandwidth can be found.

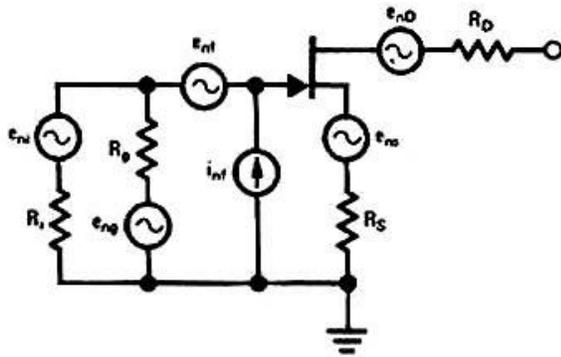


Figure 6. A Typical Resistive Source JFET Amplifier with Noise Sources

$$e_{nt} = \left[e_{nig}^2 + e_{nf}^2 + e_{ns}^2 + \frac{e_{nD}^2}{A_v^2} + i_n^2 (R_i // R_g)^2 \right]^{1/2} \quad (10)$$

- where: e_{nig}^2 = The noise of the parallel connection of R_i and R_g
 e_{nf}^2 = The noise voltage of the JFET
 e_{ns}^2 = The noise of the source resistor R_s
 $\frac{e_{nD}^2}{A_v^2}$ = The noise at the drain (thermal noise of the load plus the second stage noise)
 $i_n^2 (R_i // R_g)^2$ = The current noise contribution of the JFET

When the amplifier is operated at room temperature and moderate drain voltages, the current noise term is usually negligible with source resistances as high as 10 MΩ. Depending on the voltage gain of the stage, the drain circuit noise may be negligible, simplifying the input noise expression.

$$e_{nt} = (e_{nig}^2 + e_{nf}^2 + e_{ns}^2)^{1/2} \quad (11)$$

The final JFET selection will be based on the noise requirements from the maximum allowable noise V_{max} .

$$V_{MAX} = (e_{nf}^2 + e_{ns}^2)^{1/2} \quad (12)$$

Depending on V_{max} and e_{nf}^2 , the source resistor may have to be bypassed to ground to eliminate noise of the bias resistor.

Capacitive Sources

Preamplifiers for capacitive sources are primarily current amplifiers requiring very high input resistance and controlled input capacitance to match the source capacitance.

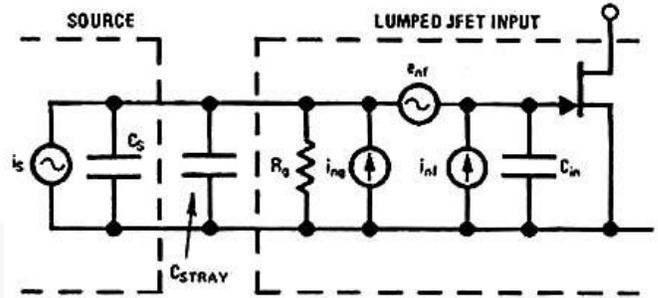


Figure 7. JFET Amplifier with an Inductive Source

The source capacitance should equal the sum of the preamplifier input capacitance and the stray capacitance for maximum frequency response and power transfer from the signal source. Assuming the gate resistor, R_g , is so large as to not load the capacitive source, the input noise voltage is:

$$e_{nt} \cong \left[e_{nf}^2 + (i_{nf}^2 + i_{ng}^2) \left(\frac{R_g^2}{1 + \omega^2 R_g^2 C^2} \right) \right]^{1/2} \quad (13)$$

where $C = C_s + C_{in}$

with an input signal of

$$e_s \cong i_s \left(\frac{R_g^2}{1 + \omega^2 R_g^2 C^2} \right)^{1/2} \quad (14)$$

When the source and input capacitance are matched, the final JFET geometry will be selected on two criteria: the noise voltage, e_n , and the current noise from the gate leakage, $I_{G(ON)}$ to optimize the signal to noise ratio. As in the resistive source case, the circuit configuration and JFET selection is an iterative process using all of the external circuit constraints, device parameters and limitations.

Inductive Sources

Amplifiers designed for inductive sources (including transformers) require fixed input resistances (as in the resistive source case) and controlled input capacitance (as in the capacitive source case). The input noise per unit bandwidth will rise with increasing frequency to a maximum value at resonance of the inductive source and the input capacitance or when the shunt resistance of the inductor is larger than the input resistance of the amplifier.

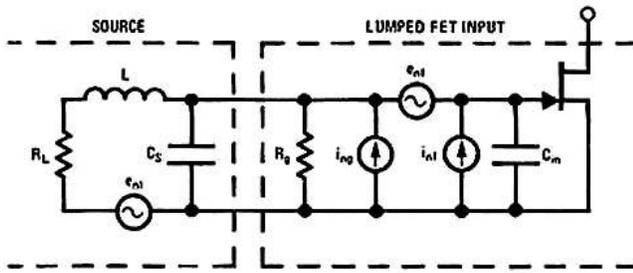


Figure 8. JFET Pre-amplifier with Capacitive Source

The inductive source amplifier is the most difficult to analyze due to the complex input impedance. The input noise per unit bandwidth is given by:

$$e_{nt}^2 = e_{nf}^2 + (i_{nf}^2)(|Z_{in}|^2) + 4 kT (\text{Re}(Z_{in})) \quad (15)$$

where $Z = X_{CIN} // R_g$

and $Z_{in} = Z // (Z_L + R_L)$

Usually the current noise of the JFET is negligible, simplifying the expression a little, but not much. The optimization process for inductive sources is very complex and it will require the spectrum to be broken up into several small bands to arrive at a final design. Generally, a JFET with a minimum noise voltage will be the proper choice.

Transformers may be used with JFET amplifiers to minimize noise with very low source impedances. Transformers have both drawbacks and advantages and both must be examined before a transformer design is chosen. Poor frequency response, susceptibility to mechanical and magnetic pickup and thermal noise head the list of disadvantages to be weighed against two very important advantages. First, the noise voltage is transformed by the turns ratio N ; second, the resistance is transformed by N^2 . These can be used to advantage by matching very low values of source resistance to a relatively noisy amplifier and still maintaining a good signal to noise ratio, i.e., the total noise at the source assuming an ideal transformer is

$$e_{nt}^2 = e_{nRs}^2 + \frac{e_{nAmp}^2}{N^2} \quad (16)$$

SUMMARY

Low noise amplifier design concepts have been introduced for the three basic types of sources. Basic parameters (C_{in} , e_n , g_m) were discussed that affect both circuit configuration and JFET type. There is no universal low noise JFET or circuit configuration that solves all problems. Each low

noise amplifier design is different and must be considered within its own frame-work of performance requirements.

SOME PRACTICAL LOW NOISE JFET INPUT CIRCUITS

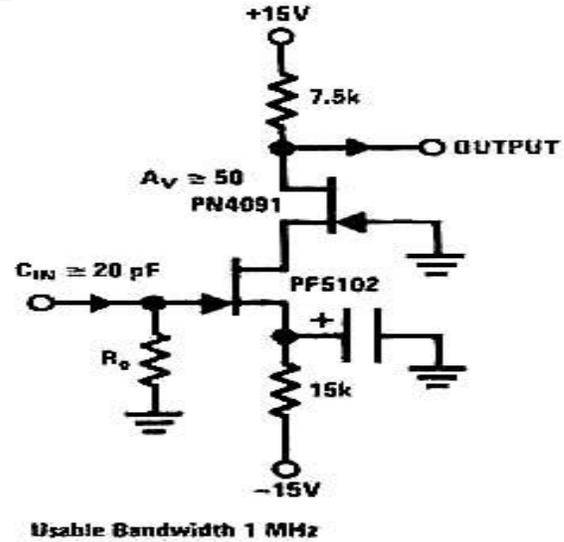


Figure 9. Wide Band, Low Input Capacitance, Very Low Noise Pre-amplifier

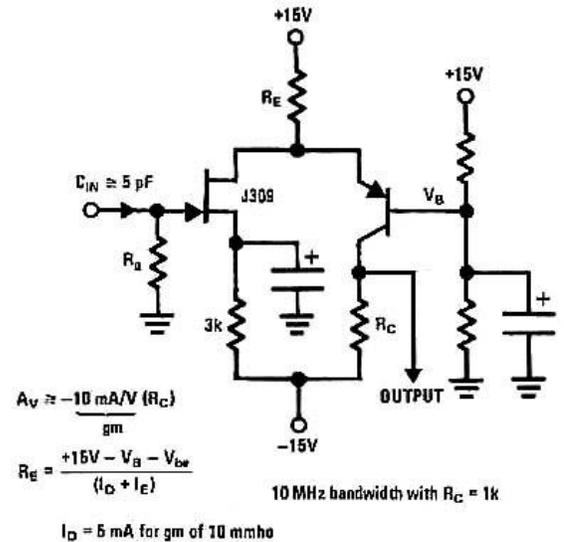


Figure 10. Low Noise, Very Low Input Capacitance Video Amplifier

APPENDIX A

NOISE PARAMETER CONVERSION

Noise Figure (NF) to an Effective e_n

It is more convenient to present noise data for bipolar transistors in the form of contours of constant noise figure at a fixed frequency or plots of noise figure versus frequency at a fixed source resistance due to large values of noise current (i_n). Noise figure must be converted to an effective noise voltage (e_n) for comparisons to be made between a BJT and a JFET or for signal to noise ratio calculations.

By definition:

$$NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise Power of the Source}} \quad (A1)$$

From equations 1 and 2, one finds the source noise power to be

$$\text{Source Noise Power} = \frac{e_{nR}^2 \Delta f}{R_S} \quad (A2)$$

for some resistance R_S .

Referring to Figure 4, the total output noise power at the input of the amplifier would be:

$$\text{Total Output Noise Power} = \frac{e_{nR}^2 \Delta f}{R_S} + \frac{e_{nf}^2 \Delta f}{R_S} + i_{nf}^2 R_S^2 \Delta f \quad (A3)$$

The noise figure (NF) can now be expressed in terms of the noise source generators, e_{nR} , e_{nf} and i_{nf} allowing an expression to convert noise figure (NF) to an effective noise voltage (e_n).

$$NF = 10 \log \left(1 + \frac{e_{nf}^2 + i_{nf}^2 R_S^2}{e_{nR}^2} \right) \quad (A4)$$

Yielding:

$$e_{nf}^2 + i_{nf}^2 R_S^2 = e_{nE}^2 = (10^{NF/10} - 1) e_{nR}^2 \quad (A5)$$

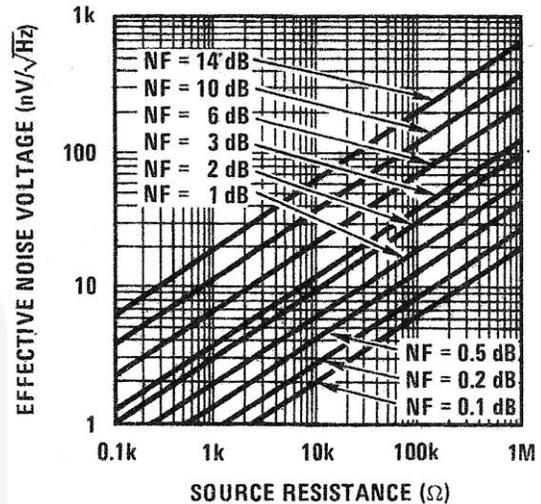


Figure 11. Effective Noise Voltage (e_{nE}) vs Noise Figure and Source Resistance (R_S).

Noise Resistance

The effective noise voltage density (e_n) and noise current density (i_n) are found directly by referring to Figure 1, and reading the values for the corresponding resistances.

$$e_{nR} = (4 KTR)^{1/2} \quad (A6)$$

$$i_{nR} = \left(\frac{4 KT}{R} \right)^{1/2} \quad (A7)$$

APPENDIX B

JFET Current Noise

At low frequencies the current noise and voltage noise sources are uncorrelated in JFETs with the current noise being pure shot noise due to gate leakage currents. As frequency is increased, the current noise also increases starting at frequencies as low as 50 kHz in some high capacitance device types.

It has been suggested and experimentally verified that the noise current at high frequencies is due to increased gate input conductance.

$$i_n^2 = 4 KT [\text{Re}(Y_{11})]^{-1} \quad (B1)$$

$\text{Re}(Y_{11})$ is available on high frequency JFET data sheet as the real portion of the common source input admittance parameters. In effect the channel noise is coupling to the gate circuit through the source-gate and drain gate capacitances. Hence low capacitance devices exhibit lower values of noise current at high frequencies than do high capacitance devices.

REFERENCES

- [1] A. Van der Ziel, "Noise," Prentice-Hall, 1964.
- [2] Richard S.C. Cobbold, "Theory and Applications of Field-Effect Transistors," John Wiley & Sons, 1970.
- [3] C.D. Motchenbacher and F.C. Fitchen, "Low Noise Electronic Design," John Wiley & Sons, 1973.

Author: John Maxwell, January 1976, Note 151

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