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AN-7010

Choosing Power Switching Devices for SMPS Designs

MOSFETs or IGBTs?

By Ron Randall, Staff Applications Engineer, Fairchild Semiconductor

Introduction

This article identifies the key parametric considerations for comparing IGBT and MOSFET performance in specific SMPS (Switch Mode Power Supply) applications. Parameters such as switching losses are investigated in both hard-switched and soft-switched ZVS (Zero Voltage Switching) topologies. The three main power switch losses: turn-on, conduction and turn-off are described relative to both circuit and device characteristics. The impact of diode recovery performance on hard-switched topologies is also discussed illustrating that diode recovery is the dominant factor determining MOSFET or IGBT turn-on switching losses.

This article also shows how device selection is complicated by the specific cooling system being utilized. For example, a single IGBT may perform well in a hard-switched PFC (Power Factor Correction) circuit with sufficient cooling heatsink; while, conversely, a design that mandates a marginal heatsink for cost or space reasons may require multiple parallel power MOSFETs. The conclusion reiterates that there is no single solution for choosing and applying IGBTs or MOSFETs in SMPSs and that each application merits careful analysis selecting an optimum switching device.

Historically, the off-line SMPS (Switch Mode Power Supply) industry has been driven by the power semiconductor industry's power component advancements. As the main power-switching devices, IGBTs, Power MOSFETs, and power diodes continually improve, there are corresponding—and significant——efficiency, size, weight and cost improvements in SMPS designs. Because of this direct component-to-application performance relationship, SMPS designers must compare the many pros and cons of the various semiconductor technologies to optimize their designs. For example, MOSFETs typically excel for lower power and higher frequency applications (i.e., power levels < 1000W and switching frequencies ≥ 100 kHz). But IGBTs have distinct advantages for lower frequency and higher power designs. This article compares an IGBT, the FGP20N6S2D SMPS2 and a MOSFET, the FCP11N60 SuperFET (from Fairchild Semiconductor) in an SMPS application. These products exemplify state-of-the-industry parts and they have comparable die size and identical thermal resistance $R_{\theta JC}$.

Turn-On Losses

The turn-on characteristics of IGBTs and power MOSFETs are quite similar, except that IGBTs have a longer voltage fall time. Referencing the basic IGBT equivalent circuit (Figure 1) the time required to fully modulate the minority carrier PNP BJT collector base region results in a turn-on voltage tail.

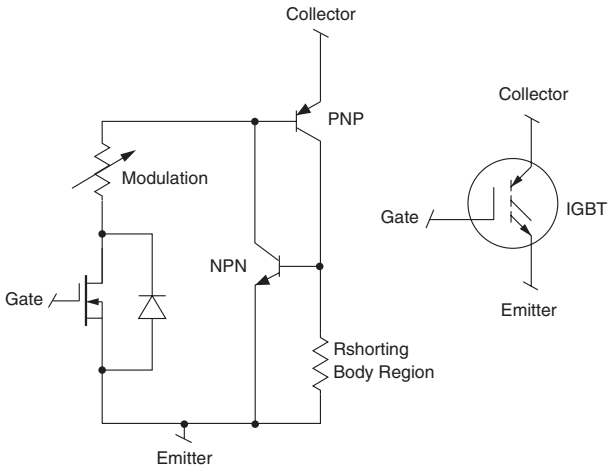

Figure 1. An IGBT Equivalent Circuit.

This delay results in a Quasi-Saturation effect wherein the collector-emitter voltage does not immediately fall to its $V_{CE(sat)}$ value[1]. This turn-on effect also results in a V_{CE} voltage bump under ZVS conditions at the point where the load current transitions from the co-packed inverse parallel diode to the IGBT collector. The Eon energy losses specified in datasheets is the time integral of $I_{collector}$ times V_{CE} in joules per switching cycle, and includes the additional losses associated with quasi-saturation.

Two Eon energy parameters, Eon1 and Eon2, are provided in IGBT datasheets. Eon1 is the energy loss without the losses associated with hard-switched diode recovery. Eon2 includes the hard-switched turn-on energy loss do to diode recovery and is measured by recovering a diode identical to the co-packed diode associated with the device. A typical Eon2 test circuit is illustrated in Figure 2. The test is performed with the diode at the same T_j as the DUT. The IGBT is switched through two pulses to measure Eon. The first pulse raises the inductor to the desired test current and the second pulse then measures the Eon loss recovering this current from the diode.

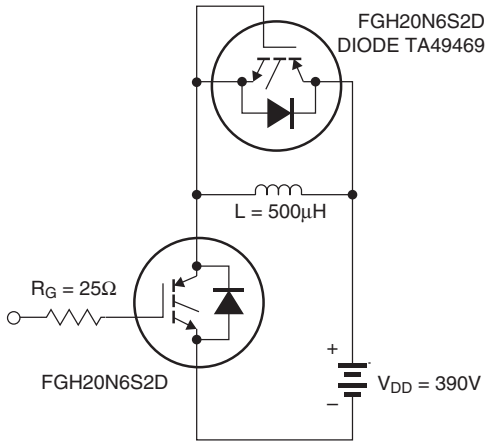

Figure 2. Typical Eon and Eoff Test Circuit.

Under hard-switched turn-on, the gate drive voltage and impedance and the recovery characteristics of the commutated diode determine the Eon switching loss. For circuits such as the conventional CCM (Continuous Current Mode) boost PFC circuit, the boost diode recovery characteristics are extremely important in controlling Eon (turn-on) energy losses. In addition to selecting a boost diode with minimal T_{rr} and Q_{RR}, it is also important to ensure that the diode has soft recovery characteristics. Softness, the ratio of t_b/t_a, has a considerable impact on the electrical noise and voltage spikes generated across the switching device. Snappy diodes with a rapid t_b period di/dt fall from $I_{RM(REC)}$ create large voltage spikes in the circuit parasitic inductances. These voltage spikes create EMI and can result in excessive reverse voltage across the recovering diode.

In hard-switched circuits, such as the full-bridge and 1/2 bridge topologies where the IGBT co-packed diode or the MOSFET body diode is conducting when the alternate switching device is turned on, the diode recovery characteristics determine the Eon loss. For this reason it is important to select MOSFETs with fast body diode recovery characteristics, such as the Fairchild's FQA28N50F FRFET™. Unfortunately, MOSFET parasitic, or body diodes, are relatively slow compared to state-of-the-industry discrete diodes. For hard-switched MOSFET applications, the body diode is often the limiting factor determining the SMPS operating frequency.

Typically, IGBT co-packed diodes are selected for compatibility with their intended applications. Slower ultra-fast diodes with lower forward conduction losses are co-packed with slower lower $V_{CE(sat)}$ motor drive IGBTs. Conversely, soft recovery hyper-fast diodes, such as the Fairchild Stealth™ series, are co-packed with the high frequency SMPS2 switched mode rated IGBTs.

Beyond selecting the right diode, a designer can control Eon losses by adjusting the gate drive turn-on source resistance. Decreasing the drive source resistance will increase the IGBT or MOSFET turn-on di/dt and decrease the Eon loss. The tradeoff is between Eon losses and EMI, since the higher di/dt will result in increased voltage spikes and radiated and conducted EMI. Selecting the correct gate drive resistance to meet a desired turn-on di/dt may require in-circuit testing and verification. A ballpark value may be determined from the MOSFET transfer curve, (Figure 3). Assuming the FET current will rise to 10 A at turn-on, and looking at the 25°C curve of Figure 3, the gate voltage must transition from 5.2 V to 6.7 V to reach 10 A and the average GFS is 10A / (6.7V–5.2V) = 6.7mhos.

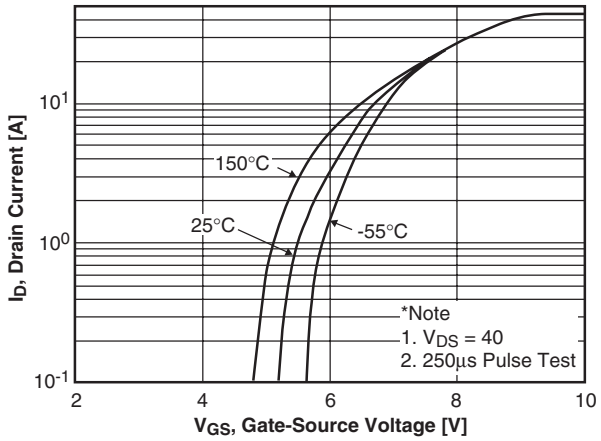

Figure 3. A MOSFET Transfer Characteristics.

$$R_{gate} = [V_{drive} - V_{GS(avg)}] \bullet \frac{G_{FS}}{(di/dt) \bullet C_{iss}}$$

Equation 1. Gate drive resistance for desired turn-on di/dt.

Applying this average G_{FS} value to Equation 1, with a gate drive of V_{drive} = 10V, a desired di/dt = 600A/µsec and typical FCP11N60 values $V_{GS(avg)}$ = 6V, C_{iss} = 1200pF; a 37Ω turn-on gate drive resistance is calculated. Since the instantaneous G_{FS} value is the slope in Figure 3, G_{FS} will vary during the Eon period, which implies a varying di/dt. The exponentially decaying gate drive current and decreasing C_{iss} as a function of V_{GS} also enter into this equation with an overall effect of surprisingly linear current rise.

Similar gate drive turn-on resistance may be calculated for the IGBT. Again $V_{GE(avg)}$ and G_{FS} may be determined from the IGBT transfer characteristic curve, and the C_{IES} value at $V_{GE(avg)}$ should be substituted for C_{iss}. The comparable calculated IGBT turn-on gate drive resistance is 100Ω. This higher Ω requirement is indicative of the higher IGBT G_{FS} and lower C_{IES}. A key point here is that gate drive circuit adjustments must be made for a transition from MOSFET to IGBT.

Conduction Losses

When comparing 600 V rated devices, IGBT conduction losses typically are less than an equivalent die size 600 V MOSFET. A qualifier is that the comparison should be made at appreciable collector and drain current densities and at the

desired worst-case operating junction temperature. For example, the FGP20N6S2D SMPS2 IGBT and FCP11N60 SuperFET both have an $R_{\theta JC}$ value of 1°C/W. Figure 4 compares conduction loss versus DC current at a junction temperature of 125°C. It shows that the MOSFET will have more conduction losses for DC currents greater than 2.92 A dc.

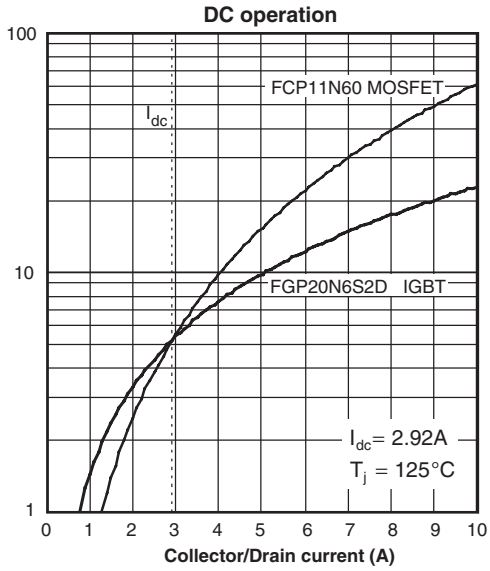

Figure 4. Conduction Losses DC Operation.

However, the DC conduction loss comparison in Figure 4 does not apply to most applications. In Figure 5, on the other hand, conduction losses are compared operating in a CCM, boost PFC circuit with a junction temperature of 125°C and Vac input of 85 V and 400 Vdc output. In this figure the MOSFET-IGBT crossover point is 2.65A RMS. For PFC circuit, AC input currents greater than 2.65A RMS, the MOSFET will have greater conduction losses. The 2.65A PFC AC input current equates to 2.29A RMS in the MOSFET as calculated by Equation 2. Boost switch RMS current in CCM PFC Circuit. The MOSFET conduction loss is calculated as an I^2R loss using the current defined by Equation 2. Boost switch RMS current in CCM PFC Circuit and the MOSFET 125°C $R_{DS(on)}$ This conduction loss may be further refined by accounting for the variation of $R_{DS(on)}$ as a function of drain current. This relationship is illustrated in Figure 6.

The impact on conduction losses may be determined as outlined in an IEEE article called *How to include the dependency of the $R_{DS(on)}$ of power MOSFETs on the instantaneous value of the drain current into the calculation of the conduction losses of high-frequency three-phase PWM inverters*, referenced below[2]. The impact of $R_{DS(on)}$ change as a function of I_D is minimal for most SMPS topologies. As an example, the impact of operating the FCP11N60 MOSFET in the PFC circuit to an I_D of 11A peak current, or two times the 5.5 A, its $R_{DS(on)}$,is specified at will increase the effective $R_{DS(on)}$ and conduction losses by 5%.

The $R_{DS(on)}$ characteristic illustrated in Figure 6 should be considered in topologies where the MOSFET conducts high pulse currents for very short duty-factors. If the FCP11N60 MOSFET is operated in a circuit with a 20A pulse at 7.5% duty-factor (i.e., 5.5A RMS), the effective $R_{DS(on)}$ will be 25% greater than the specified 0.32 Ω at 5.5 A.

$$Irms_{switch} = Iac_{RMS} \bullet \sqrt{1 - \frac{8 \bullet \sqrt{2}}{3 \bullet \pi} \bullet \frac{Vac}{Vout}}$$

Equation 2. Boost switch RMS current in CCM PFC Circuit

Where:

Iac_{RMS} is the PFC circuit RMS input current

Vac is the PFC circuit RMS input voltage

Vout is the DC output voltage

It is more complex to calculate the IGBT conduction loss in applications, such as a PFC circuit, where each switching period is at a different I_{CE}. This is because the $V_{CE(sat)}$ cannot be represented as a resistance voltage drop. A relatively straight-forward approach is to represent the IGBT $V_{CE(sat)}$ as a fixed V_{FCE} voltage in series with a resistor R_{FCE}. $V_{CE}(I_{CE}) = I_{CE} \times R_{FCE} + V_{FCE}$. The conduction losses may then be calculated as the product of the average collector current times V_{FCE}, plus the RMS collector current squared, times the resistance R_{FCE}. This technique is detailed in the articles referenced below[3,4], which include validation in a PFC circuit.

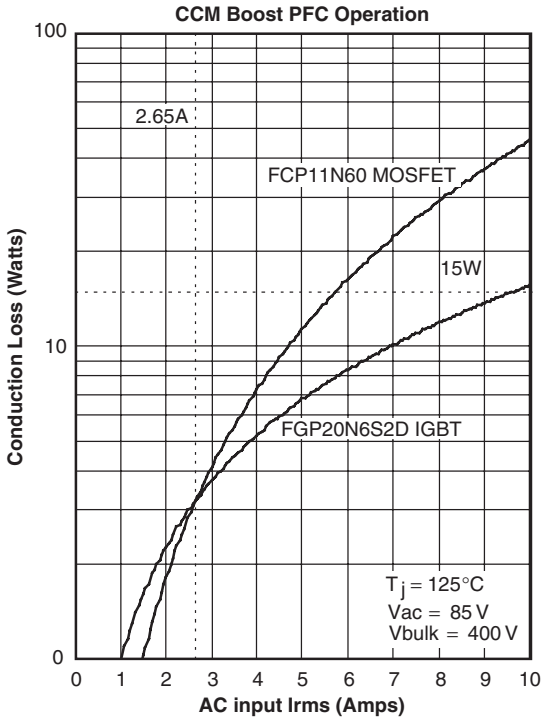

Figure 5. Conduction Losses in CCM Boost PFC Circuit.

The loss curves in Figure 5 consider only the IGBT and MOSFET conduction losses in a CCM PFC circuit. If, as an example, the design objective is to maintain the worst-case conduction losses too less than 15W then using the FCP11N60 MOSFET , the circuit is limited to 5.8A. However, the FGP20N6S2D IGBT can operate with an AC input current of 9.8A—which means it can handle 70% more power with this 15W conduction loss restriction.

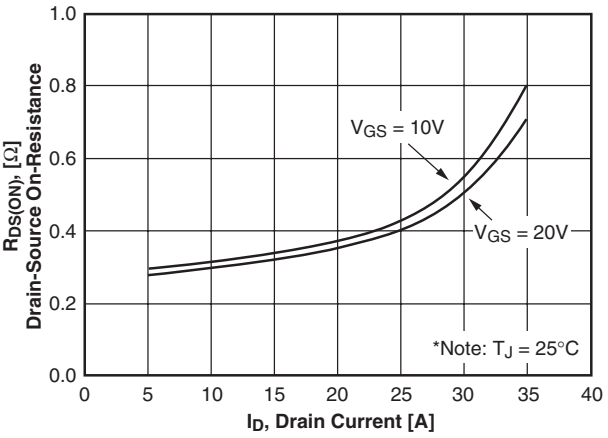

Figure 6. FCP11N60(MOSFET): $R_{DS(on)}$ vs. I_{DRAIN} and V_{GE}.

While IGBTs will exhibit lower conduction losses, most 600V IGBTs are PT (Punch Through) devices. PT devices have a NTC (Negative Temperature Coefficient) and will not share current when operated in parallel. PT devices may be paralleled with limited success by matching device $V_{CE(sat)}$, $V_{GE(TH)}$ (gate-to-emitter threshold voltage), and by mechanically packaging, such that the IGBT die temperatures will track closely. Conversely, the MOSFET has a PTC (Positive Temperature coefficient) that provides good current sharing.

Turn Off Loss

MOSFETs have considerably lower turn-off losses than IGBTs in hard-switched, clamped inductive operation. This is because of the IGBT tail current associated with clearing the minority carriers, which are associated with the PNP BJT (Figure 1). IGBT Eoff energy curves as a function of collector current and junction temperature (Figure 7) are provided in most IGBT datasheets. These curves are applicable for a fixed clamped inductive test voltage and include the tail current energy loss. Figure 2 illustrates the typical test circuit used for measuring IGBT Eoff as a function of I_{CE} and T_j. The Eoff test voltage, the V_{DD} in Figure 2, varies with manufacturer and the specific device's BV_{CES}. This test V_{DD} should be considered when comparing devices. Testing and operating at a lower V_{DD} clamp voltage will result in reduced Eoff energy loss.

Lowering the gate drive turn-off resistance will have minimal effect in reducing IGBT Eoff loss. As illustrated in Figure 1, once the equivalent majority carrier MOSFET is turned off there is still a $t_{d(OFF)I}$ storage time delay in the IGBT minority carrier BJT. Lowering the Eoff drive resistance will, however, reduce the risk of the Miller capacitance C_{RES} and turn-off V_{CE} dv/dt injecting a current into the gate drive that re biases the device into conduction causing multiple Eoff switching.

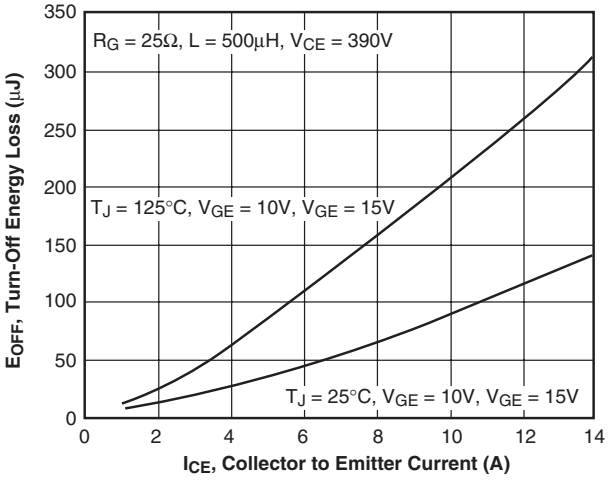

Figure 7. IGBT Eoff vs. ICE and T_j.

ZVS and ZCS (Zero Current Switching) topologies have advantage in reducing turn-off losses in both MOSFETs and IGBTs. The ZVS operation advantage is not as great in IGBTs since an Eoff tail bump current, albeit smaller, will still exist once the collector voltage rises to a potential that permits dissipation of excess stored charge. ZCS topologies produce the greatest IGBT Eoff performance improvement. Proper gate drive sequence, wherein the IGBT gate signal is not removed until the point of second collector current zero crossing, can have a marked improvement in IGBT ZCS Eoff reduction[5].

The MOSFET Eoff energy loss is a function of its Miller capacitance C_{rss}, the gate drive speed, gate drive turn-off source impedance, and parasitic inductance in the source power circuit path. The circuit parasitic inductance Lx, shown in Figure 8, generates a potential that increases the turn-off loss by limiting the current fall di/dt. At turn-off, the current falls at a di/dt determined by Lx and $V_{GS(th)}$. If, as an example, Lx = 5 nano-henries and $V_{GS(th)}$ = 4V the maximum rate current fall will be $V_{GS(th)}$ / Lx = 800A / μsec.

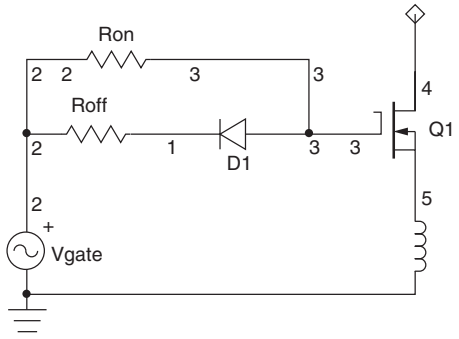

Figure 8. Gate Drive Circuit in Typical Hard-Switched Applications.

Gate Drive Requirements

While both MOSFETs and IGBTs have high gate impedance and are voltage-controlled devices, the minimum-drive voltage requirements are different. The minimum acceptable gate drive voltage is important, since falling below this value will result in switching from the "ON" state to a highly dissipative linear mode. Drive circuits for either device should be designed such that the gate drive does not fall below the minimum value under any condition. Good circuit-design hygiene mandates that a gate drive UFLO (Under Voltage Lock Out) circuit be incorporated to ensure that gate drive is removed for low drive voltage conditions to prevent the switching devices from entering the linear conduction mode.

When comparing the FGP20N60S2D and FCP11N60 gate characteristics, the FGP20N60S2D's V_{GEP} plateau voltage is 8 V max and the FCP11N60 $V_{GS(th)}$ threshold voltage is 5 V max. The FGP20N60S2D IGBT V_{GEP} value is meaningful since it is tested at an appreciable 7 A current. However, the FCP11N60 MOSFET $V_{GS(th)}$ voltage is measured at 250 µA and does not guarantee that the device will be "ON" at a V_{GS} of 5V. Further useful information may be obtained from the MOSFET's V_{GS} versus I_D on-region characteristic curve. For example, in order to guarantee that the FCP11N60 is "ON" for a 10 A load, the V_{GS} should be 6.5 V minimum. Parasitic gate capacitances heavily impact the switching characteristics of both MOSFETs and IGBTs. For the MOSFET the drain-to-gate C_{rss}, reverse transfer capacitance, in conjunction with the Gate drive source resistance, determines the rate of drain voltage fall at turn-on and rise at turn-off.

The IGBT collector-gate C_{RES} capacitance acts similarly by limiting the rate of V_{CE} fall at turn-on. At turn-off, the IGBT C_{RES} may cause multiple switching if the gate drive resistance Roff is not sufficiently small. In this case, the equivalent MOSFET (Figure 1) turns off, but the VCE does not rise until after the excess charge is cleared from the BJT. At that point, the rapidly rising collector voltage and C_{RES} may drive a current into Roff that re biases the N-channel MOSFET back into conduction.

The gate drive coulomb charge Q_G required to switch MOSFETs and IGBTs are very similar. The FGP20N60S2D IGBT Q_G = 30 nC for V_{CE} = 300 V, I_{CE} = 7 A and Vgate = 15 V. Gate charge for FCP11N60 is 40 nC for V_{DS} = 400 V, I_D = 11A and Vgate = 10 V.

In typical hard-switched applications, different gate drive turn-on and turn-off impedances are required, as illustrated in Figure 8. As previously described, turn-on resistance is typically set to control turn-on di/dt. The turn-off impedance is set much lower, particularly for MOSFETs where the switching speed can be greatly impacted by the speed at which the V_{GE} voltage is pulled to zero potential.

The FOM, or Figure of Merit, which is the gate charge $Q_{G(on)}$ times $R_{DS(on)}$ is often used for comparing MOSFETs; the lower the FOM, the better the devices performance. This comparison is only valid, however, if compared under identical conditions. That is typical parameter versus typical parameter or max versus max at the same T_j, V_{DS}, V_{GS} and I_D.

Thermal Management

One of the more critical parameters in optimizing SMPS component selection is the thermal system. If the SMPS will operate in a high thermal ambient, or has a marginal heatsink, the only solution may be to select a larger die size or to parallel power devices. Another key thermal factor is the thermal interaction between power devices. A good example is the boost diode and boost switch in a CCM boost PFC circuit. If the circuit is hard-switched then the primary switch loss is the Eon turn-on, which is predominantly a function of the boost diode. If the boost diode is closely coupled thermally to the boost switch, an interaction will occur. Eon loss in the switch will raise the boost diode temperature. This in turn will increase the diode I_{RRM} further increasing the switch Eon loss.

For hard-switched operating frequencies in the range of 50 kHz or greater, the cooling system often determines the choice between IGBTs and MOSFETs. If the design is below 50 kHz, and sufficient cooling is available, the IGBT may be the optimum choice. However, if the boost switch losses must be spread out over a broader area requiring device paralleling, the MOSFET should be chosen since its PTC characteristics will ensure load current sharing.

Conclusions

While IGBT and MOSFET gate drive requirements are similar, subtle differences in minimum required gate drive voltage and gate drive source resistance require adjustments when switching from one device to the other. There is no across-the-board solution when using power switching devices; circuit topology, operating frequency, ambient temperature and physical size constraints all play a part in determining the optimum choice. In ZVS and ZCS applications with minimized Eon losses, MOSFETs are capable of operating at higher frequencies because of their faster switching and lower turn-off losses. For hard-switched applications, the MOSFET parasitic body diodes recovery characteristics can be a detriment. Conversely, since IGBT co-pack diodes are matched to the specific application, excellent soft-recovery diodes are matched with the higher speed SMPS rated devices.

Endnotes

[1]Pittet, Serge and Rufer, Alfred *Analytical analysis of Quasi-Saturation Effect in PT and NPT IGBTs* PCIM Europe 2002 http://leiwww.epfl.ch/publications/pittet_rufer_pcim_02.pdf

[2]Kolar, J.W., Ertl, H., and Zach, F.C. (1998), *How to include the dependency of the Rds(on) of power MOSFETs on the instantaneous value of the drain current into the calculation of the conduction losses of high-frequency three-phase PWM inverters*, IEEE Trans. Ind. Electronics, Vol. 45, No.3, pp. 369–375, June 1998.

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