AND8072/D

Thermal Analysis and Reliability of WIRE BONDED ECL

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APPLICATION NOTE

INTRODUCTION

Normal operation of Integrated Circuits will cause electrical power, P, to be converted into heat by the die circuitry and thermally dissipated into adjacent materials. As the electrical system generates heat and the physical system thermally dissipates this heat, an operational equilibrium is reached after a stabilization period. This stable, operational junction temperature of the Integrated Circuit die is represented as Theta J or T_J, and is measured with reference to the temperature of ambient air, T_A.

Heat evolved in the electrical energy conversion by the die circuit (T_J) must be conducted away and dissipated by:

1. Conduction through the package case and connections into the printed circuit board

2. Conduction through the package case and connections into air

3. Radiance

The consequent local rise in temperature of the internal die accelerates failure mechanisms responsible for the eventual functional non−operation of the Integrated Circuit. These failure mechanisms predominantly determine the reliability of the Integrated Circuit and subsequent operational lifetime.

Factors affecting this failure mechanism and determination of the device reliability will be analyzed and discussed. Control and influence of some of the factors by the System Designer offer opportunities for increasing reliability and extending operational lifetime.
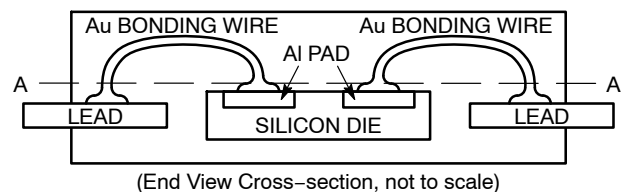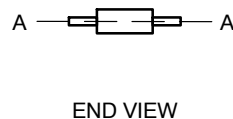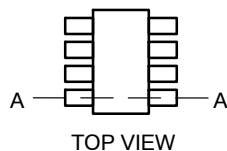
WIRE BONDED Device Failure Mechanisms

For the plastic DIP, SOIC, TSSOP, PLCC, TQFP, and other "WIRE BONDED" device packages, the dominant mode of failure is related to gold wire connecting the die pads to corresponding pin leads.

A good, operational wire bond electrically connects a package lead to the appropriate die circuit contact. Gold wire is used in the fabrication of die bond wire connecting a die pad to the package lead as shown in **Figure 1, Typical "WIRE BONDED" Integrated Circuit Bond Wire Connect Diagram**. Each gold wire is bonded at one end to the silicon circuit die at an aluminum pad, usually located near an outer edge. The other gold wire end is bonded to a device lead.

The very dominant mode of failure (>99.99% occurrence) related to operational lifetime in devices has been found historically to be die wire continuity, or "Opens". Device reliability theoretically follows a characteristic "bathtub" shaped curve consisting of:

1. High early failure rate attributed to defects and flaws in process and assembly,

2. Low rate during the operation lifetime due to die wire continuity,

3. High terminal rate associated with junction wearout.

Figure 1. Typical Integrated Circuit Bond Wire Connect Diagram

Normal operation of an integrated circuit device elevates the temperature of the device system, including die, aluminum pad, gold bond wires, device, board, and environment (air). It is the thermal elevation of die junction transferred from die to bond wires which causes aluminum from the die bond pad to migrate into the gold wire proportional to both temperature elevation and the duration of time elevated. The resultant intermetallic "gold–aluminum" contaminates a segment of the bond wire altering and raising the resistivity higher than the remaining pure gold segment, leading to localized heating. Aluminum migration accelerates with local temperature increase, concentrating the contamination. This failure process continues the thermal cascade until melting of the bonding wire occurs and opens the wire connection. When a gold bond wire fails, the discontinuity is usually located close to the aluminum die pad.
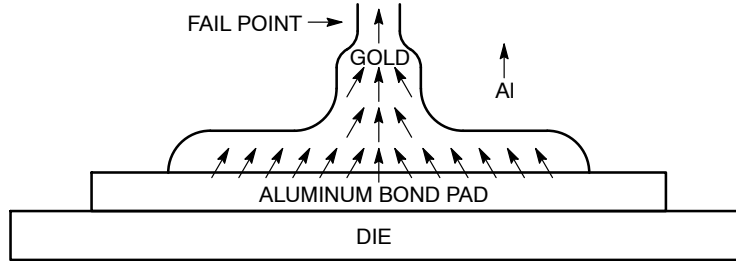

Figure 2. Aluminum Migration from the Die Bond Pad into the Gold Wire

Bond Failure Rate

Device failure rate is benchmarked at 0.1%, or 1 bond failure per 1000 bonds in Reliability calculations. This is based on the special Arrhenius equation **(Eq. 1)** expressing junction temperature as the bond failure rate benchmark of 0.1%:

$$T_{hours} = (6.376 \times 10^{-9})\ell^{[11554.267 / (273.15+T_J)]} \quad \text{(Eq. 1)}$$

Where:

T_{hours} = Time in hours to 0.1% bond

T_J = Device junction temperature °C.

Operational Lifetime and Maximum Acceptable Junction Temperature

The bond failure rate equation above renders a table of operational device lifetimes based on various junction temperatures (see **Table 1: T_J versus Time to 0.1% Bond Failure**. The maximum acceptable junction temperature is considered to be 140°C, since this predicts the 0.1% bond failure rate occurs after 8,900 hours, or one year of continuous service. The determination of T_J indicates operational device lifetime.

Table 1. T_J VERSUS TIME TO 0.1% BOND FAILURE

T_J, Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Junction Temperature Determination

Operating die junction temperature results from the total electrical power converted on chip, P_D, and the total physical thermal transfer resistance to ambient temperature T_A. This thermal resistance from the die to ambient temperature is defined as θ_{JA}, according to equation **Equation 2**:

$$T_J = (P_D)(\theta_{JA}) + T_A \quad \text{(Eq. 2)}$$

Where:

T_J is junction temperature

T_A is ambient air temperature

P_D is device total power dissipation

θ_{JA} is device thermal resistance, junction to ambient

The operating lifetime is determined by selecting T_J in Equation 2. The Power Dissipation, P_D, and Thermal Resistance, θ_{JA} in Equation 2 will be discussed as sections:

SECTION 1: P_D, Power Conversion Dissipation

SECTION 2: θ_{JA}, Device Thermal Resistance, Junction to Ambient

T_A, Ambient Air Temperature

SECTION 1
P_D, POWER DISSIPATION

The total device power dissipation, $\Sigma \mathbf{P_D}$, is calculated from summing the internal device electrical power conversions: $\mathbf{P_{Dstatic}}$, $\mathbf{P_{Doutput}}$, and possibly $\mathbf{Pd_{Rterm(internal)}}$ found on some devices. Refer to **Figure 3: P_D, Device Power Dissipation,** and Equation 3. Note the device input currents are not considered due to their very small magnitudes.

$$\Sigma P_D = \Sigma P_{Dstatic} + \Sigma P_{Doutput} + Pd_{Rterm} * \qquad \text{(Eq. 3)}$$

Where:

$$\Sigma P_{Dstatic} = \Sigma(I_{EE} \times |V_{CC} - V_{EE}|) \qquad \text{(Eq. 4)}$$

$$\Sigma P_{Doutput} = \Sigma(I_{(output)}^2 \times Z_{(output)}) \qquad \text{(Eq. 5)}$$

$$* \ \Sigma Pd_{Rterm(internal)} = \Sigma(Pd_{VIH} + Pd_{VIL}) \qquad \text{(Eq. 6)}$$

(* if present internally on the inputs)
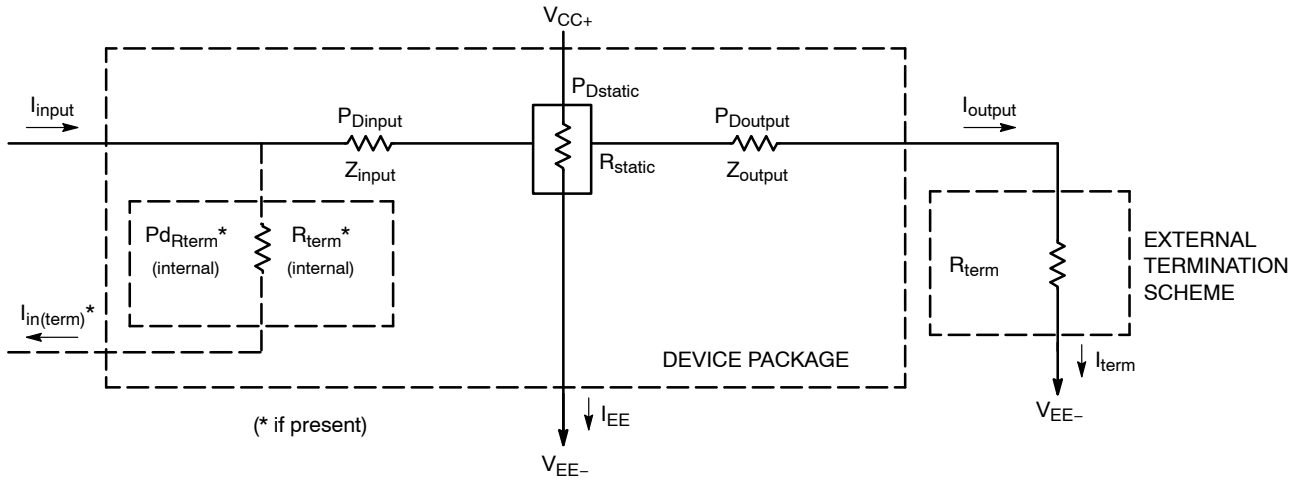
Figure 3. P_D, Device Power Dissipation

$\Sigma P_{Dstatic}$: STATIC POWER DISSIPATION:

$$\Sigma P_{Dstatic} = \Sigma(I_{EE} \times |V_{CC} - V_{EE}|) \qquad \text{(Eq. 4)}$$

The first internal power conversion, **$\Sigma P_{Dstatic}$** (Eq. 4), typically represents the product of a spec current, I_{EE}, and the voltage potential developed across the two power supplies, the (more) positive supply: V_{CC}; and the (more) negative supply, V_{EE}. I_{EE} does not include output or load currents and varies little across the operating frequency range. As stated within the Data Sheet limit tables, there is a min and max. Output currents can vary from zero (open) to the pin limit (50 mA) depending on the termination in use.

For example, the **$P_{Dstatic}$** of MC10LVEP16 operating from a V_{CC} of 2.5 V and V_{EE} of 0.0 V:

$$P_{Dstatic} = \Sigma(I_{EE} \times |V_{CC} - V_{EE}|)$$
$$= 22 \text{ mA} \times 5.0 \text{ V}$$
$$= 110 \text{ mW}$$

Of course, the **$P_{Dstatic}$** of MC10LVEP16 must be summed with the **$\Sigma P_{Doutput}$** to determine ΣP_D as per Eq. 3.

Some devices (such as LVEL90, LVEL91, E1651, E1652, etc.) will require three unique supplies (V_{CC}, GND, & V_{EE} or V_{CC1}, V_{CC2}, & V_{EE}) and will specify two unique currents, **I1** and **I2**, as indicated in **Equation 4a.**

$$\Sigma P_{Dstatic} = P_{D1} + P_{D2} + ... \qquad \text{(Eq. 4a)}$$

$$\Sigma P_{Dstatic} = (I1 \times |V_{CC1} - V_{EE1}|) + \qquad \text{(Eq. 4b)}$$
$$(I2 \times |V_{CC2} - V_{EE2}|) + ...$$

Spec currents may be from V_{CC1} to GND, V_{CC2} to GND, or from GND to V_{EE}. Refer to **Figure 4: Power Currents in Three Supply Devices**. Each current and respective voltage potential will determine a power conversion dissipation. All dissipations must be summed for the total power dissipation.
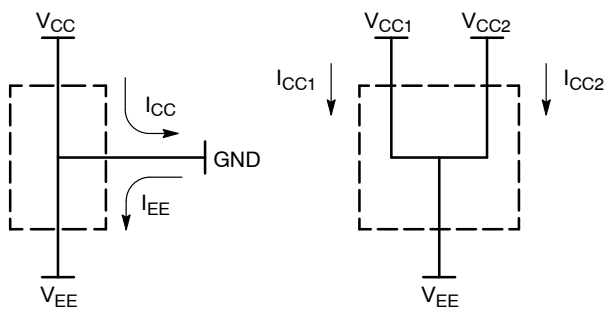
Figure 4. Power Currents in Three Supply Devices

An example would be the **$P_{Dstatic}$** of MC100EL91, operating from a V_{CC} of 5.0 V and a V_{EE} of −5.0 V:

$$\Sigma P_{Dstatic} = P_{D1} + P_{D2} + ...$$
$$= 55 \text{ mW} + 140 \text{ mW}$$
$$= 190 \text{ mW}$$

Where:

$$P_{D1} = (I_{CC} \times |V_{CC} - GND|)$$
$$= 11 \text{ mA} \times 5.0 \text{ V}$$
$$= 55 \text{ mW}$$

$$P_{D2} = (I_{EE} \times |GND - V_{EE}|)$$
$$= 28 \text{ mA} \times 5.0 \text{ V}$$
$$= 140 \text{ mW}$$

Of course, the **$\Sigma P_{Dstatic}$** of MC100EL91 must be summed with the **$\Sigma P_{Doutput}$** per Eq. 3 to determine **ΣP_D**.

Non−ECL Circuitry

When any non−ECL output circuitry is present, such as in the TTL and LVTTL/LVCMOS translators, both the static ECL and non−ECL type dissipation contributions to **$\Sigma P_{Dstatic}$** must be separately determined and summed as Eq. 4c:

$$\Sigma P_{Dstatic} = P_{Dstatic(ECL)} + P_{Dstatic(non-ECL)} \quad \text{(Eq. 4c)}$$

An example would be the **$P_{Dstatic}$** of the TTL output translator, MC100EPT25, operating from a V_{CC} of 3.3 V, a V_{EE} of −5.0 V, and a GND of 0.0 V. A signal duty cycle of 50% is assumed and typical currents:

$$\Sigma P_{Dstatic} = P_{Dstatic(ECL)} + P_{Dstatic(non-ECL)}$$
$$= 80 \text{ mW} + 55 \text{ mW}$$
$$= 135 \text{ mW}$$

Where:

$$P_{Dstatic(ECL)} = (I_{EE} \times |GND - V_{EE}|)$$
$$= 16 \text{ mA} \times 5.0 \text{ V}$$
$$= 80 \text{ mW}$$

$$P_{Dstatic(non-ECL)} = ((I_{CCH} + I_{CCL})/2) \times (|V_{CC}-GND|)$$
$$= 22/2 \text{ mA} \times 5.0 \text{ V}$$
$$= 55 \text{ mW}$$

…and of course, the **$\Sigma P_{Dstatic}$** of MC100EPT25 must be summed with the **$\Sigma P_{Doutput}$** per Eq. 3 to determine **ΣP_D**.
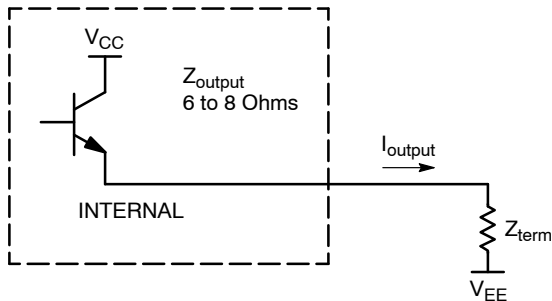
P$_{Doutput}$: OUTPUT STRUCTURE POWER DISSIPATION:

$$\Sigma PD_{output} = \Sigma(I_{(output)} \times V_{(output)}) + \qquad \text{(Eq. 5)}$$
$$\Sigma P_{D(dynamic)}$$

Where:

$V_{(output)}$ is V_{OH} or V_{OL}
$I_{(output)} = V_{(output)} / Z_{term}$

The device electrical power conversion, **P$_{Doutput}$**, results from the output termination current, I_{output} flowing through the output structure, Z_{output}, per **Figure 5: Typical ECL Output.** An ECL OUTPUT structure has 6 to 8 ohms internal impedance, whereas the internal impedance of a TTL output structure may vary considerably.

Figure 5. Typical ECL Output

Only the internal heat associated with the output structure, **P$_{Doutput}$** is added to the total thermal load as I_{output} current passing through the Z_{term} dissipates heat externally. Of course, the physical location of Z_{term} heat could affect a device's total thermal management. Note the device's input currents are not considered due to their very small magnitudes.

An average single output line current, I_{output}, may be calculated using Z_{term}, (the external user selected termination), spec output voltages (V_{OH} and V_{OL}) as shown in Eq. 5a. and frequency.

Duty cycle (HIGH to LOW level ratio) in a single line is a co−factor, but assuming the signal is 50%, then:

$$I_{output(typ)} = ((V_{OH} + V_{OL})/2)/Z_{term} \qquad \text{(Eq. 5a)}$$

Where:

V_{OH} = spec Voltage Output High
V_{OL} = spec Voltage Output LOW
Z_{term} = termination impedance

In the differential pair termination, the two lines will essentially be in complimentary states, but the average current in a differential pair is 2X a single line. For example, consider the MC10EP016 TCbar output (pin 12) and:

1. V_{CC} = 3.3,
2. V_{EE} = 0.0,
3. 85°C,
4. Z_{term} = 150 Ohms

generates an I_{output}:

$$I_{output(typ)} = ((2.4 + 1.6)/2)/150 \text{ ohms} \qquad \text{(Eq. 5b)}$$
$$= 13.3 \text{ mA}$$

The 13.3 mA average current applies to both lines in the differential pair, creating an average total of 26.6 mA, typical I_{output}.

This single line average of 13.3 mA I_{output} current passing through the internal output transistor generating P$_{Doutput}$.

$PD_{(dynamic)} = f * C_{load} * V_{swing} \char`^ 2$; usually neglected. Substituting the termination current from Eq. 5b into Eq. 5, and using typical V_{OH} of 2.4 V and a V_{OL} of 1.6 V, then yields the nominal power dissipation for a single output line:

$$= 0.013 \times ((3.3 - 2.4) + (3.3 - 1.6)/2) = 16.9 \text{ mW}$$

or 33.8 mW per diff pair.

In a typical MC100LVEP16, V_{CC} = 2.5, V_{EE} = 0.0, at 85°C, with Z_{term} = 100 ohms, the internal single output line generates **P$_{Doutput}$** per Eq. 5 and 5a:

$$P_{Doutput} = (I_{(output)} \times V_{(output)})$$
$$= (((V_{OH} + V_{OL})/2)/Z_{term}) \times ((V_{OH} + V_{OL})/2)$$
$$= (((1.6 + 0.8)/2)/100) \times ((1.6 + 0.8)/2)$$
$$= 14.4 \text{ mW}$$

per line or 28.8 mW per diff pair.

The MC100LVEP16 **ΣP$_{Dstatic}$**, of course, must be summed with the **ΣP$_{Doutput}$** per Eq. 3 to determine **ΣP$_D$.**

Non ECL ΣP$_{Doutput}$

A non ECL output is typically not subjected to ECL termination schemes. Still, the total **P$_{Doutput}$** (TTL) thermal contribution to the device may be calculated from the Output current (I_{output}) and the output impedance Z_{output} per Eq. 5. Generally, a TTL $Z_{(output)}$ is about 30 ohms in the High and 5 ohms when Low. A notable exception is the MC10/100H646 with about 7 ohm (internal output) impedance for both HIGH and LOW states. The MC10/100H646 output is designed to terminate with a series 43 ohm resistor in 50 ohm impedance traces. Power calculations over the frequency range is indicated in the MC10/100H646 data sheet (Figure 2).

The device P$_{Doutput}$ may be determined as:

$$P_{Doutput} = f * C_{load} * V_{swing}^2 \qquad \text{(Eq. 7)}$$

Where:

V_{swing} = signal $V_{OH} - V_{OL}$
f = frequency
C_{load} = load capacitance

This is multiplied by the number of outputs for total **P$_{Doutput}$**. The **ΣP$_D$** results from the sum of **ΣP$_{Dstatic}$** with the **ΣP$_{Doutput}$** per Eq. 3.

Pd$_{Rterm(internal)}$: (if present) INPUT R$_{term}$ POWER DISSIPATION:

$$\Sigma Pd_{Rterm} = \Sigma(PdV_{IH} + PdV_{IL}) \qquad \text{(Eq. 6)}$$

Where:

$$PdV_{IH} = I_{term} * \Delta V_{IH}$$
$$PdV_{IL} = I_{term} * \Delta V_{IL}$$

The R_{term} power dissipation, Pd_{Rterm}, results from signal currents through internal impedance matching resistors of 50 ohms, located internally. Two configurations are in use:

1. Internal Termination Combo Pin (see Figure 6)
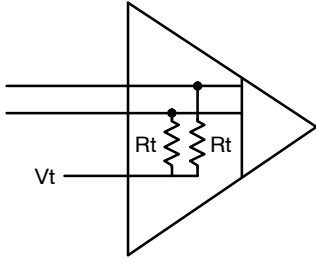2. Internal Termination Singulated Pins (see Figure 7)

Figure 6. Internal Termination Combo Pin

When the Internal Termination Combo pin, Vt, of Figure 6 is connected to a V_{TT} sinking power supply ($V_{CC} - 2.0$ V) and a signal, V_{IH} to V_{IL}, is applied, the internal resistors will draw current according to the equations:

$$IV_{IH} = (V_{IH} - V_{TT})/ Rt$$
$$IV_{IL} = (V_{IL} - V_{TT})/ Rt$$

The Rt values are 50 ohms and $V_{TT} = V_{CC} - 2.0$ V:

$$PdV_{IH} = \frac{(I_{term})(\Delta V_{IH})}{50} \cdot (V_{IH}(V_{CC} - 2.0))$$

$$PdV_{IL} = \frac{(I_{term})(\Delta V_{IL})}{50} \cdot (V_{IL}(V_{CC} - 2.0))$$

When $V_{CC} = 3.3$ V, the $V_{TT} = 1.3$ V, and when typical LVPECL levels of $V_{IH} = 2.4$ V & V_{IL} 1.6 V, are applied:

$$\begin{aligned} PdV_{IH} &= ((2.4 - 1.3)/50) * (2.4 - 1.3) \\ &= (1.1/50) * 1.1 \\ &= 24.2 \text{ mW} \end{aligned}$$

$$\begin{aligned} PdV_{IL} &= ((1.6 - 1.3)/50) * (1.6 - 1.3) \\ &= (0.3/50) * 0.3 \\ &= 9.8 \text{ mW} \end{aligned}$$

$$Pd_{Rterm} = 24.2 + 9.8 = 34 \text{ mW}$$

With standard (800 mV) signal amplitude, this value does not change with V_{CC}, since V_{TT} voltage remains referenced to V_{CC}.

The second configuration, Figure 7: Internal Termination Singulated, allow greater circuit versatility but still dissipates a thermal contribution to the device according to:

$$\Sigma Pd_{Rterm} = I_{term} * V_{term}$$

Where:

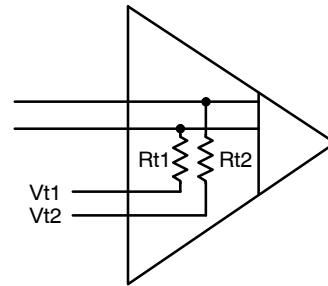$$I_{term} = (V_{in} - Vt) / Rt$$
$$V_{term} = V_{in} - Vt$$

Figure 7. Internal Termination Singulated

SECTION 2

θ$_{JA}$

As per Eq. 2, the **θ$_{JA}$** is multiplied by the total power dissipated, P$_D$, then added to the ambient air temperature, T$_A$, to determine T$_J$, junction temperature.

$$T_J = (P_D)(\theta_{JA}) + T_A$$

The following table lists the junction to ambient and junction to case temperature rise for several device packages.

Table 2. PACKAGE THERMAL CHARACTERISTICS

Package	Leads	Case	θJA Still Air 0.0 LFPM (°C/W)	θJA 500 LFPM (°C/W)	θJC Std. Bd. (°C/W)
FCBGA	16	489	149	127	
TSSOP	8	948R	185	140	41−44
	16	948F	138	108	33−36
	20	948E	90	60	30−35
	28	948A	76	60	25
SOIC	8	751	190	130	41−44
	16	751B	100	60	33−36
	20 WIDE	751D	90	60	30−35
PLCC	20	775	35	42	
	28	776	63.5	43.5	22 − 26
DIL	16	648	80		50
	24	724	75		50
MICRO−10	10	846B	177	132	40
DFN	8	506AA	129	84	
QFN	16	485G	42	35	4
	20	485E	47	33	18
	24	485L	37	32	11
	32	488AM	31	27	12
	52	485M	25	19.6	21
LQFP	32	873A	74	61	12−17
	52	848D	35.6	30	21
	64	848G	35.6	30	3.2−6.4

*See Appendix A

GREEN Stand−by Mode in NECL:

Standard "two−supply" ECL devices using V$_{CC}$ and V$_{EE}$, may, in NECL mode only, safely conserve system power consumption during non−functional periods by shutting down the V$_{EE}$ (Negative) supply (to 0.0 V) with no ill effects. This is NOT acceptable for devices operating in PECL or LVPECL mode.

System Considerations:

The following items are mentioned as other potential issues when determining a complete thermal performance and behavior for a board or system, although a detailed consideration of each will not be present:

1. Package mount:
   − package leads and mounts heat conduction (i.e. soldered versus non−soldered)
   − copper traces conduction and area
   − thermally conductive adhesive
2. Board material thermal conduction
   − planes thickness, material, and thermal transfer
3. Device locations and topology on board
4. Airflow:
   − forced−air (temperature, humidity, velocity)
   − parallel verses transverse
   − turbulence
   − blockages
5. Heat sinks (external)

Appendix A:

θ_JC of a 52 TQFP?

Thermal analysis of the 52 TQFP was conducted on a one layer copper clad (0.035″, "1 oz." type) FR4 fiberglass board, 3″ X 3″ X 0.0625″, 27 mil traces, with devices soldered in place.

For the 52 TQFP (MC100LVE222) in 0 l fpm (still air):

θ_{JA} is considered to be between 69−71°C/W

θ_{JC} is considered to be between 8.1 (Oil Bath Immersion Method) and 15 (Top Center Probe Method) °C/W.

Any heat sink calculations should be based on the Top Center Probe Method values.