Optimizing the LiDAR Signal Chain, Application Note

Sensors and Integrated Processing from onsemi and LeddarTech®

AND90101/D

INTRODUCTION

Direct Time of Flight (dToF) pulsed LiDAR is a measurement technique which calculates the time delay between a transmitted signal pulse and its return echo(es). dToF is suitable for both short− and long−range depth sensing applications. It offers faster acquisition rates and the ability to measure multiple echoes, allowing for detection of multiple objects in a return path. SiPM detectors from **onsemi** enable best LiDAR performance and provide benefits such as low operating voltage and excellent uniformity compared to legacy detectors such as APDs. However, when it comes to sensor readout, system designers are faced with the challenge of either creating their own discrete readout chain from off−the−shelf components or having to develop a custom ASIC.

LeddarTech provides off−the−shelf, integrated readout solutions. The benefit is a lower cost per channel and significant BOM and board size reduction compared to discrete solutions. Devices such as the LCA3 LeddarEngine™, which combines a LiDAR core SoC with patented signal processing software, can be used to amplify and digitize signals from various detectors including SiPMs and APDs.

In this application note we will present the use of the unique **onsemi** Fast output of the ARRAYRDM−0116A10−DFN connected to the LCA3 front end for simple, cost−effective readout and digitization of 16 channels simultaneously. This note will provide a comparison of the sensors available today, the various readout architectures and the benefits of full waveform digitization.

As part of this collaboration, **onsemi** and LeddarTech have developed and validated a reference design to enable our customers to evaluate the benefits and get working quickly with both technologies.

SENSORS FOR LIDAR

Highly sensitive sensors are required for LiDAR applications. PIN diodes and Avalanche Photodiodes (APDs) are linear−mode detectors that provide an output proportional to the amount of incoming light. Both require a certain accumulation of photons prior to reaching a threshold that can be detected as an object reflection. These legacy detectors are fast being replaced with higher performance sensors, which are sensitive down to single photon level built on single photon avalanche diodes (SPADs). Examples of these sensors include Silicon Photomultipliers (SiPMs), SiPM Arrays, and SPAD Arrays. At **onsemi**, these products are manufactured in a CMOS process offering tight part−to−part uniformity, low voltage operation, and very high gain. These sensor traits are desirable for low−cost and high−performance LiDAR that can be mass−produced in large volumes.

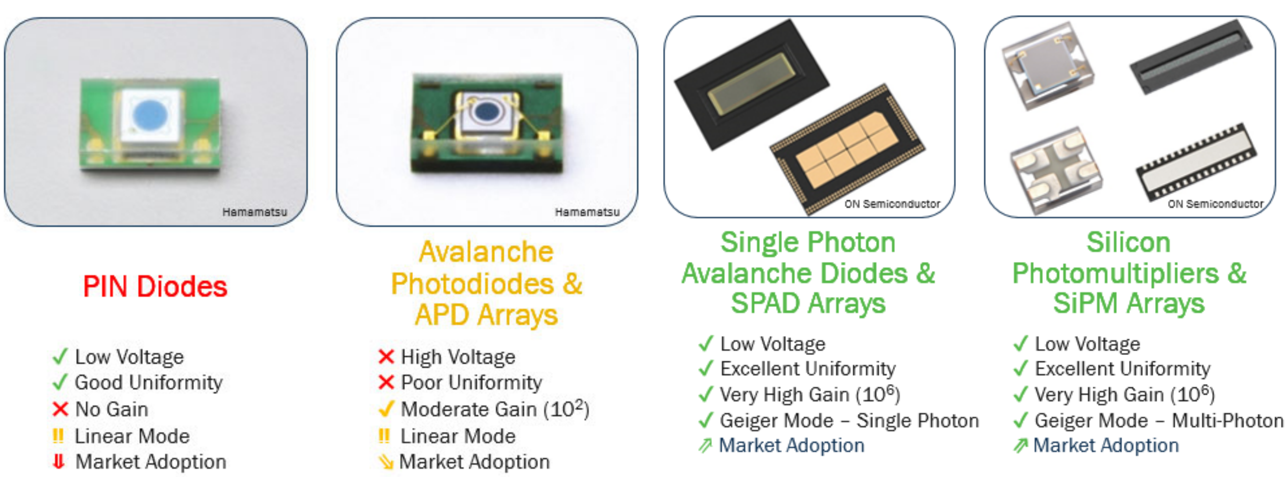

Figure 1. Sensors for Direct Time of Flight LiDAR

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How a SiPM Works

The SiPM consists of an array of microcells. Each microcell consists of a Single Photon Avalanche Diode (SPAD) and a quench resistor. **onsemi** SiPMs have 3 terminals; cathode, anode and Fast output. For further details of SiPM technology, please refer the [Introduction to the Silicon Photomultiplier] application note. The SiPM circuit structure and circuit schematic symbol are shown in the figure below.

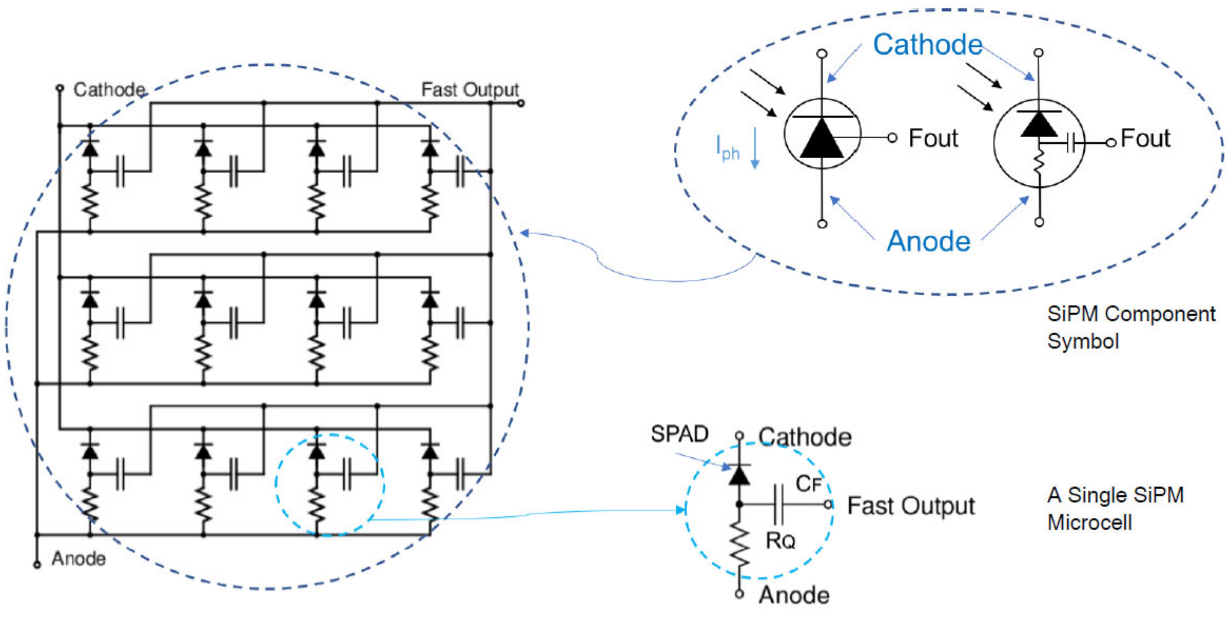


Figure 2. SiPM Simplified Schematic

onsemi Fast Output

The Fast output is unique to **onsemi** SiPM products. This is a capacitively coupled output within each microcell and all the Fast outputs within a SiPM are connected in parallel. The Fast output is a voltage pulse where the pulse amplitude is proportional to the number of microcells that have triggered. Due to the short pulse width, the Fast output is not constrained by the SiPM recovery time and allows for detection of higher photon count rates. As the Fast output is AC coupled, it does not carry any DC information.

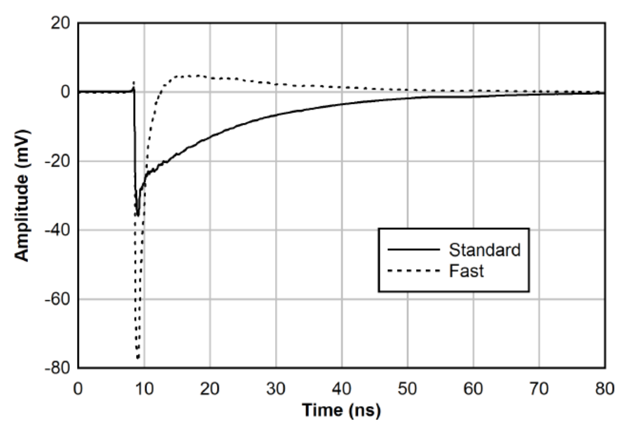


Figure 3. Standard and Fast Output Pulse Comparison

ArrayRDM−0116A10−DFN

Figure 4. ArrayRDM−0116A10−DFN

The ArrayRDM−0116A10−DFN is a 1 x 16 monolithic SiPM array designed for scanning LiDAR applications. Microlens technology is used to maximize the PDE while minimizing the noise. In order to meet the requirements for automotive LiDAR applications, this product is qualified to the AEC−Q102 standard.

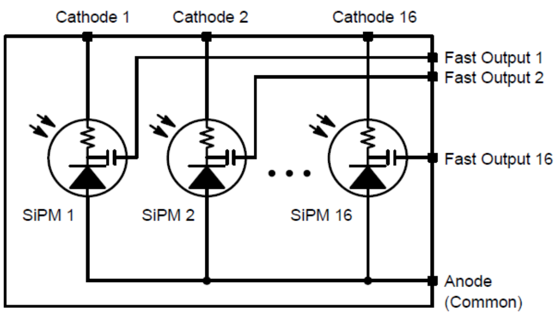


Figure 5. Array Schematic Showing Pixel Connections

Table 1.

Parameter	Min	Typ	Max	Unit	Comment
PDE @ 905 nm	–	15	–	%	
Dark Count Rate	–	30	–	kcps	Per pixel
Optical Crosstalk	–	25	–	%	
Gain	–	0.8E6	–		
90% − 10% Recovery Time	–	28	–	ns	
10% − 90% Rise Time	–	0.25	–	ns	
Fast Output Pulse Width	–	1	–	ns	
Breakdown Voltage (Vbr)	–	21.7	–	V	
Overvoltage (Vov)	–	12.3	14.3	V	
Operating Bias (Vop)	Vop = Vbr + V_{OV}				

The ArrayRDM−0116A10−DFN is formed of a linear array of 16 SiPM pixels and housed in a 36−pin DFN package. Figure 5 shows the sensor array schematic. The signals from each pixel can be accessed either via the pixel cathode or Fast output. The common anode is also available and allows the provision of a single bias supply for all 16 pixels.

Advantages of the ArrayRDM−0116A10−DFN in a LiDAR application include:

- Single photon sensitivity
- 16 depth points acquired simultaneously per acquisition
- Highly uniform pixels biased with a single supply

READOUT ARCHITECTURES

After the photon return has been detected, dToF LiDAR system signal chains can use either Analog−to−Digital Converters (ADCs) or Time−to−Digital Converters (TDCs) to digitize the detected laser echo(es). ADC−based systems allow for full pulse digitization, which provides additional information on the target such as its reflectivity, which can be inferred by the pulse shape. However, there are implementation and power advantages to the TDC−based method as the discrimination circuits are relatively simple to implement, and this approach is compatible with narrow pulse width lasers. This means that higher peak power can be used per pulse without affecting eye safety limits.

Find out more about **onsemi**s TDC based reference designs in our detailed white paper.

ADC Full Waveform Processing

One of LeddarTech’s core technologies is to capture the full−received waveform using an ADC instead of capturing echoes with a TDC and histogram technique.

The following figure shows a typical scenario with different target and environment conditions. It can be seen in the raw waveform, captured at high speed, that these targets and conditions return multiple signals with some noise added. The ambient light is one noise contributor for SiPM or also APD sensor arrays. Fog will generate signal at the beginning of the curve. Depending on the reflectivity and range of the target several peaks are visible or not, when they are overlaid by the noise. Using the full−waveform method, it is possible to capture all of these elements at once.

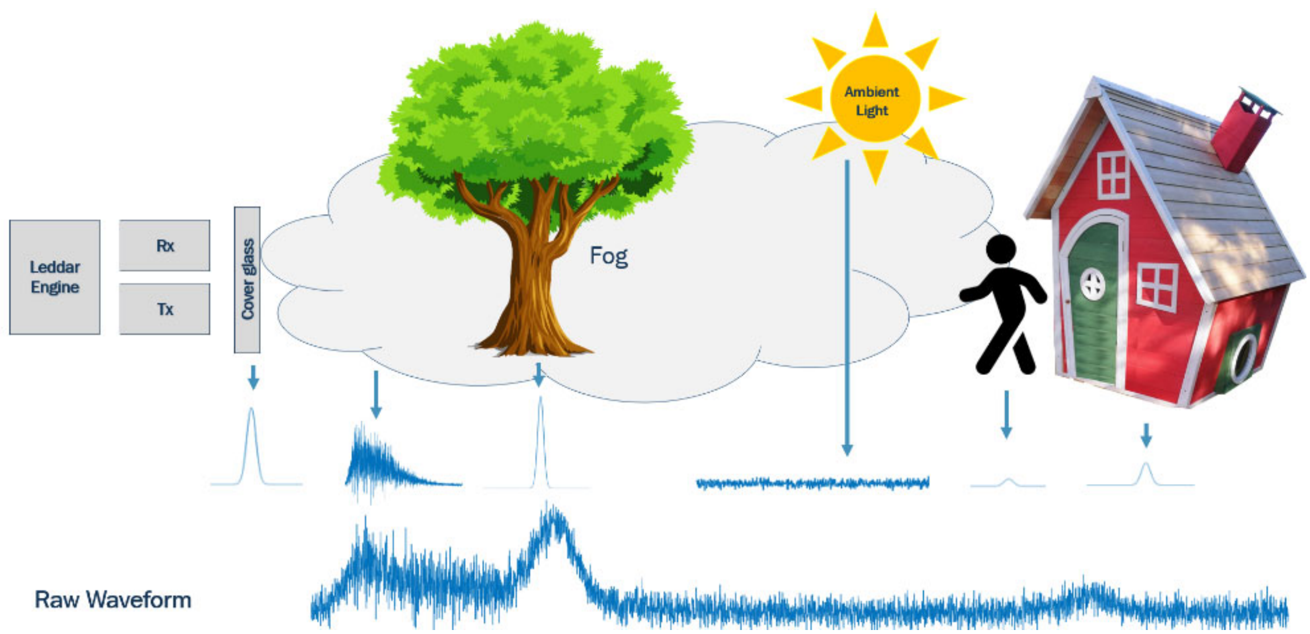


Figure 6. High−Speed Captured Raw Waveform by LCA3 LeddarEngine

Using full−waveform pre−processing, the LCA3 LeddarEngine can filter and/or average out most of the noise components and make the resulting waveform shapes much better and the various events more easily visible.

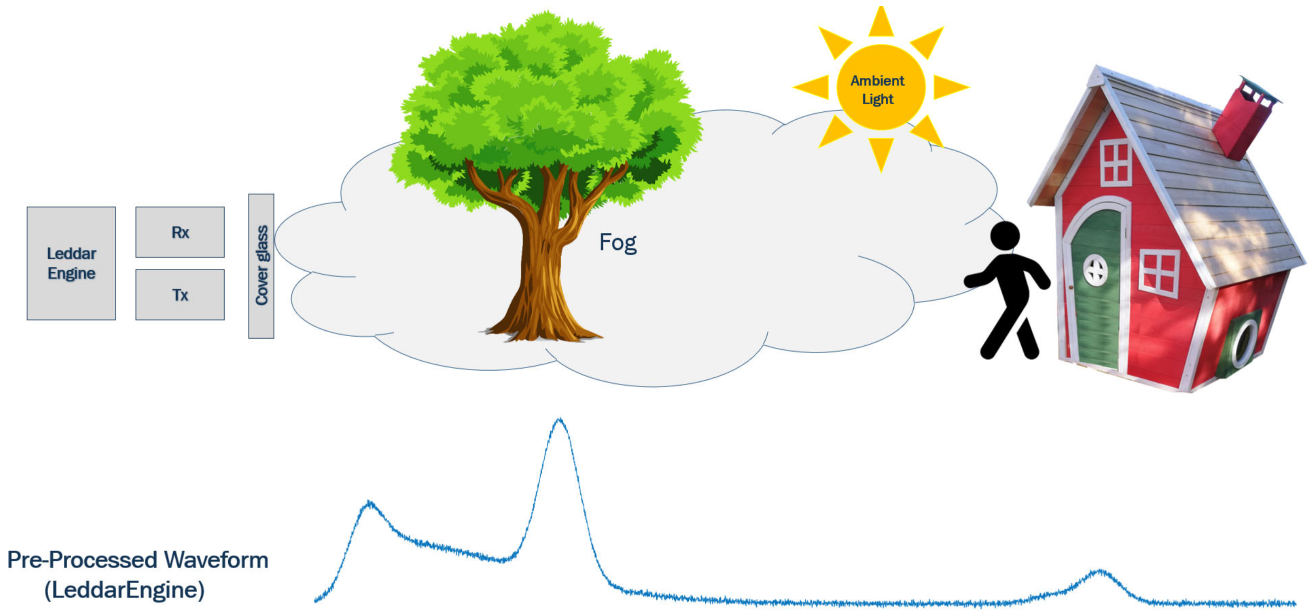


Figure 7. Pre−processed Waveform by LeddarEngine

Based on these preprocessed data, it is now possible by analyzing the full shapes of the signals to discriminate the signal trace from environmental impacts (fog, electrical and optical crosstalk) or to distinguish between two very close targets. Another advantage for the following perception stack is the additional amplitude (reflectivity) information, which can be captured out of one single shot.

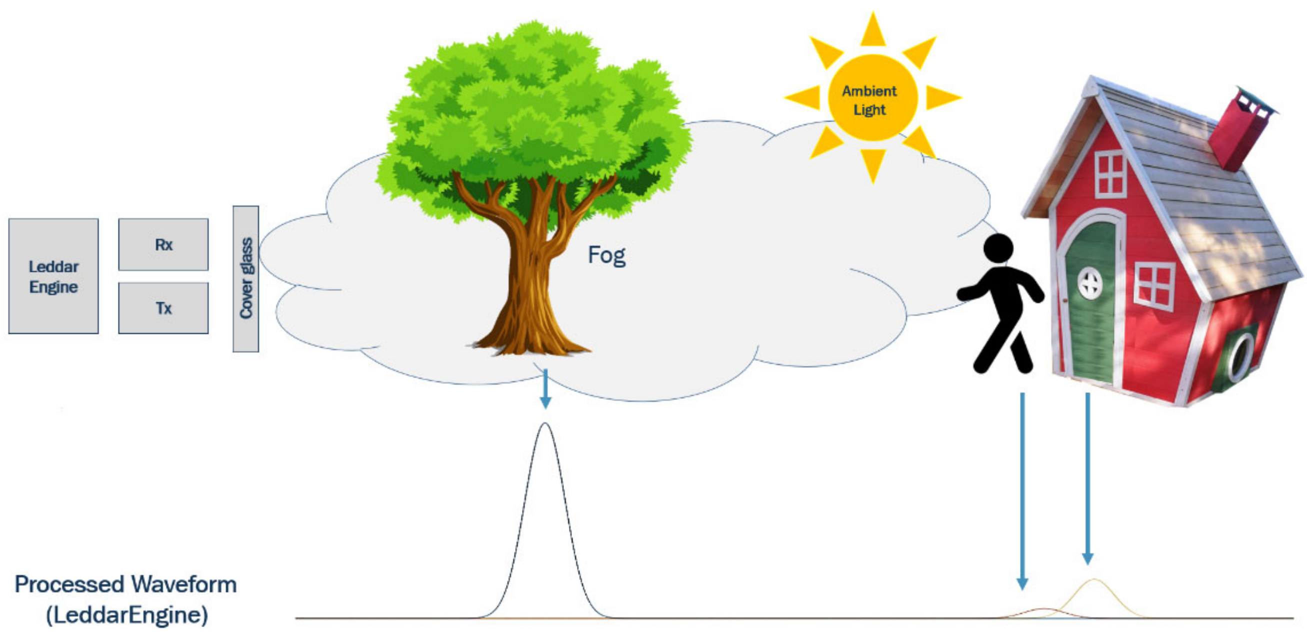


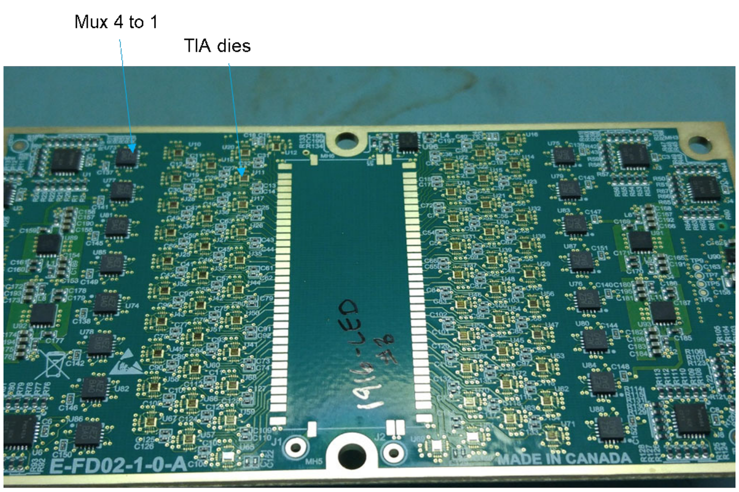
Figure 8. Processed Waveform by LeddarEngine

Summarizing the benefits using full waveform ADC−architecture:

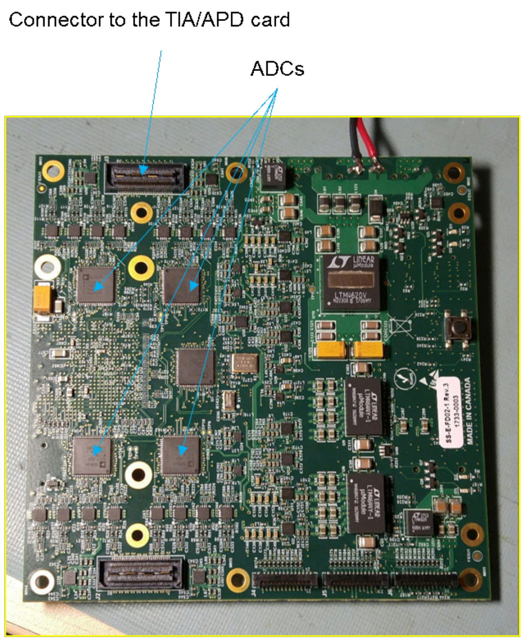
- Multi target detection per pixel with a single shot
  - Allows wider pulse width lasers to be used, cost reduction
  - Significant reduced laser firing rate
  - Improves frame rate and perception
  - Improves SNR = better range with post−processing
- Improved Crosstalk compensation (optical and electrical)
  - Reduction of false detections on neighbor channels in presence of a high−reflective target
  - Possible to detect a weak target superimposed by crosstalk incl. range error compensation
- Improved perception using amplitude information over large dynamic range
  - with high frame rate (only single shot necessary)
  - with reduced overall power consumption (only single shot necessary)
- ADC−based architectures offers flexibility to support for different photodetector technologies
  - PIN, APD and SiPM
  - Flexible reconfiguration of proper detection thresholding in the digital instead of analog domain

Integrated vs Discrete

One significant path to reduce LiDAR system costs is to strive towards higher integration especially on the electronic side. A discrete analog solution (Multiplexer, TIA) for a 32−channel receiver system with discrete realization takes around 60 mm × 120 mm PCB size and consists of more than 48 components (see left−hand side of Figure 9 below). The following analog digital conversion with 4−channel discrete ADC takes also in the range of 120 mm × 120 mm PCA area (right−hand side of Figure 9 below).



Dicrete TIA (64 wire bond die) card top (60mm x 120mm)



Discrete ADC/FPGA card top (120mm x 120mm)

Figure 9. Resulting PCB Size for 32 Channel Receive Chain Using Discrete Components

Using LeddarTech's highly integrated LCA3 ASIC the necessary PCB size can be reduced to 12 mm × 12 mm (Figure 10) which results in significantly reduced PCB area and therefore significantly reduces the cost and form factor.

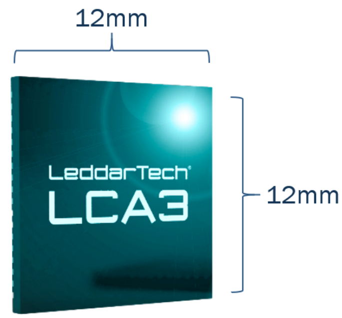


Figure 10. Resulting PCB Size for 64−Channel Receive Chain Using Integrated LCA3 ASIC

Such an integrated data capture solution has multiple major advantages:

- Significantly reduced board space
- Significantly reduced costs
  - Cost per channel integrated: ~1.2 $
  - Cost per channel discrete: ~4 $
  - →~70% cost saving per channel
- Significantly reduced layout complexity
- Use of standard assembly line

In summary, LeddarTech's highly integrated LCA3 LeddarEngine is a key enabler for a low−cost, small form factor LiDAR.

LCA3 LeddarEngine Overview

At the core of the LiDAR platform, the LCA3 LeddarEngine is designed for ISO 26262:2018 ASIL B and sets a new standard to integrate and customize solid−state LiDAR solutions optimized for high−volume production.

Comprised of the LCA3 LeddarCore™ system−on−chip (SoC) and LeddarSP™ signal processing running on a FPGA and/or Microcontroller (MCU), LCA3 LeddarEngine supports multiple LiDAR architectures and technologies, including solid−state flash and hybrid flash.

The LCA3 LeddarCore integrates in a small form factor, AEC−Q100 qualified package the main acquisition and control elements of a LiDAR, i.e. Analog Front End (AFE), digitization, a pre−processing stage, and a timing module to send out pulses to control the light emission and to synchronize the devices to its environment.

The LeddarSP Library includes all the necessary functions to drive the LCA3 LeddarCore and the advanced signal processing technology to output the LiDAR's pixel matrix from the electrical signal acquired through the LeddarCore.

For each pixel of a frame, the LeddarEngine provides a list of echoes characterized by their position in the frame, the distance, the timestamp, the quality attributes, and a status flag. Multiple detections per pixel are available.

Multi−LeddarCore architectures are also supported at LeddarCore and LeddarSP Levels.

Functional Safety hardware features ensure a safe operation and fast error detection within the LiDAR system.

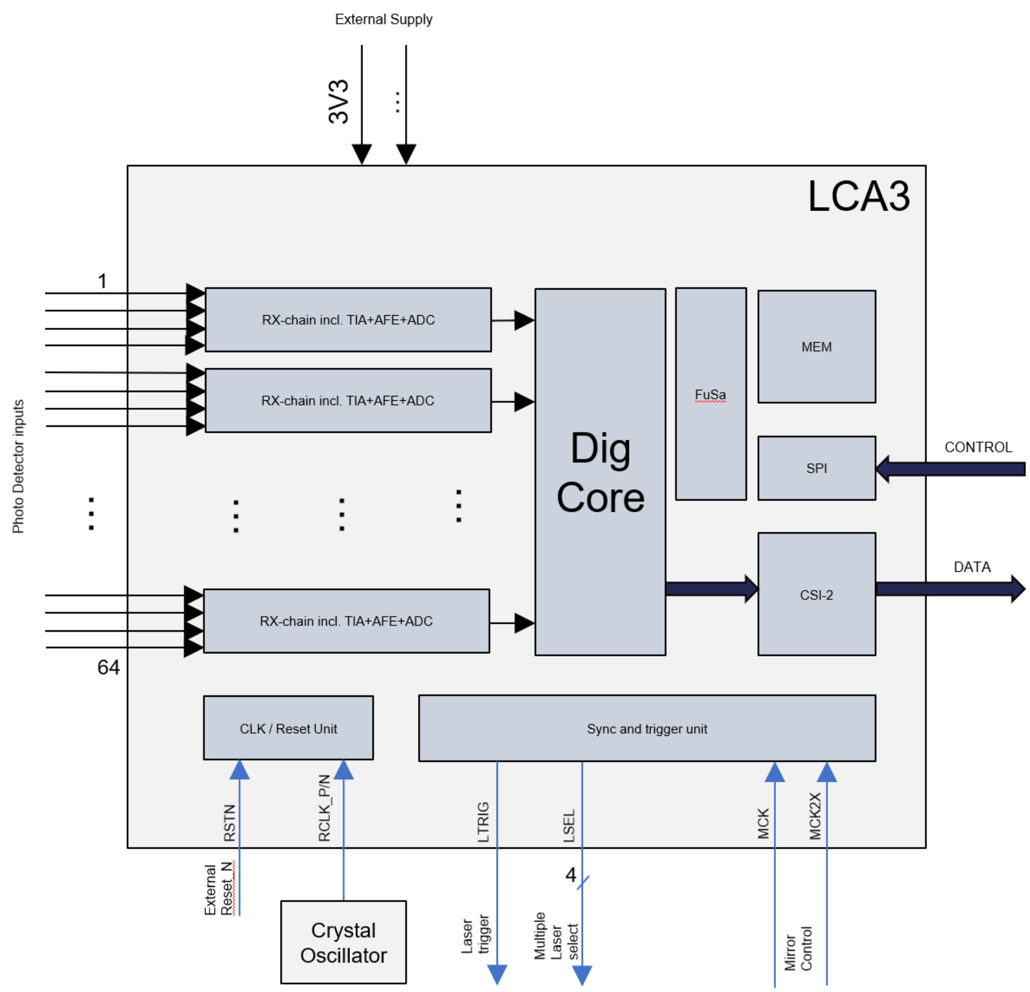


Figure 11. Block Diagram LCA3

The LCA3 LeddarEngine's main features and key benefits are summarized in the following table:

Table 2.

LCA3 Feature	Customer Benefit
– Single−chip solution – 64 physical detector inputs switchable to 16 parallel processing channels – Each channel consists of low−noise front end, high−speed ADC	– Enables processing of high pixel count within a high frame rate – BOM reduction – Minimizes the number of interfaces and component count – Reduced application development effort due to reduced interfaces
Enhanced detector input compatibility – APD and SiPM	Customized detector technology possible
Autonomous execution of freely programmable LIDAR scenarios (Flash, MEMS…)	– Reduced development effort for sequencing and execution – Enables late followers to develop a LiDAR system
Only standardized digital interfaces – High speed CSI−2 data interface (10 Gbps) – SPI control interface (200 Mbps)	– Reduced system development effort – Flexibility of compatibility for signal and perception processing
Possibility to cascade SoC's	Single−platform development for scalable LiDAR system solutions
ISO26262−compliant integrated monitoring functionalities (ASIL−B) with high coverage and HW−interrupt	– Reduced development effort – Less supervision effort on system level
FCCSP package (12 mm x 12 mm)	– Use of standard assembly line – Reduced board space and costs – Reduced layout complexity

LCA3 and SiPM Compatibility Investigations

The **onsemi** SiPMs support two different outputs, the standard and the Fast output. The main difference is that one delivers a current (standard) and the second a voltage (Fast) as output signal. In the following, we will give an overview how the two SiPM outputs can be connected to an LCA3, and as a conclusion which one is the preferred one in terms of performance and overall BOM cost. For all the investigations, we used the ArrayRDM−0116A10−DFN SPICE model in combination with the LCA3 LeddarEngine.

Standard Output

Because the standard output delivers a current, the LCA3 is used as standard transimpedance amplifier (TIA). To ensure electrical compatibility some external components like an AC−decoupling are necessary. A schematic overview is given in the following figure.

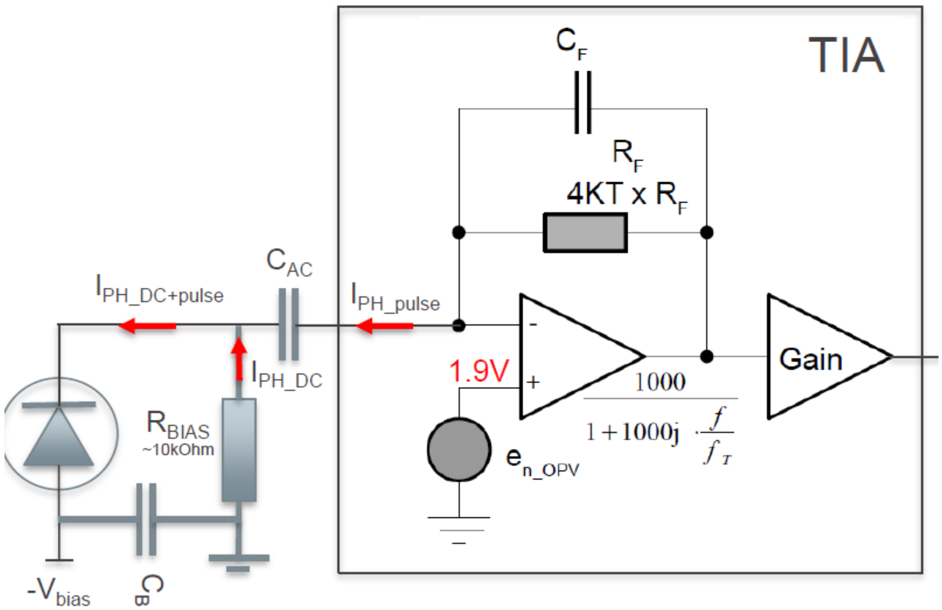


Figure 12. Schematic Overview How to Connect the Standard Output to an LCA3

Simulation setup was done with an ideal TIA to check behavior

- TIA pos limit is 50 V (to check saturation)
- R_F is set to 2 kΩ and 128 kΩ (smallest and largest possible value)
- R_{BIAS} is set to 10 kΩ (>> compared to TIA input impedance of 2 Ω and 128 Ω)
- High pass corner frequency is set to 25 kHz

An overview of the test bench is given in the following figure. On the left we see the model delivered by **onsemi**, followed by the necessary external components, and finally the model of the LCA3 input stage.

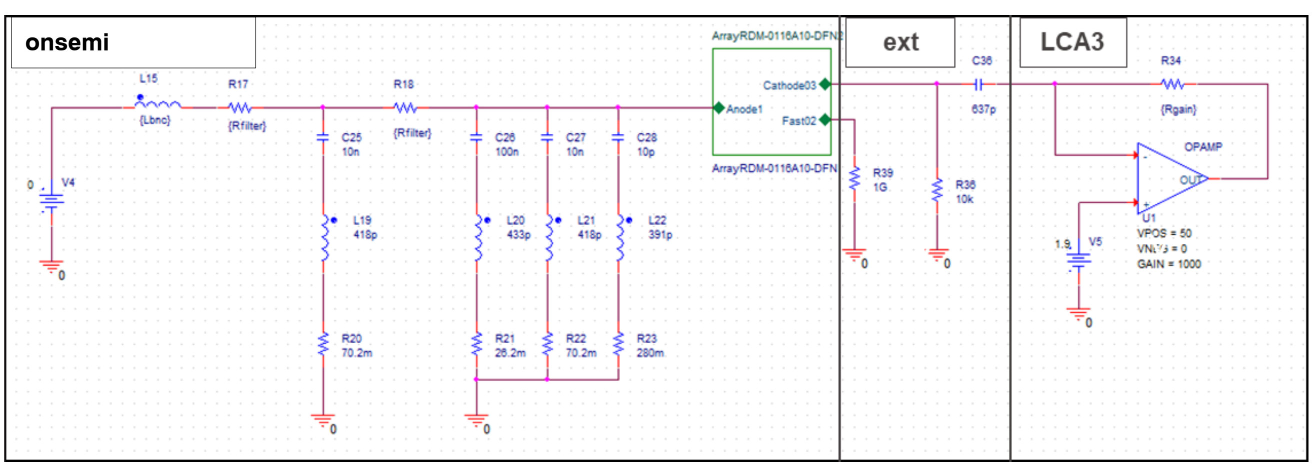


Figure 13. Simulation Test Bench for the Standard Output

The simulation results show that the behavior is as expected including the external AC−coupling and the additional bias resistor R36 which is necessary to close the DC−path caused by ambient light. The TIA gain of the LCA3 was set to the minimum of 2 kV/A. In the following figure, the LCA3 output signal is shown for different number of fired cells of the SiPM. What can be seen is that the TIA will run in saturation at around 50 fired cells, which leads to a limited input dynamic range.

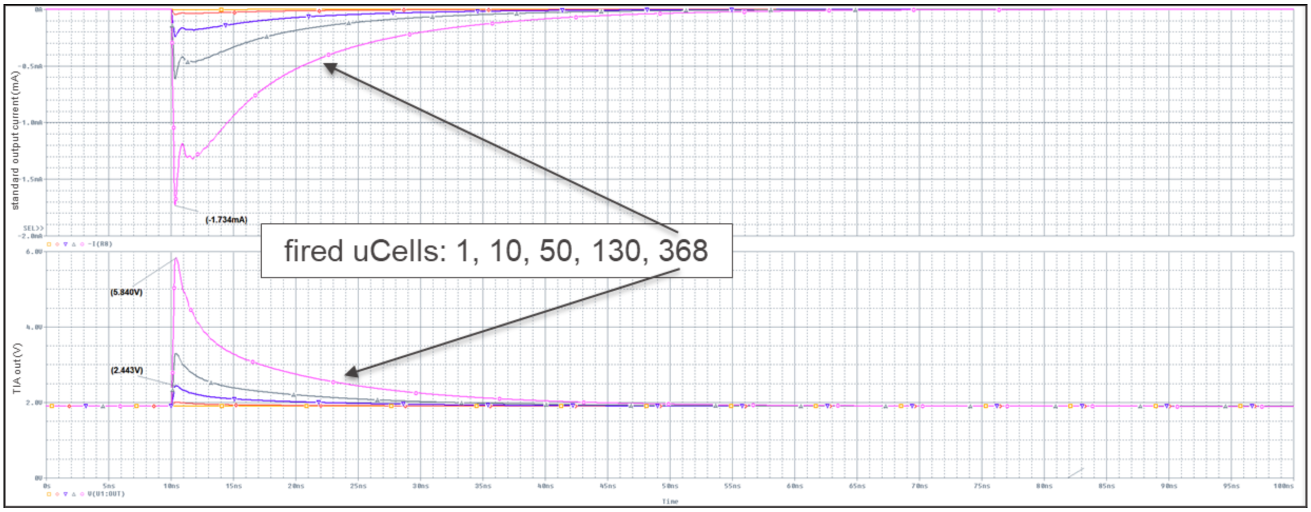


Figure 14. Simulation Results Using the Standard Output, Impact of Different Number of Fired Cells

Fast Output

The SiPM delivers a voltage signal for the Fast output, therefore the LCA3 input stage is used as an inverting amplifier instead of a classical TIA. A first big advantage of doing this is the reduced necessary external components as shown in the following schematic overview.

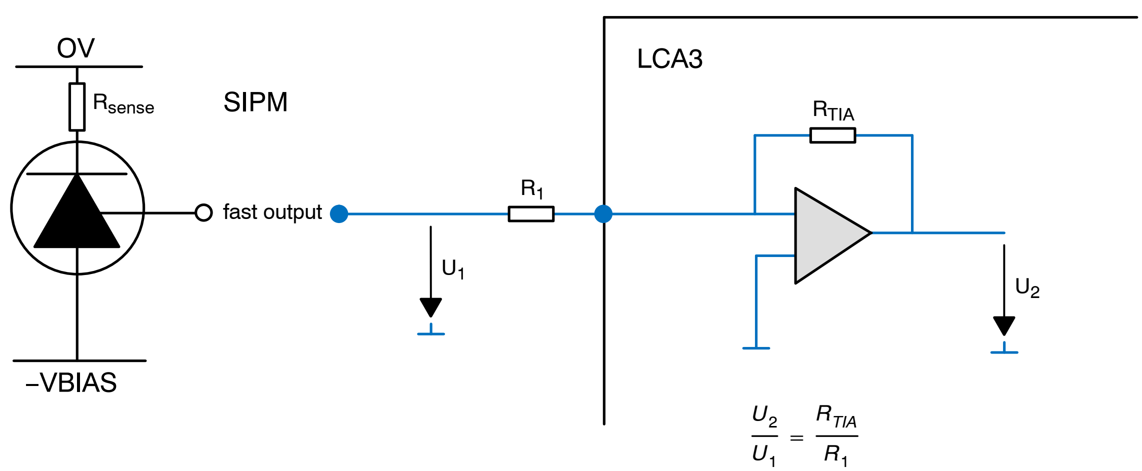


Figure 15. Schematic Overview How to Connect the Fast Output to an LCA3

Another advantage is that, with the right choice of external resistor R1, the pulse width of the Fast output can be adjusted in order to ensure compatibility with the LCA3 ADC sampling frequency.

Simulation setup was done with an ideal TIA of LCA3 to check behavior

- TIA pos limit is 2.4 V (LCA3 design constraint)
- Output voltage as function of Rsense and R1 is investigated
- R_{TIA} (= TIA gain) is set to 2 kΩ (= smallest possible value)

An overview of the test bench is given in the following figure. On the left we see the model delivered by **onsemi**, followed by the necessary external components, and finally the model of the LCA3 input stage.

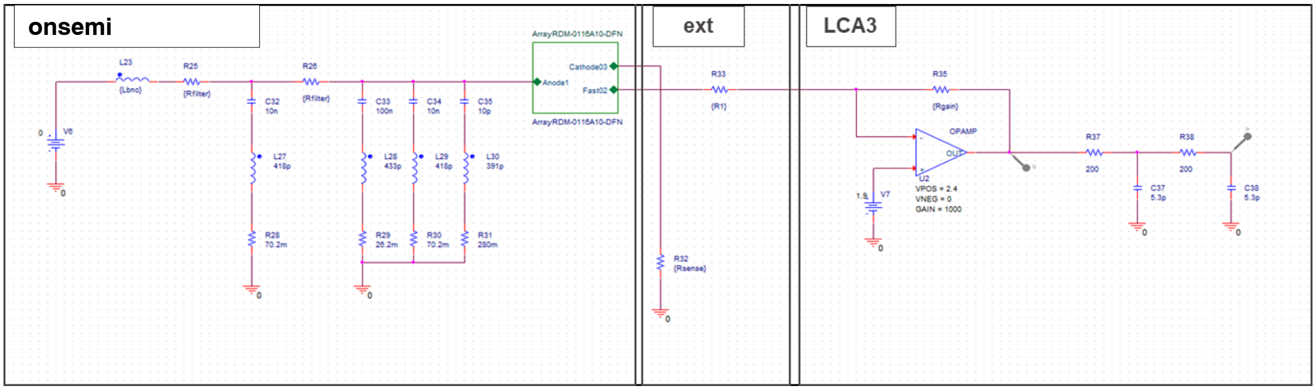


Figure 16. Simulation Test Bench for the Fast Output

For the following simulations, all (368) cells were fired to get the max output amplitude of one pixel and to get the right value, so that the LCA3 input stage does not saturate and that we achieve the best possible input dynamic range.

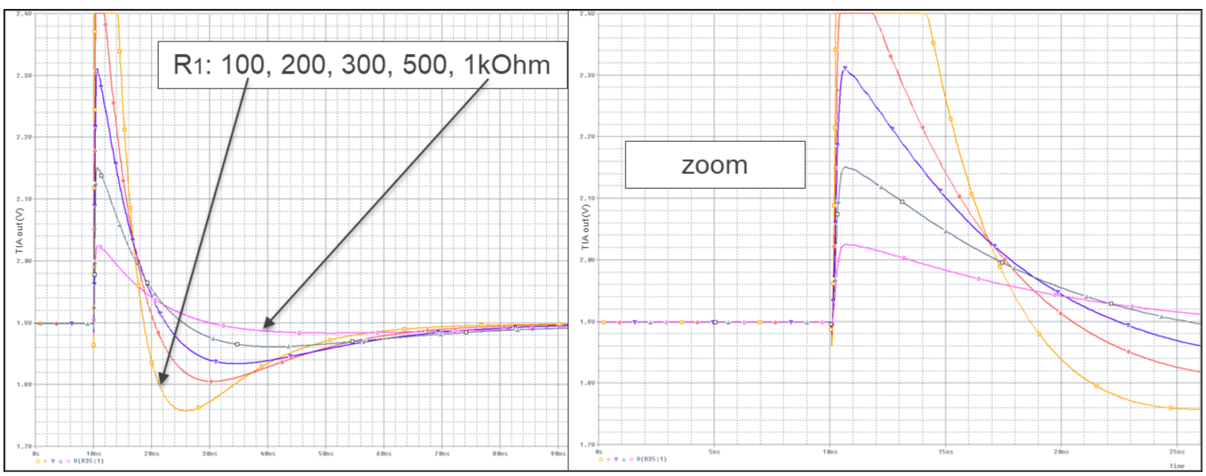


Figure 17. Simulation Results Using the Fast Output, Impact of Different R1 Values

The main outcome of these investigations is that R1 impacts the amplitude, delay and gain of the system but also (as expected) the pulse width can be increased from ~4 ns up to ~10 ns for values ~1 kΩ. R1 shall also be > than 200 Ω, so that the LCA3 input stage is not running in saturation.

The following investigations show the impact of different fired cells for the LCA3 TIA output only and for the complete LCA3 receive chain including the anti–aliasing filter in front of the ADC. The focus of these investigations was to verify if the peak position of the pulse changes for different number of fired cells. If this was the case, it would lead to a distance error for different input amplitudes. But the conclusion of these simulations was that the peak position does not change with the number of fired cells and that we can clearly sample the resulting low pass filtered pulse with the integrated ADC.

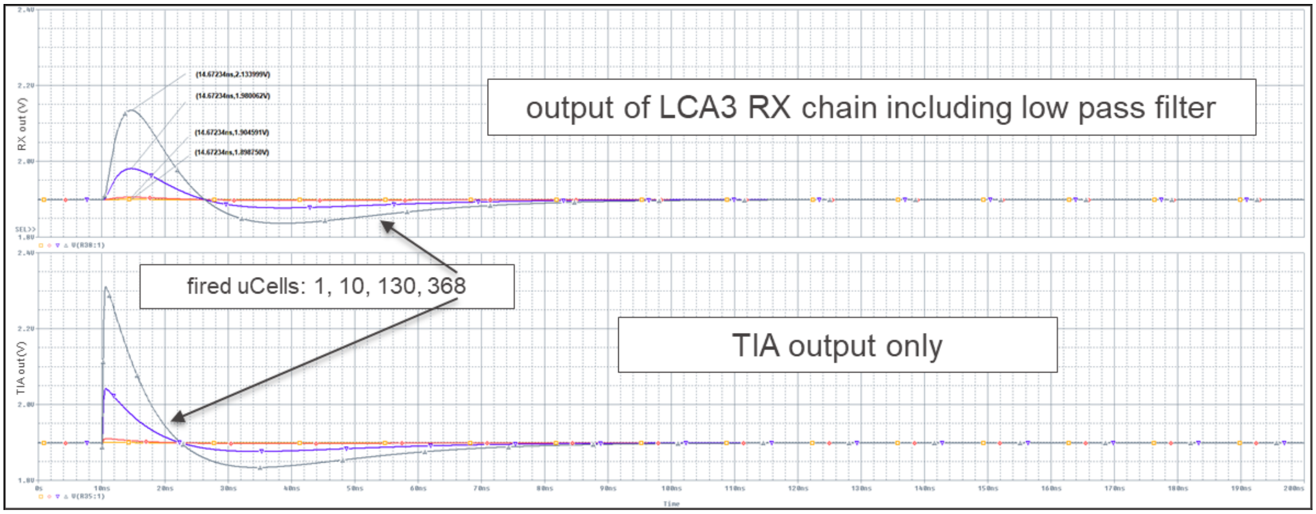


Figure 18. Simulation Results Using the Fast Output, Impact of Different Number of Fired Cells

As a summary of these investigations, we can conclude that:

- Fast output is the preferred choice
  - ♦ Only one external component necessary (BOM cost reduction)
  - ♦ With R1 it is possible to adjust the dynamic range depending on microcells/Pixel
  - ♦ Pulse width is increased and good fit to LCA3 sampling frequency
  - ♦ Peak position does not change with number of fired cells
- Standard output presents limitations
  - ♦ More external components are necessary
  - ♦ Input dynamic range is limited compared to Fast output (Pulse saturation starts above ~50 fired microcells)

Validation Results

A SiPM Array PCB was fabricated with the SiPM array, with mounting holes for a lens mount and mating connectors for the LCA3 evaluation board. A picture of the SiPM Array PCB connected to the LCA3 evaluation board can be seen in the figure below.

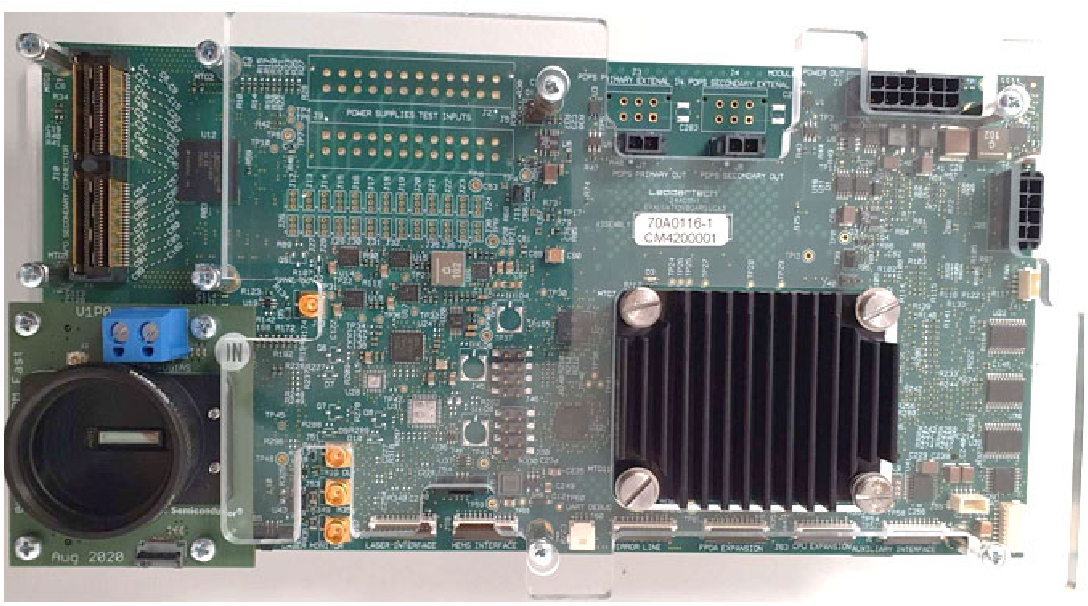
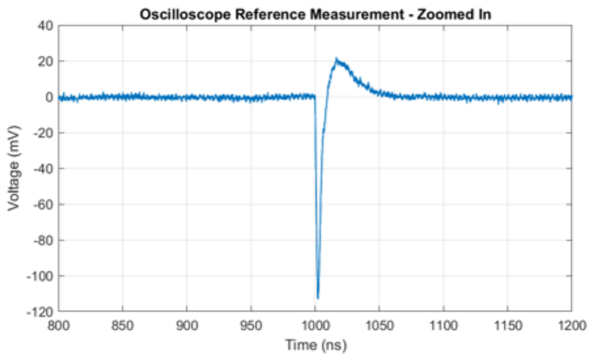


Figure 19. SiPM Array PCB Connected to LCA3 Evaluation Board

The SiPM Array PCB was populated with 1 kΩ resistors in series with the Fast output to ensure the best dynamic range as per the simulations. In the figure below, a comparison is shown of the Fast output pulses observed by connecting the SiPM Array Fast output to the LCA3 and to an oscilloscope via an external amplifier as a reference.



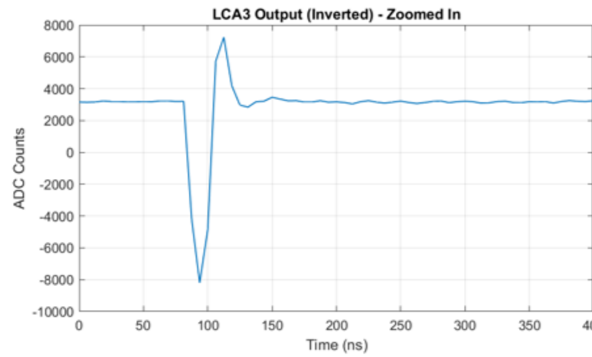


Figure 20. Fast Output Pulses Observed on Reference Oscilloscope and LCA3 Output

The Fast output response for each channel was measured to assess the achievable dynamic range. The single photo electron (PE) level response was measured by covering the SiPM and measuring the dark pulses. The SiPM array was then illuminated with a VCSEL and neutral density (ND) filters were used to reduce the incident light for subsequent measurements. The specifications of the VCSEL used can be seen the table below. The VCSEL trigger signal was provided by the LCA3 evaluation board.

Table 3.

Parameter	Value
Laser Type	VCSEL Array
Wavelength	850 nm
Peak Optical Power	16 W
Peak Optical Power Incident on SiPM Active Area	< 20 mW
Optical Pulse Width	2.3 ns
Beam Divergence	18°
Repetition Rate	230 kHz (driven by LCA3)
Distance from SiPM Array	~275 mm

Two different settings for the LCA3 TIA were tested and the results can be seen in the following table. Note that the SiPM bias voltage was changed between the two measurements, which did lead to a change in the internal gain of the SiPM.

Dynamic ranges of 37 and 67 PE levels were achieved for the 64 k and 2 k gains respectively. The LCA3 can digitize the Fast output signals from the ArrayRDM−0116A10−DFN effectively.

Table 4.

Parameter	Gain setting = 64 k	Gain setting = 2 k (min gain/max dynamic range)	TDC Reference Design	Unit
SPE Pulse Height	250 ADC	170 ADC	33 mV	
SPE Pulse Width	9	8	1.5	ns
Dynamic Range	37	67	13	PE
SiPM Bias Voltage*	−40 (external supply)	−43 (Power PCB)	−43 (Power PCB)	V
SiPM Gain*	1.25E6	1.5E6	1.5E6	

*Note that the results in the table above were taken for a development sample of the ArryRDM−0116A10−DFN. Tests will be repeated with production devices and an updated version of this application note will be released.

JOINT REFERENCE DESIGN

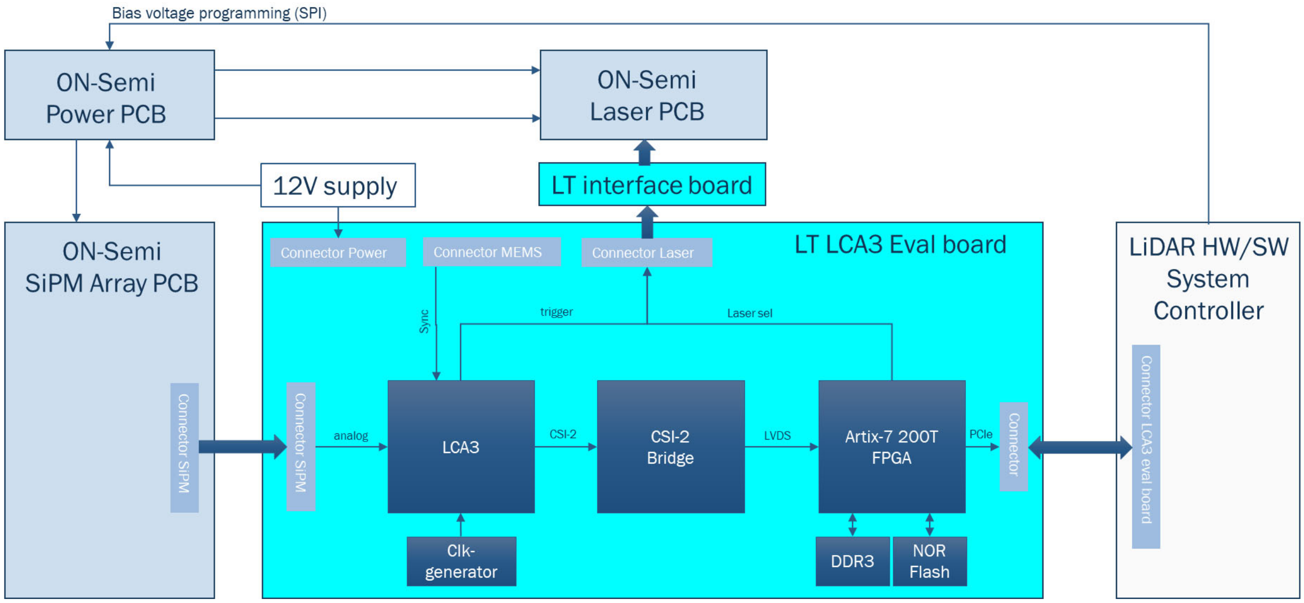


Figure 21. onsemi (ON−Semi) and LeddarTech (LT) Reference Design

onsemi and LeddarTech have collaborated to create a validated ADC−based reference design for LiDAR applications. Note that this design is not a full LiDAR system and does not contain optics or a scanning system.

LCA3 Evaluation Board

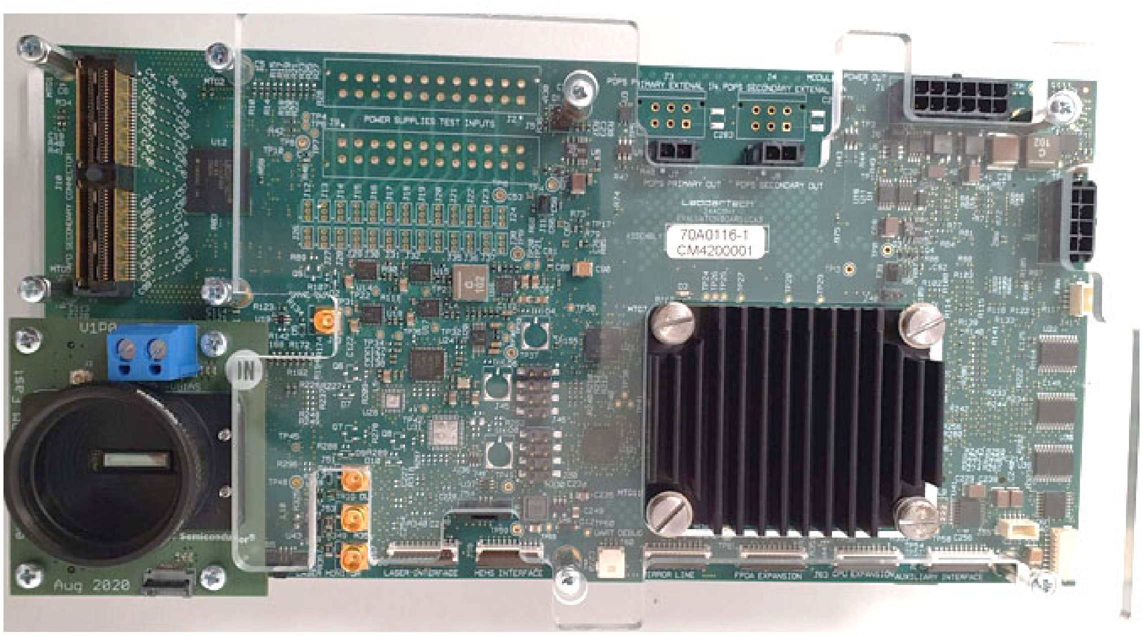


Figure 22. LCA3 Evaluation Board with SiPM Array PCB Connected

The LCA3 evaluation board consists of three main components, the LCA3 a CSI−2 bridge and a FPGA. The connection to the environment (SiPM, Lasers, uC…) is realized using dedicated connectors.

The LCA3 is responsible for:

* Digitize the signal coming from the SiPM and provide the data via a CSI−2 interface to the following stage
* Providing synchronized Laser trigger signal

The CSI−2 bridge, shown in Figure 21, is necessary to convert the CSI−2 protocol to raw−LVDS so that an interface compatibility to the following FPGA can be ensured.

The FPGA consists of the first part of LeddarTech's signal processing. Main processing content are filtering, thresholding, and first peak detection. The output of the FPGA is a pre−processed, enhanced point cloud which can then be used in LeddarTech's second SW−signal processing part to compensate for system imperfections like crosstalk. This SW−processing is placed in a dedicated System Controller but was not necessary and therefore not used for these investigations.

SiPM Array PCB

This board has an ArrayRDM−0116A10−DFN mounted on the PCB, a lens mount footprint, and resistors in series with the Fast outputs. A board−to−board connector allows the PCB to connect to the LCA3 evaluation board. To bias the SiPM array, this PCB can connect to the Boost Power PCB or to an external power supply.

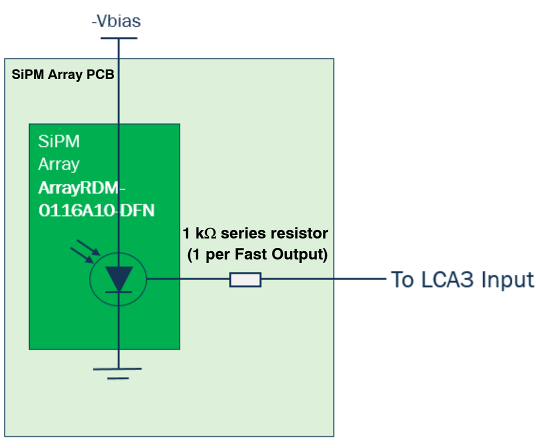


Figure 23. SiPM Array PCB Block Diagram

Boost Power PCB

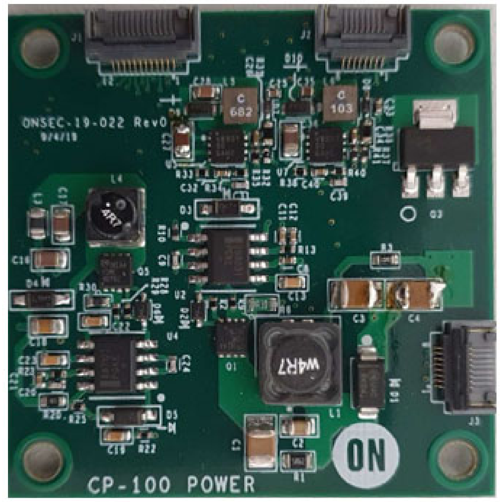


Figure 24. Boost Power PCB

The power PCB covers the SiPM boost converter to step the 12 V input up to 50 V. The SiPM bias supply can be modified over SPI communication from the HW/SW controller or ECU to control its sensitivity. A boost converter is also used to supply the laser PCB.

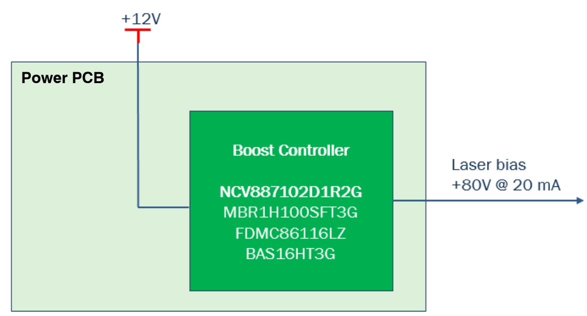


Figure 25. Power PCB Laser Bias Supply Block Diagram

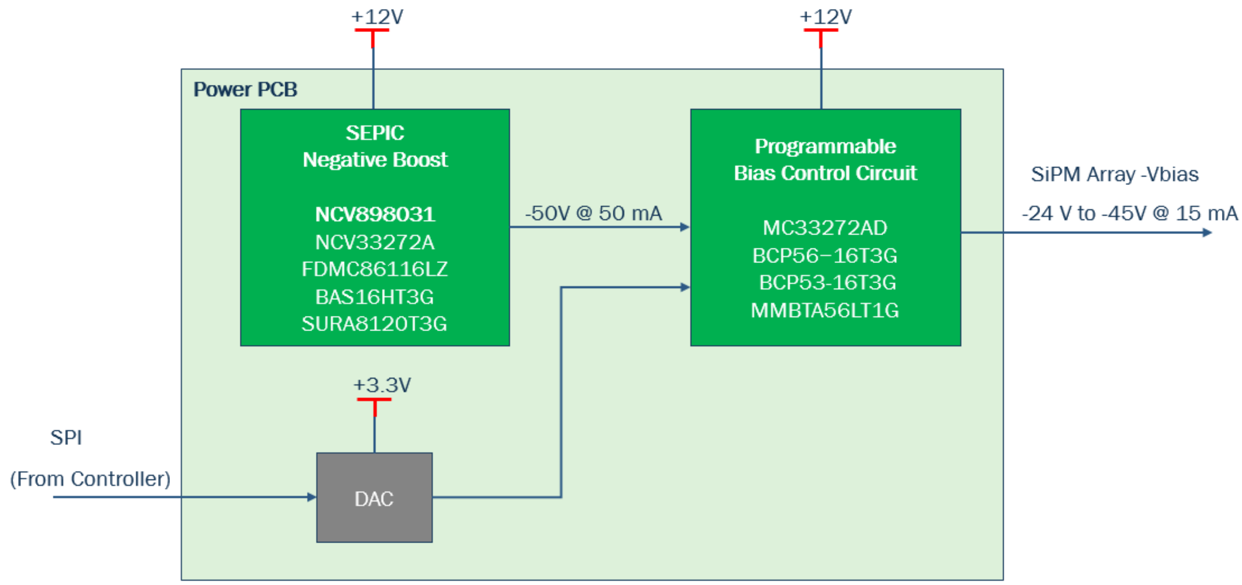


Figure 26. Power PCB Adjustable Negative Bias Supply Block Diagram

Laser PCB

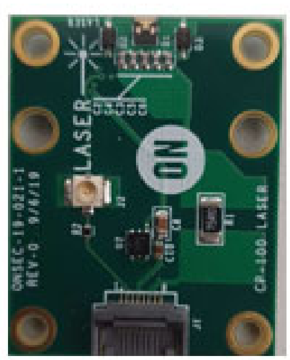


Figure 27. Laser PCB

The optical transmitter is a single laser emitter @ 905 nm wavelength. This edge emitting laser source uses a discrete GaN based laser driver to achieve 75 W peak power lase pulse in a 3 ns pulse width. The LCA3 Evaluation board can provide a repetition rate of 230 kHz.

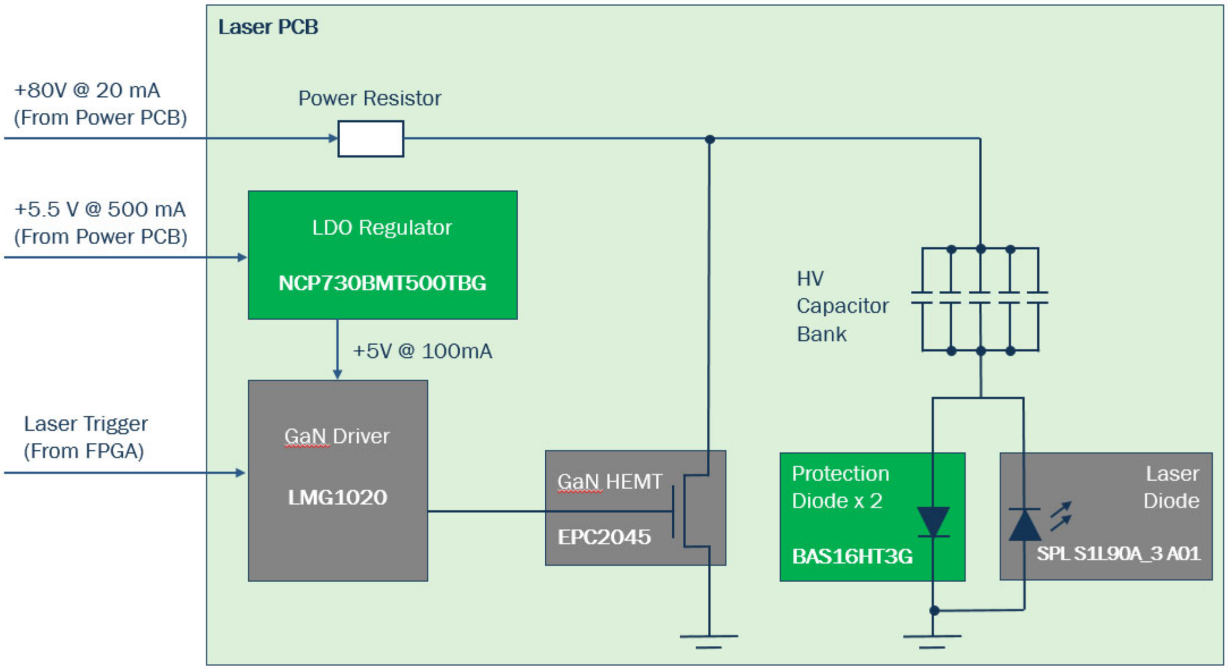


Figure 28. Laser PCB Block Diagram

Interface PCB

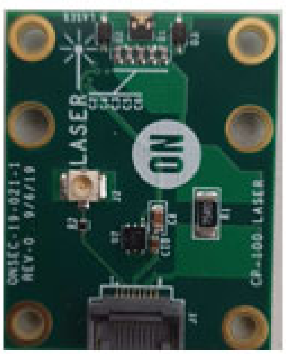


Figure 29. Interface PCB

The interface board ensures electrical compatibility between the LCA3 evaluation board connector and allows the **onsemi** Laser and Boost Power PCBs to be controlled.

SUMMARY

We have outlined in the above paragraphs how the 16 x Fast outputs of ArrayRDM−0116A10−DFN can simultaneously be read by the LCA3 SoC. The Fast output allows for a smaller number of passive components, when compared to APDs or SiPM standard outputs, reducing the BOM costs.

SiPM sensors enable longer ranging thanks to their single photon sensitivity and high internal gain. Low bias requirements < 40 V and uniformity by design reduce the need for calibration and help to reduce system cost. Products such as the ArrayRDM−0116A10−DFN are among the first automotive qualified SiPMs available on the market today. These sensors are qualified to AECQ−102 and can operate from −40°C to +105°C.

LeddarTech's LCA3 is an integrated readout solution that reduces the BOM and offers a significant cost per channel improvement. The LCA3 LeddarEngine is designed for ISO 26262:2018 ASIL B.

onsemi and LeddarTech have collaborated to create a validated ADC−based reference design for LiDAR applications that includes:

- SiPM Array PCB
- LeddarTech's LCA3 Evaluation board
- Boost power PCB for SiPM and Laser PCBs
- Laser PCB
- Interface PCB – controls all PCBs from LCA3 Evaluation board

For more details on these files, please contact:

- https://www.onsemi.com/support
- sales@leddartech.com

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