Electrical Rules Check Report

Class	Document	Message
		Successful Compile for BLE-SWITCH001-GEVB.PrjPcb

Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\Projects\BLE-SWITCH001-GEVB\design_fil

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (HasFootprint('IC_ON_RSL10_SiP')),(InNet('NetR8_1'))	0
Clearance Constraint (Gap=3.9mil) (HasFootprint('IC_ON_RSL10_SiP')),(InNet('NetR3_2'))	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Clearance Constraint (Gap=5.9mil)	0
Clearance Constraint (Gap=3.9mil) (HasFootprint('IC_ON_RSL10_SiP')),(InNet('NetDIO_1'))	0
Clearance Constraint (Gap=5mil) (IsRegion And HasFootprint('IC_ON_XDFN4_CASE711AJ_NO_SILK')),(IsRegion And	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=3.9mil) (Max=20mil) (Preferred=12mil) (InNet('NetDIO_1'))	0
Width Constraint (Min=6mil) (Max=78.74mil) (Preferred=12mil) (All)	0
Width Constraint (Min=3.9mil) (Max=20mil) (Preferred=12mil) (InNet('NetR3_2'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=393.701mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1.9mil)	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (Not InNet('P3V3'))	0
Component Clearance Constraint (Horizontal Gap = 8mil, Vertical Gap = 8mil) (Disabled)(All),(All)	0
Height Constraint (Min=0mil) (Max=1200mil) (Prefered=500mil) (All)	0
Silk primitive without silk layer	0
Total	0