CS5124DEMO/D

Demonstration Note for CS5124 48 V to 5.0 V, 1.0 A Flyback Converter

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DEMONSTRATION NOTE

Description

The CS5124 demonstration board is a fixed frequency, isolated, 48 VDC to 5.0 VDC flyback converter. High efficiency over a wide input voltage range is accomplished by powering the CS5124 controller from a winding on the flyback transformer. Short circuit, overload, and input undervoltage protection are all accomplished by integrated CS5124 circuitry. The demonstration board also accomplishes bootstrapping, Soft Start and blanking with a minimal number of discrete components.

Features

- 36 to 75 VDC Input Voltage Range
- 5.0 V, 1.0 A Isolated Output
- 1″ × 1.6″ Footprint
- Up to 82% Efficiency
- Input Undervoltage Shutdown and Sleep Mode
- Remote Enable Input
- Overcurrent Protection
- Thermal Shutdown

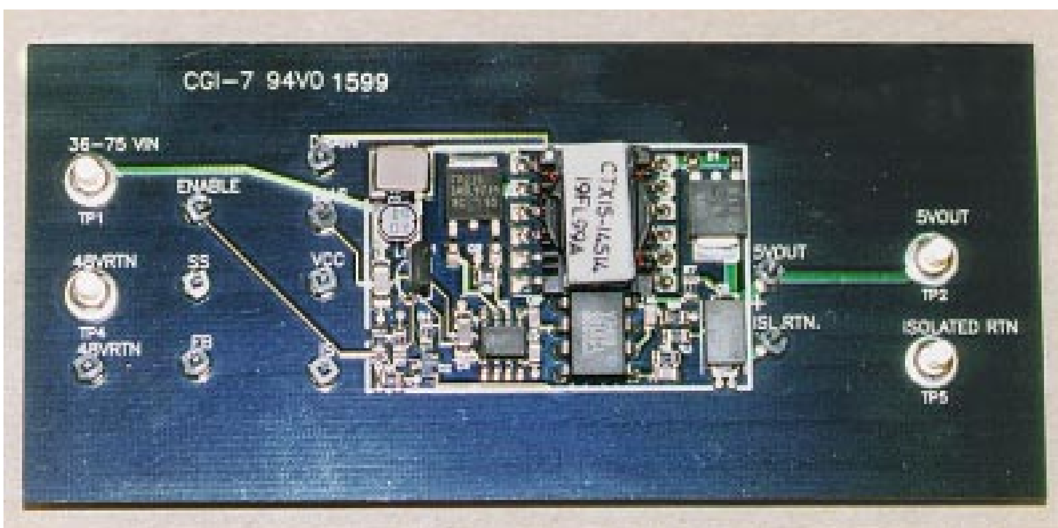

Figure 1. CS5124 Demonstration Board

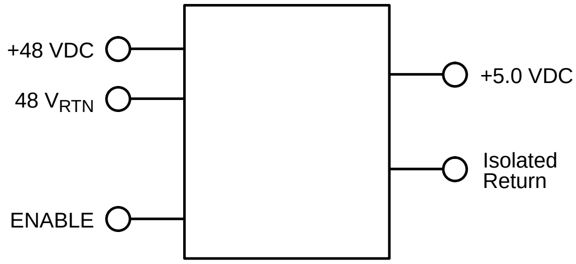

Figure 2. Applications Diagram

ABSOLUTE MAXIMUM RATINGS*

Input/Output Name	Minimum	Maximum	Unit
+48 VDC	-0.3	80	V
Output Current	-	Internally Limited	A
ENABLE	-0.3	6.0	V
Isolated Return	-500	+500	VDC

*T_A = 25°C

ELECTRICAL CHARACTERISTICS (TA = 25°C, 36 V to 75 V, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Voltage	0.15 A < I_{OUT} < 1.0 A	4.85	5.00	5.15	V
Load Regulation	0.15 A < I_{OUT} < 1.0 A, 36 V < V_{IN} < 75 V	-	0.25	-	%
Line Regulation	0.15 A < I_{OUT} < 1.0 A, 36 V < V_{IN} < 75 V	-	0.15	-	%
Transient Regulation and Recovery Time to within 1%	Step between 50% and 75% of maximum load.	- -	100 200	- -	mV µs
Output Ripple and Noise	75 V_{IN} @ Full Load (20 MHz BW)	- -	200 20	- -	mV_{p-p} mV_{rms}
Efficiency	0.2 A Out 1.0 A Out	- -	72 82	- -	% %
ENABLE (Turn-On) Threshold	-	2.30	2.63	2.76	V
ENABLE Hysteresis	-	170	185	200	mV
Sleep Mode (Turn-Off) Threshold	-	1.50	1.83	2.30	V
Sleep Mode Hysteresis	-	35	85	150	mV
ENABLE Pin Source Current	ENABLE Pin = 0 V	-	-	1.0	mA
Sleep Mode Input Current	75 V_{IN}	-	650	1000	µA
ENABLE/SS Time	Full Load	-	5.0	-	ms
Undervoltage Lockout (Turn-Off)	-	28	31	33	V
Undervoltage Lockout (Turn-On)	-	31	33	35	V
Undervoltage Lockout Hysteresis	-	-	2.0	-	V
Overcurrent Limit Threshold	V_{IN} = 36 V V_{IN} = 75 V	- -	1.2 1.7	- -	A A
Oscillator Frequency	-	380	400	420	kHz

PIN DESCRIPTION

Pin Symbol	Function
+48 VDC	36 to 75 VDC input.
48 V_{RTN}	Return for +48 VDC input.
ENABLE	This pin is internally pulled up and performs the UVLO function if left open. Pull this pin to between 2.25 V and 2.5 V to stop the converter from switching. Pull this pin to blow 1.5 V to put the converter in sleep mode.
+5.0 VDC	+5.0 VDC isolated output.
Isolated Return	Return for +5.0 VDC output and load.

OPERATING INSTRUCTIONS

Input Power

The converter is designed to run with an input voltage between 36 VDC to 75 VDC. Approximately 180 mA of current will be required for full load with a 36 V input.

Output Load

An external load is required for the demo board to run normally at fixed frequency. If the demo board is run with a load less than about 80 mA it will regulate the output at 5.0 V in hiccup mode.

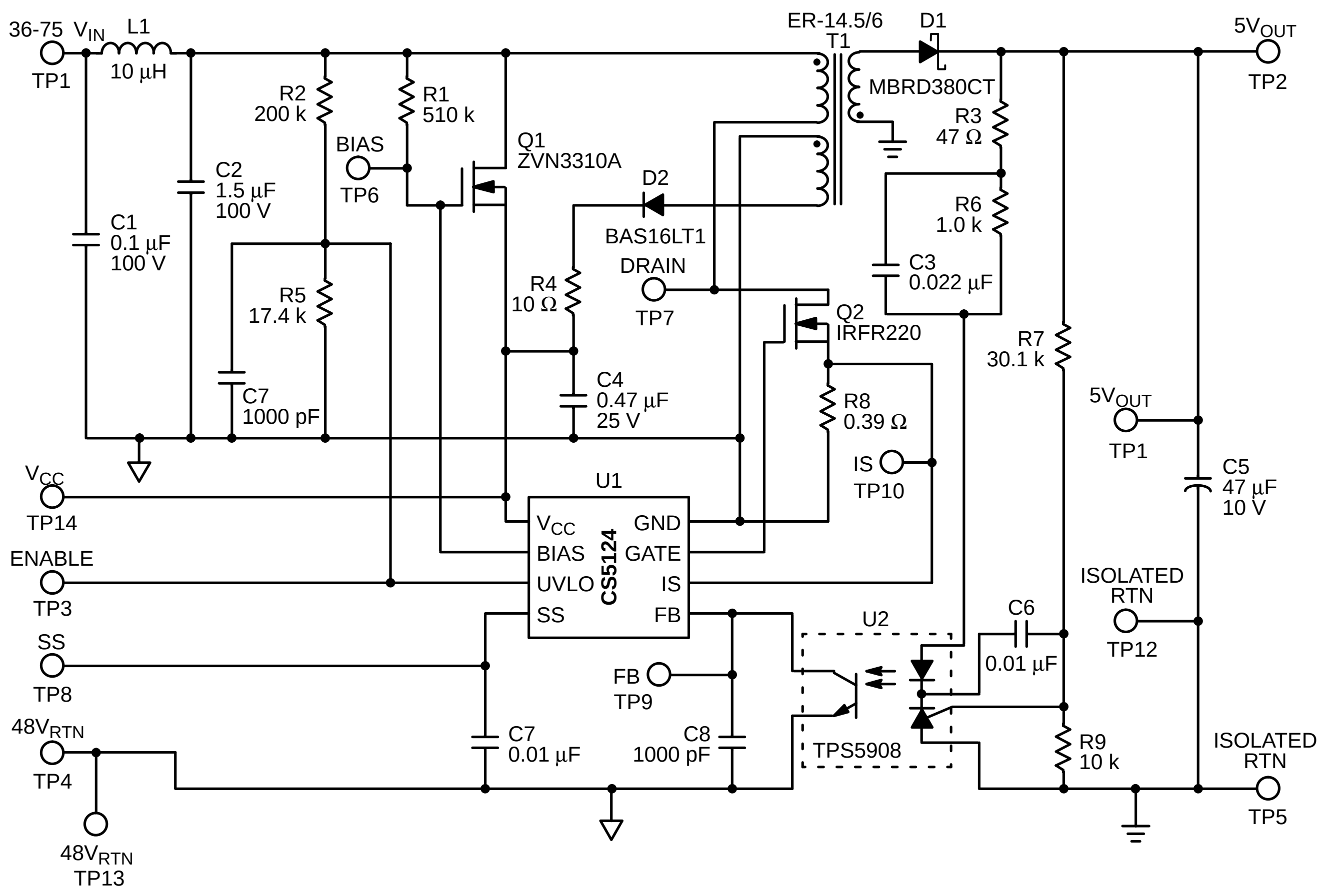

Figure 3. Circuit Schematic

THEORY OF OPERATION

ENABLE/UVLO

R2 and R5 form a divider for the UVLO function. If the ENABLE pin of the supply is left open it will operate in three modes depending on the input voltage. For V_{IN} less than 18 V the supply will be in sleep mode. For V_{IN} between approximately 18 V and 31 V the BIAS section is operational and V_{CC} is regulated to 8.0 V, but the PWM section is disabled. If V_{IN} exceeds 35 V the supply operates normally.

C9 is included on the demonstration circuit to prevent radiated noise from coupling to the ENABLE pin through the ENABLE test point. This part may not be needed with a more typical pcb layout.

The ENABLE pin can also be controlled by open collector logic to perform an ENABLE function. When the ENABLE pin is below 1.5 V the supply will be in sleep mode and input current will be less than 1.0 mA.

V_{CC} Bias

R1 provides a pull-up to turn Q1 on and the BIAS pin sinks current to regulate V_{CC} or turn off Q1. When the IC is operational, but not powered by the flyback winding, V_{CC} will be regulated to 8.0 V by the BIAS pin and Q1. During normal operation, when sufficient energy to power the controller is available from the flyback winding, V_{CC} rises above 8.0 V and the BIAS pin turns Q1 off.

The BIAS pin and associated components form a high impedance node. Care should be taken during pcb layout to avoid connections that could couple noise into this node.

Current Sensing

R8 is the current sense resistor. The turn-on spikes, shown in Figures 16-18, are blanked internally by the CS5124.

During heavy load conditions the primary current is pulse by pulse limited as shown in Figure 19. Under conditions where the current sense pin measures high currents with fast rise-times the CS5124 second threshold will be exceeded the converter will enter a low duty cycle hiccup mode as shown in Figures 20 and 21. The CS5124 Demonstration Board typically reaches this condition only when the input voltage is greater than 65 V and there is a low impedance short across the output pins.

Soft Start & Hiccup Mode

Soft Start capacitor C7 determines the Soft Start time during turn-on, and the dead time when the supply is operating in hiccup mode. During Soft Start there will be a dead time of about 1.5 ms while C7 charges to 1.6 V. The ramp-up time of the output voltage will last about 1-2 ms depending on output load.

During hiccup mode the dead time will be about 1.4 ms while C8 charges from 0.25 V to 1.6 V as shown in Figure 21.

Feedback

R7 and R9 divide the 5.0 V output to the 1.24 V reference of U2. C6 and the Thevenin resistance of R7 and R9 set the low frequency roll-off of U2. R6 sets the maximum current through U2’s photodiode and adjusts gain. C3 provides phase boost near the crossover frequency. C8 is primarily for high frequency noise reduction.

DESIGN INFORMATION

Flyback Transformer

The transformer was designed to operate in continuous and discontinuous conduction modes. Running in discontinuous conduction mode at light loads allows for a smaller core size, and by requiring a higher peak current offers a larger current sense signal. Operating in continuous conduction mode during at heavy loads reduces ripple current in the output filter capacitor.

The transformer also runs at less than 50% duty cycle under all conditions. This eliminates the need to choose the transformer inductance to meet slope compensation criteria and in a continuous flyback converter lower duty cycle means lower output filter capacitor ripple.

The V_{CC} flyback winding powers the controller and is clamped to a voltage proportional to the secondary voltage. If the initial turn-off spike is snubbed this winding will provide a regulated V_{CC} voltage. To provide V_{CC} power from the flyback winding rather than the bias circuit during normal operation, the number of turns should be chosen to to provide more than 9.0 V under operating conditions.

Flyback Transformer Design Procedure

1. Choose duty cycle less than 50% at low line. For a 400 kHz nominal operating frequency choose T_{ON} = 1.1 μs and T_{OFF} = 1.4 μs with 36 V_{IN}.
2. Choose primary to secondary ratio.

$$\frac{N_P}{N_S} = \frac{T_{ON}}{T_{OFF}} \times \frac{V_{IN}}{V_{OUT}} = \frac{1.1\ \mu s}{1.4\ \mu s} \times \frac{36\ V}{5.4\ V} = \frac{5.2}{1}$$

3. Choose auxiliary to secondary ratio.

$$\frac{N_A}{N_S} = \frac{V_{CC} + 0.7\ V + I_{CC} \times R_{SNUB} \times 2}{V_{OUT} + 0.4\ V} = \frac{11.7 + 10\ mA \times 10\ \Omega \times 2}{5.4\ V} = \frac{2.2}{1}$$

4. Calculate the minimum primary inductance so that the on time at minimum load and maximum V_{IN} is longer than CS5124 blanking plus propagation delay time. (see document number CS5124/D available through the Literature Distribution Center or via our website at http://www.onsemi.com).Minimum load is chosen to be 60 mA.

$$L \geq \frac{V^2 \times D^2}{P_{MIN} \times Freq \times 2}$$
$$= \frac{75^2 \times 0.124^2}{0.52\ W \times 400\ kHz \times 2} = 208\ \mu H$$

where

$$T = (T_{BLANK} + T_{PROP}) \times Freq$$
$$= (130\ ns + 180\ ns) \times 400\ kHz = 0.124$$

and

$$P_{MIN} = \frac{(V_{OUT} \times I_{OUT}) + P_{CS5124}}{Efficiency}$$
$$= \frac{(5.3\ V \times 60\ mA) \times 100\ mW}{0.8} = 52\ W$$

5. Choose core type and design the transformer using standard techniques. The winding sheet for the demo board transformer is shown in Figure 4.

2/1/1999 5124 Flyback Transformer

ITEM	DESCRIPTION	
CORE	Coiltronics ER 14.5, AL-2	AL = 2.16E-07
BOBBIN		MLT = 1.06
TAPE		
CLIP		

LEAD TERM
10, 11, 12
7, 8, 9

TRANSFORMER WINDING DATA

LEAD TERM	TURNS	WIRE SIZE	# of Wires	RNOM	LNOM	NOTES
2						
	30	32	1	0.431	1.9E-04	1, 2
4						
	14	32	1	0.201	4.2E-05	1
1 3	6	31	3	0.023	7.8E-06	1

Notes:
1. Start all windings together. (The number of turns are the total for each winding.)
2. Finish with tape.
3. A minimum of 500 V isolation is required.

Figure 4. Winding Sheet for the Demo Board Transformer

Output Filter

Figure 5 shows the output filter ripple currents at low line and full load. The lower left section shows current supplied to the output by the output filter while the main switch (Q2) is on. The lower right section shows current supplied to the output by the transformer secondary when Q2 is off (during flyback). The upper right shows current supplied by the transformer secondary to recharge the output filter. The total charge in the upper right section must be equal the (dis)charge in the lower left during steady state. The RMS current in the output filter capacitor (C5) is ≅ 1.0 A.

Due to the high di/dt in the output filter of flyback converters, spikes on the output are nearly impossible to eliminate with one filter stage. In this design the output filter sees approximately a 2.0 A step current in 50 ns. With such a high di/dt just 3.0 nH (a typical via is 0.7 nH) of inductance in a single stage output filter will produce a 120 mV spike. See Figure 11. If this spike is unacceptable a second filter stage, as shown in Figure 12, using a ferrite bead (Steward HI0805N410R) and a ceramic capacitor can reduce the spike to the magnitude shown in Figure x. (The feedback connection should also be moved to connect to the 1.0 μF filter capacitor.)

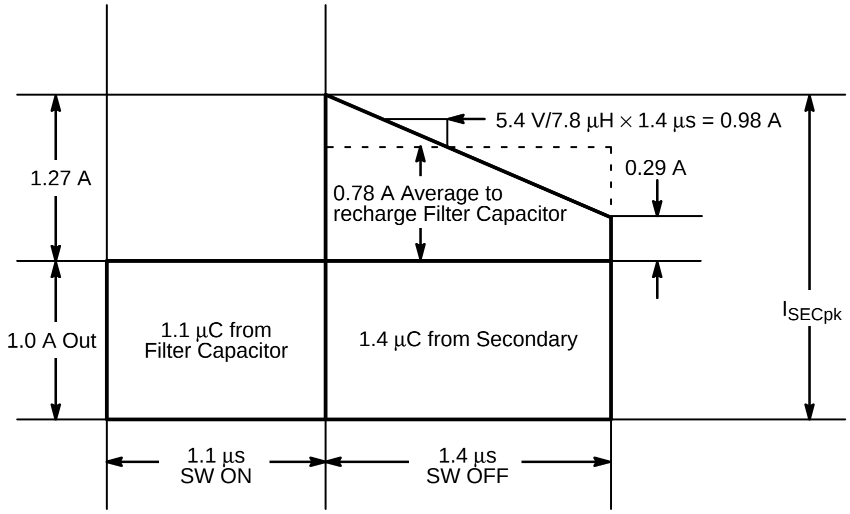

Figure 5. Output Filter Currents

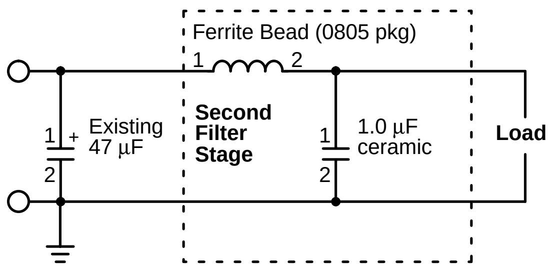

Figure 6. Second Output Filter Stage

Current Sense Resistor Selection

The current sense resistor (R8) value is chosen to keep the peak voltage of the current sense waveform below the CS5124 1st Threshold during normal operation. The peak primary current can be calculated by dividing the secondary peak current (in Figure 5) by the transformer ratio.

$$I_{PRIpk} = I_{SECpk} \times \frac{N_S}{N_P} = 2.27\ A \times \frac{6}{30} = 0.45\ A$$

The First Current Sense Threshold decreases with higher duty cycles and should be calculated at maximum duty cycle.

$$\text{CS5124 1st Threshold} = \frac{2.9\ V - 170\ mV/\mu s \times T_{ON}}{10} - 60\ mV$$

$$= \frac{2.9\ V - 170\ mV/\mu s \times 1.1\ \mu s}{10} - 60\ mV$$

$$= 211\ mV$$

The current sense resistor with a 20% margin is:

$$R_{SENSE} = \frac{\text{1st Threshold}}{I_{PRIpk} \times 1.2} = \frac{211\ mV}{0.45\ V \times 1.2} = 391\ m\Omega$$

TYPICAL PERFORMANCE CHARACTERISTICS

The figures below show typical performance of the CS5124 Demo Board. Unless noted all waveforms were taken with the 20 MHz filter option selected on the oscilloscope.

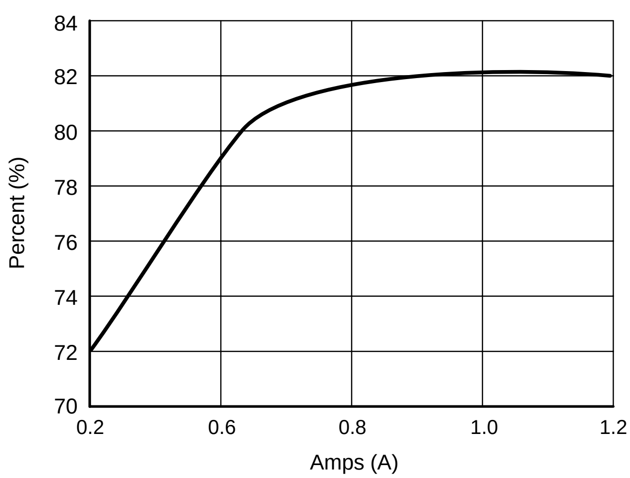

Figure 7. Typical Output Efficiency at 48 V_{IN}

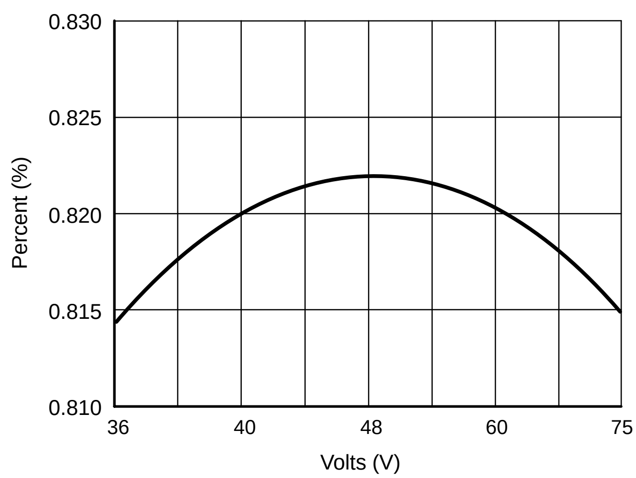

Figure 8. Typical Output Efficiency at 1.0 A Out

TYPICAL PERFORMANCE CHARACTERISTICS

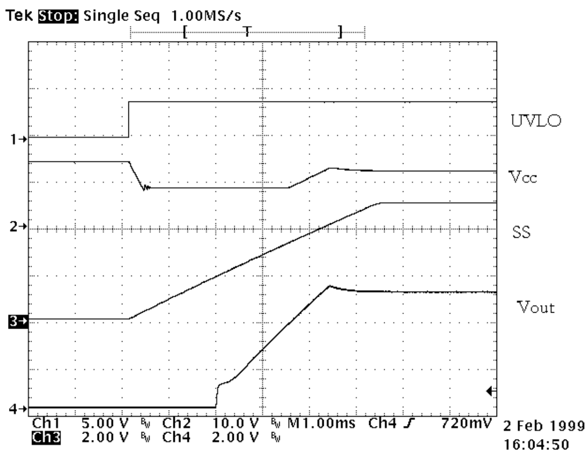

Figure 9. Start-up Waveforms at 48 V_{IN}, 1.0 A Load

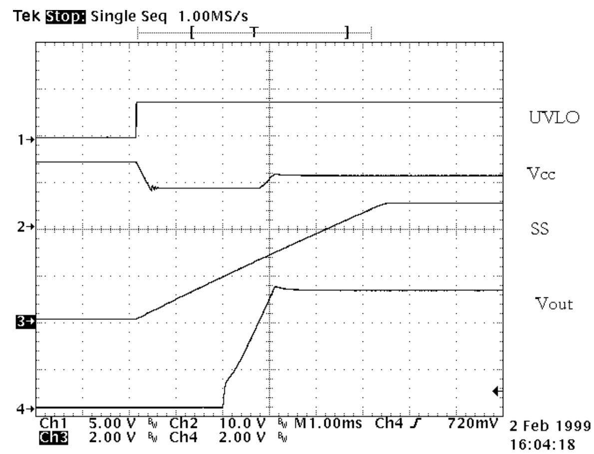

Figure 10. Start-up Waveforms at 48 V_{IN} with 0.17A Load

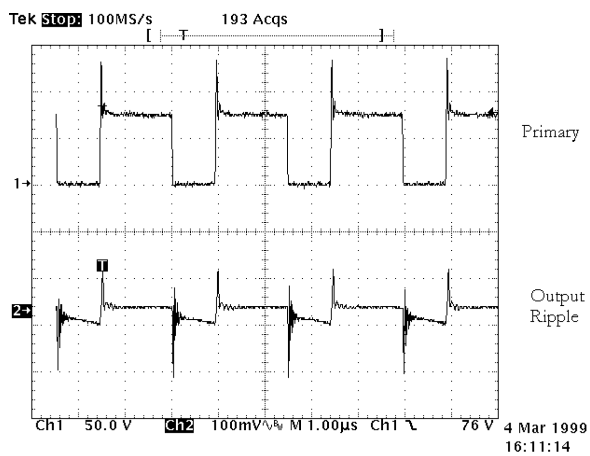

Figure 11. Primary Voltage and Output Ripple at 36 V_{IN}, 1.0 A Out

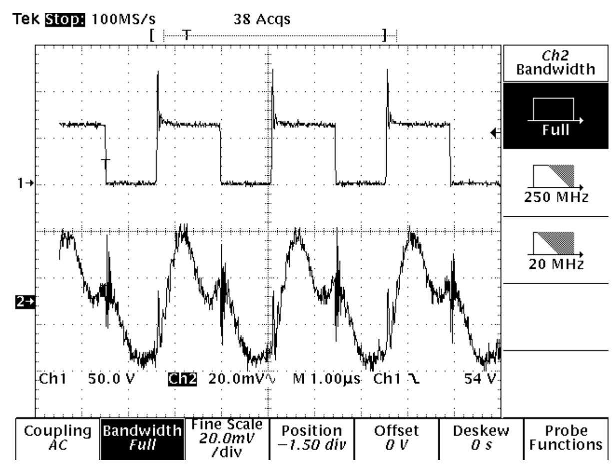

Figure 12. Primary Voltage and Output Ripple with Additional Filter Stage; Ferrite Bead and 1.0 µF Ceramic Capacitor-Full Bandwidth Measurement

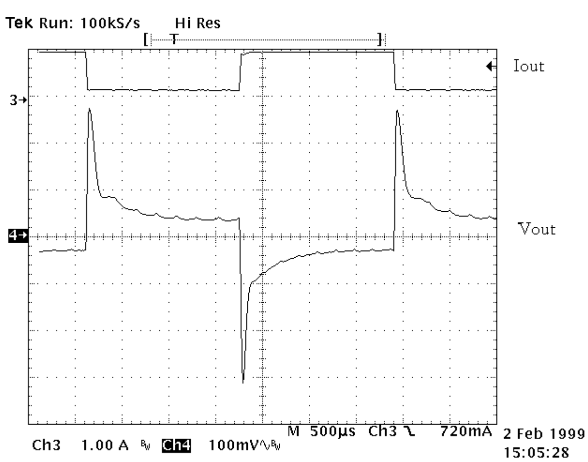

Figure 13. Transient Response 0.17 A to 1.0 A Step

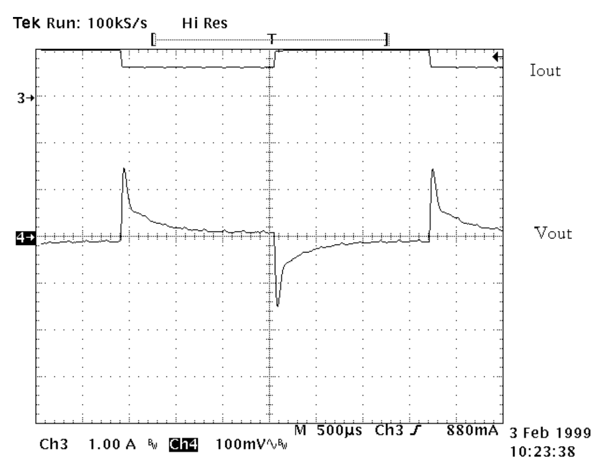

Figure 14. Transient Response 0.6 A to 1.0 A Step

TYPICAL PERFORMANCE CHARACTERISTICS

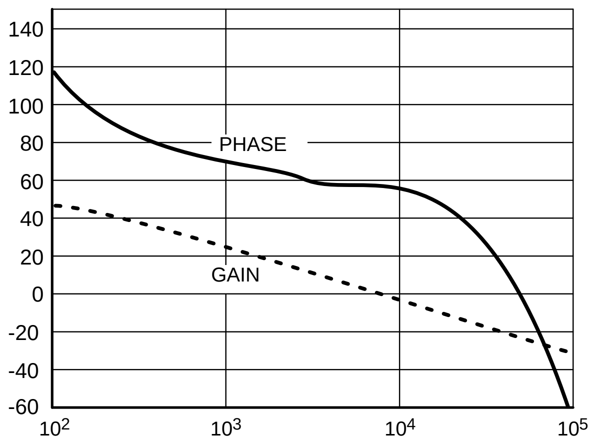

Figure 15. Control Loop at 48 V_{IN}, 0.5 A Out

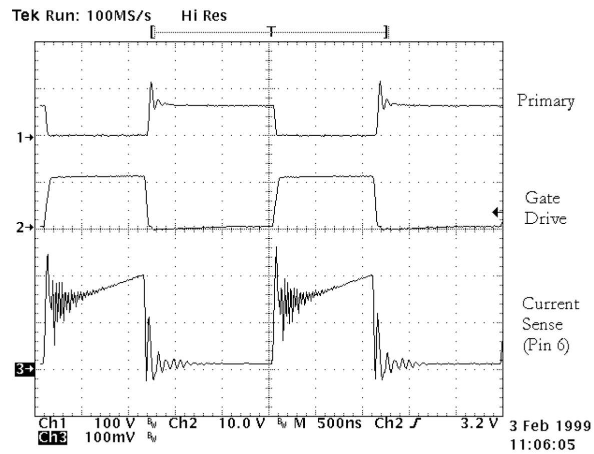

Figure 16. Current Sense 36 V_{IN}, 1.0 A Out

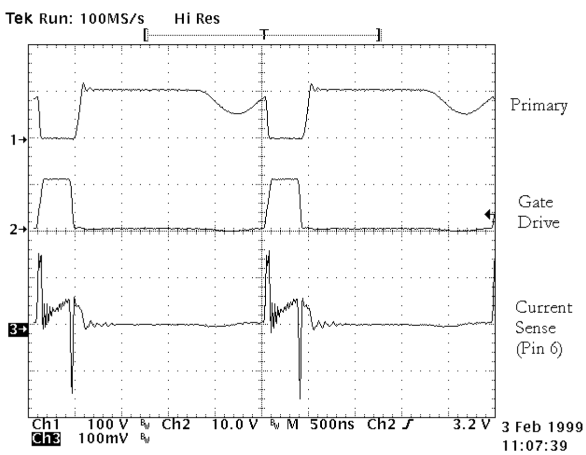

Figure 17. Current Sense 75 V_{IN}, 0.15 A Out

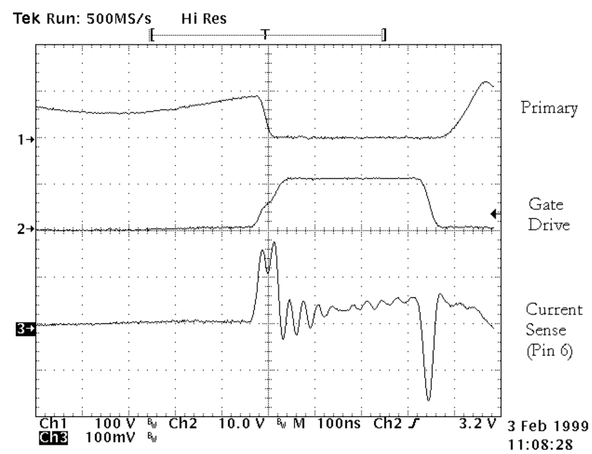

Figure 18. Current Sense 75 VIN, 0.15 A Out Expanded

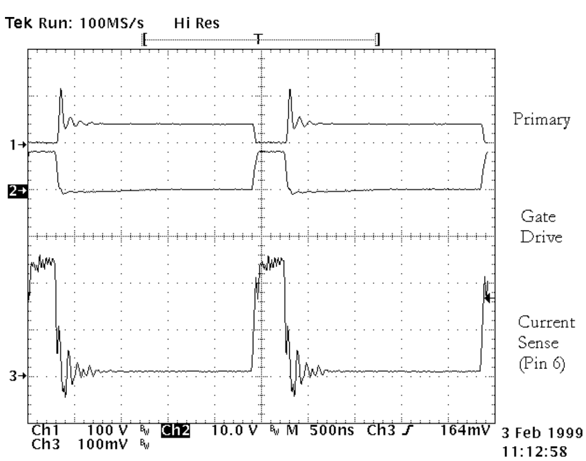

Figure 19. Current Sense 36 V_{IN}, Output Shorted

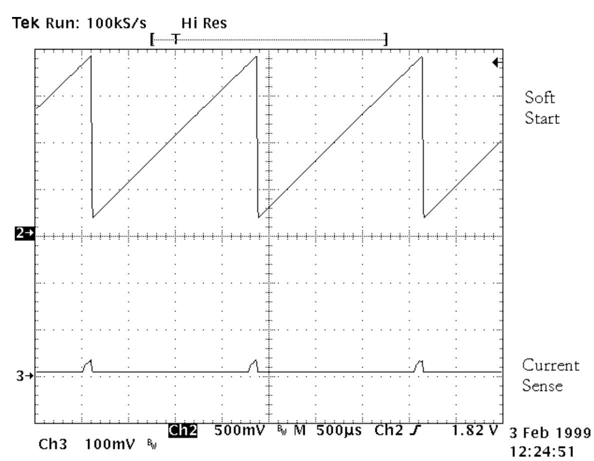

Figure 20. Second Threshold Operation 75 VIN, Output Shorted (Current Sense Pulses Are Attenuated Due to Sampling Frequency)

TYPICAL PERFORMANCE CHARACTERISTICS

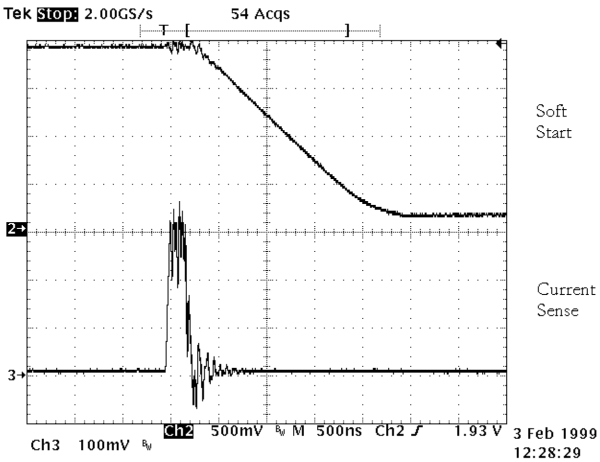

Figure 21. Second Threshold Operation-The Last Pulse Before Soft Start, 75 V_{IN}, Output Shorted

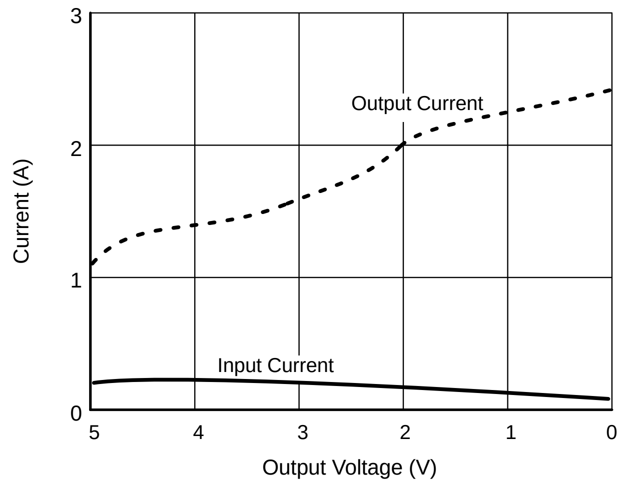

Figure 22. V-I Curves During High Output Currents and 36 V_{IN}

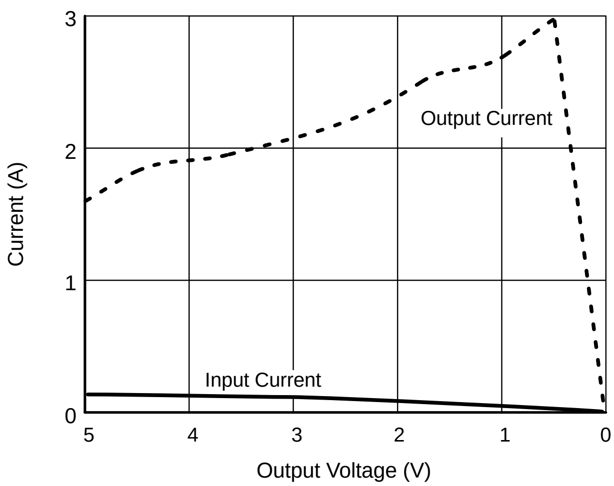

Figure 23. V-I Curves During High Output Currents and 75 V_{IN} (Low Currents Near 0 V_{OUT} Occur During Hiccup Mode)

Location	0.15 A Output	1.0 A Output	Shorted Output (~2.5 A)
Ambient	24°C	25°C	26°C
PCB (below U1 & U2)	27°C	31°C	37°C
U1	42°C	46°C	52°C
U2	28°C	36°C	46°C
Q2	31°C	40°C	46°C
T1	30°C	45°C	67°C
D1	28°C	43°C	72°C

Figure 24. Component Temperature at 48 V_{IN}

BILL OF MATERIALS

Item	Qty	Reference	Part	Mfg. & P/N	Distributor
Converter					
1	1	C1	cer, 0.1 μF, 100 V, 1206	TDK C3216X7R2A104K	TDK 603-886-6600
2	1	C2	cer, 1.5 μF, 100 V	TDK C5750XR72A155K	TDK
3	1	C3	cer, 0.022 μF, 50 V, 0805	TDK C2012X7R1H223K	TDK
4	1	C4	0.47 μF, 25 V, 1206	TDK C3216X7R1E474K	TDK
5	1	C5	47 μF, 6.3 V	Panasonic EEFCDOJ470R	Digi-Key 800-344-4539
6	2	C6, C7	cer, 0.01 μF, 50 V, 0805	TDK C2012X7R1H103K	TDK
7	2	C8, C9 Note 1	cer, 1000 pF, 50 V, 0805	TDK C2012X7R1H102K	TDK
8	1	D1	Schottky	ON Semiconductor MBRD360	Newark
9	1	D2	Diode	ON Semiconductor BAS16LT1	Newark
10	1	L1	Inductor, 10 μH	J.W. Miller PM43-100M	Newark
11	1	Q1	MOSFET, 100 V	Zetex ZVN3310A	Digi-Key
12	1	Q2	MOSFET, 200 V, 0.8 Ω	International Rectifier IRFR220	Newark
13	1	R1	res, 510 k, 0805	Panasonic ERJ-6GEYJ514V	Digi-Key
14	1	R2	res, 200 k, 1%, 0805	Panasonic ERJ-6ENF2003V	Digi-Key
15	1	R3	res, 47 Ω, 0805	Panasonic ERJ-GEYJ470V	Digi-Key
16	1	R4	res, 10 Ω, 0805	Panasonic ERJ-GEYJ100V	Digi-Key
17	1	R5	res, 17.4 k, 0805	Panasonic ERJ-6ENF1742V	Digi-Key
18	1	R6	res, 1.0 k, 0805	Panasonic ERJ-GEYJ103V	Digi-Key
19	1	R7	res, 30.1 k, 0805	Panasonic ERJ-6ENF3012V	Digi-Key
20	1	R8	res, 0.39 Ω, 1%, 0805	Panasonic ERJ-6RQFR39V	Digi-Key
21	1	R9	res, 10 k, 1%, 0805	Panasonic ERJ-6ENF1002V	Digi-Key
22	1	T1	Transformer	Coiltronics CTX15-14514	Cooper Electronic Technologies 561-752-5000 www.cooperet.com
23	1	U1	Current Mode Controller	ON Semiconductor CS5124-DR8	ON Semiconductor 401-885-3600
24	1	U2 Note 2	Optoisolated Feedback Amp	Texas Instruments TPS5908	Wyle 781-271-9953
Miscellaneous					
1	4	TP1, 2, 4, 5	Turret Terminal	Cambion 160-1558-02-01-00	Newark
2	10	TP3, 6-14	Single Pin Header	Winpoint 201-01-S-3-02-T	-
3	4	F1-4	Standoff	Bumpons (Digi-Key) SJ5003-0-ND	Digi-Key

1. For the Rev-0 printed circuit, C9 is a leaded component on the solder side.
2. TPS5908 is now an obsolete part and may be replaced by a TLV431 and an MOC8106.

PCB LAYOUT

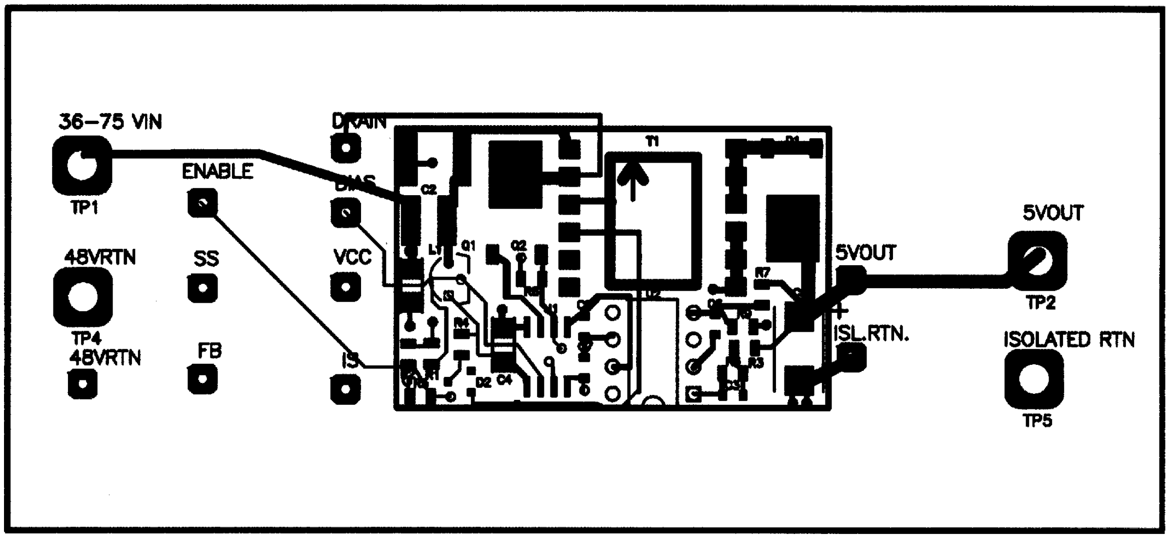

Figure 25. Top (Component) Layer

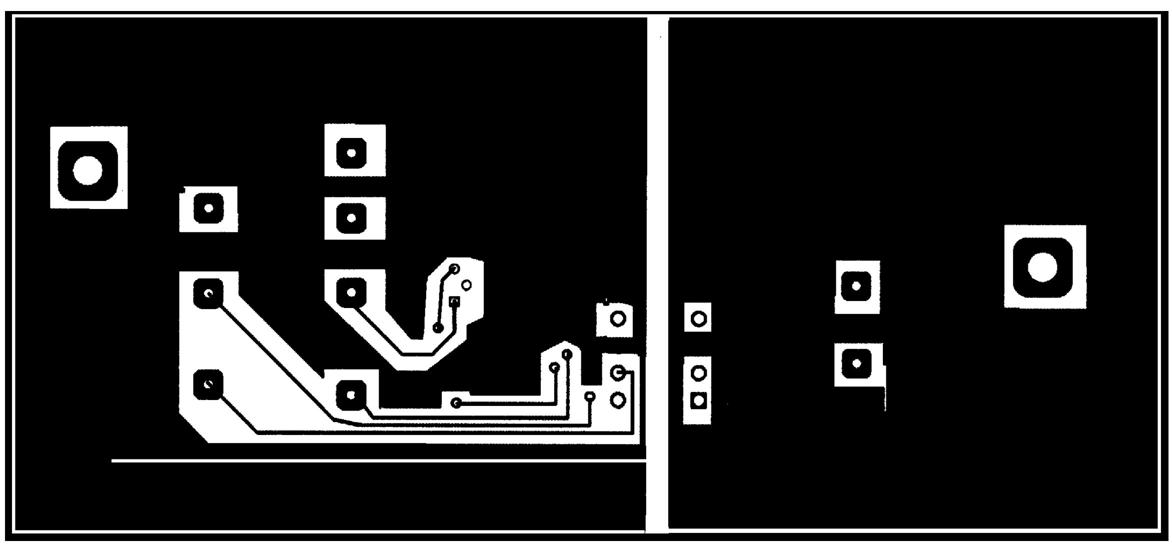

Figure 26. Bottom (Solder) Layer

PUBLICATION ORDERING INFORMATION

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