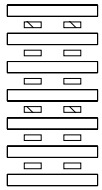
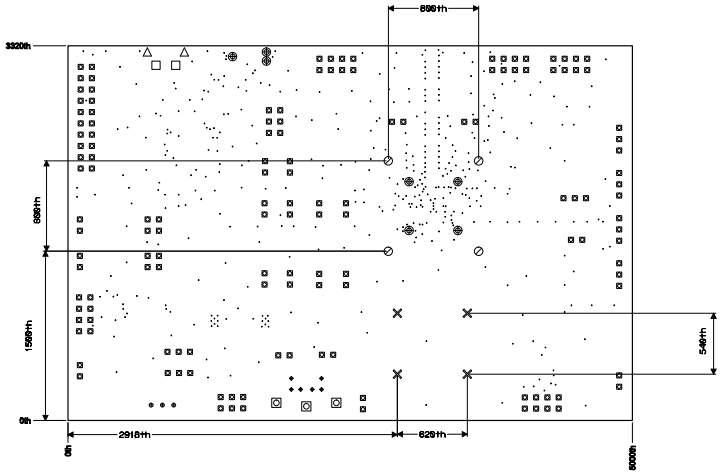
Layer Stackup
Design: E7160SL.pcb
Board thickness: 60.6



0.5th, SMT, Solder_Mask, Dk = 1
1.4th, SIGNAL_1, Microstrip_half_oz, Dk = 1
12th, DIELECTRIC_1, Core, Dk = 4.2
0.7th, SIGNAL_2, Plane, Dk = 1
10th, DIELECTRIC_2, Prepreg, Dk = 4.1
0.7th, SIGNAL_3, Stripline, Dk = 1
10th, DIELECTRIC_3, Core, Dk = 4.2
0.7th, SIGNAL_4, Stripline, Dk = 1
10th, DIELECTRIC_4, Prepreg, Dk = 4.1
0.7th, SIGNAL_5, Stripline, Dk = 1
12th, DIELECTRIC_5, Core, Dk = 4.2
1.4th, SIGNAL_6, Microstrip_half_oz, Dk = 1
0.5th, SMB, Solder_Mask, Dk = 1

NOTES:

1. Board material, FR4 RoHS Compliant [Hi-Temp FR4 (for wire bonding)] with nominal thickness of 0.062 INCH, 1/2 OZ. copper on top and bottom layers, 1/2 OZ. copper on inner layers.
2. Order of layers is TopLayer(Signal_1), Signal_2,Signal_3, Signal_4, Signal_5 and BottomLayer (Signal_6).
3. All dimension +/- 5 MIL unless specified otherwise.
4. LDI mask both sides. Mask must be between all lands. [Minimum of 1.5 MIL per side around BGA.]
5. Silkscreen to be white ink, soldermask green. No ink to be on surface mount land pads.
6. Board to use ENIG (Electroless Nickel Immersion Gold) finish.
7. Boards to be 100% tested to Gerber net list file.
8. Minimum hole plating 1MIL.
9. Include a minimum of two fiducials per panel.
10. Maximum warp/twist 0.005 INCH per INCH.
11. Controlled impedance board - top layer (TopLayer) to gnd (Layer_1) 22mil traces shall be 50 ohms +/-10%.
12. Fabricate to IPC-6012 Class 2.



All Holes

Symbol	Diameter	Tolerance	Plated	Punched	HoleName	Quantity	Span
○	0.0080	+/-0.003 INCH	Yes	No	Rnd 8	435	1-6
✦	0.0354	+/-0.003 INCH	Yes	No	Rnd 0.9mm	6	1-6
⊕	0.0390	+/-0.003 INCH	Yes	No	Rnd 39	3	1-6
⊠	0.0400	+/-0.003 INCH	Yes	No	Rnd 40	141	1-6
⊠	0.0866	+/-0.003 INCH	Yes	No	Rnd 86.6	3	1-6
●	0.0394	+/-0.003 INCH	No	No	Rnd 1 Non-Plated	7	1-6
⊘	0.1120	+/-0.003 INCH	No	No	Rnd 112 Non-Plated	4	1-6
✕	0.1750		No	No	Rnd 175 Non-Plated	4	1-6
△	0.0236	+/- 0.0020	Yes	No	Slot 1.3x0.6 +/-Tol 0.05mm	2	1-6
□	0.0276	+/- 0.0020	Yes	No	Slot 0.85x0.7 +/-Tol 0.05mm	2	1-6

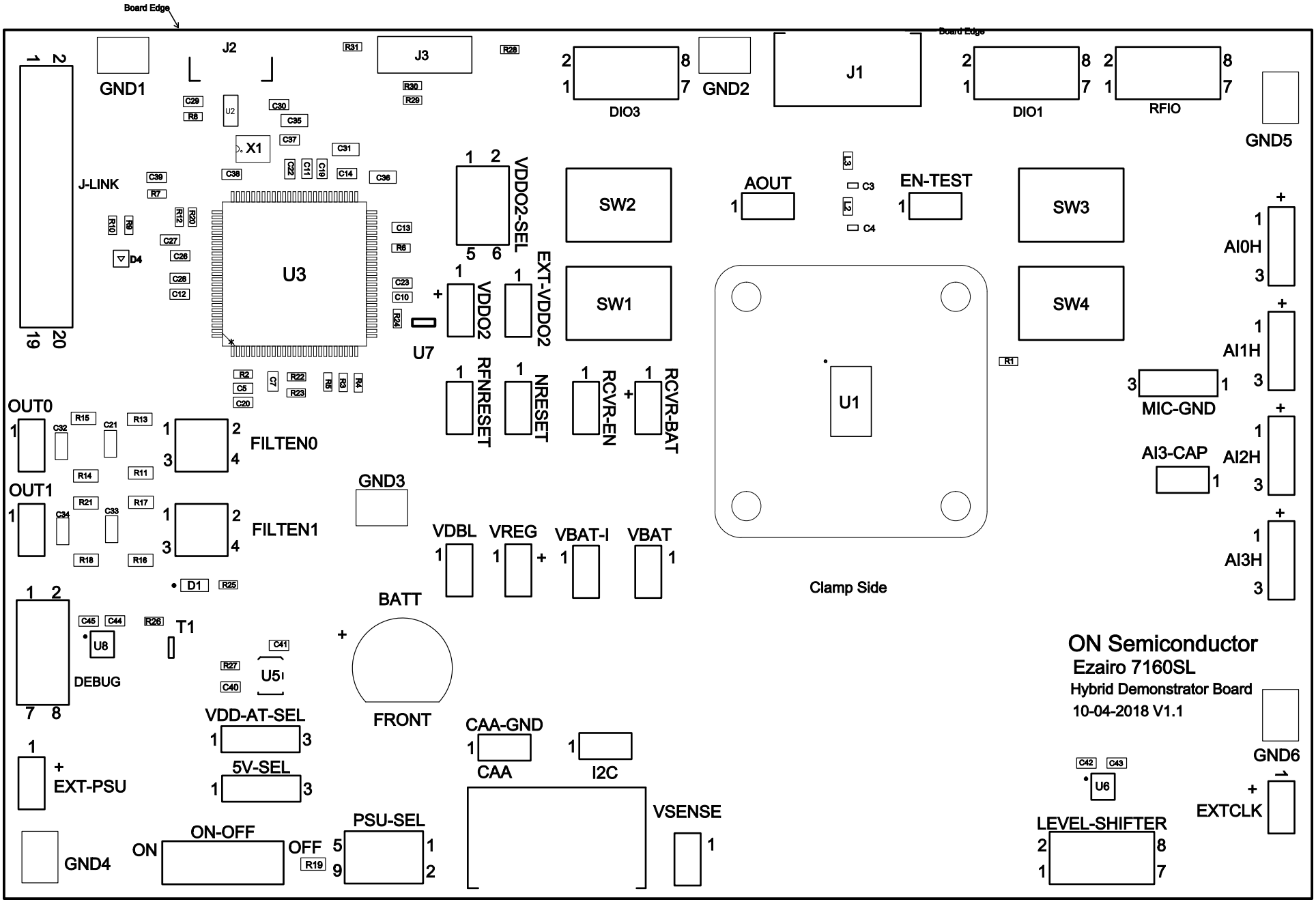
REVISION HISTORY	DATE
V1.0 Initial Design	12/21/201
V1.1 Corrected Level Shifter error	3/21/2018

ON Semiconductor
611 Kumpf Drive, Unit 200
Waterloo, Ont.
Canada, N2V 1K8

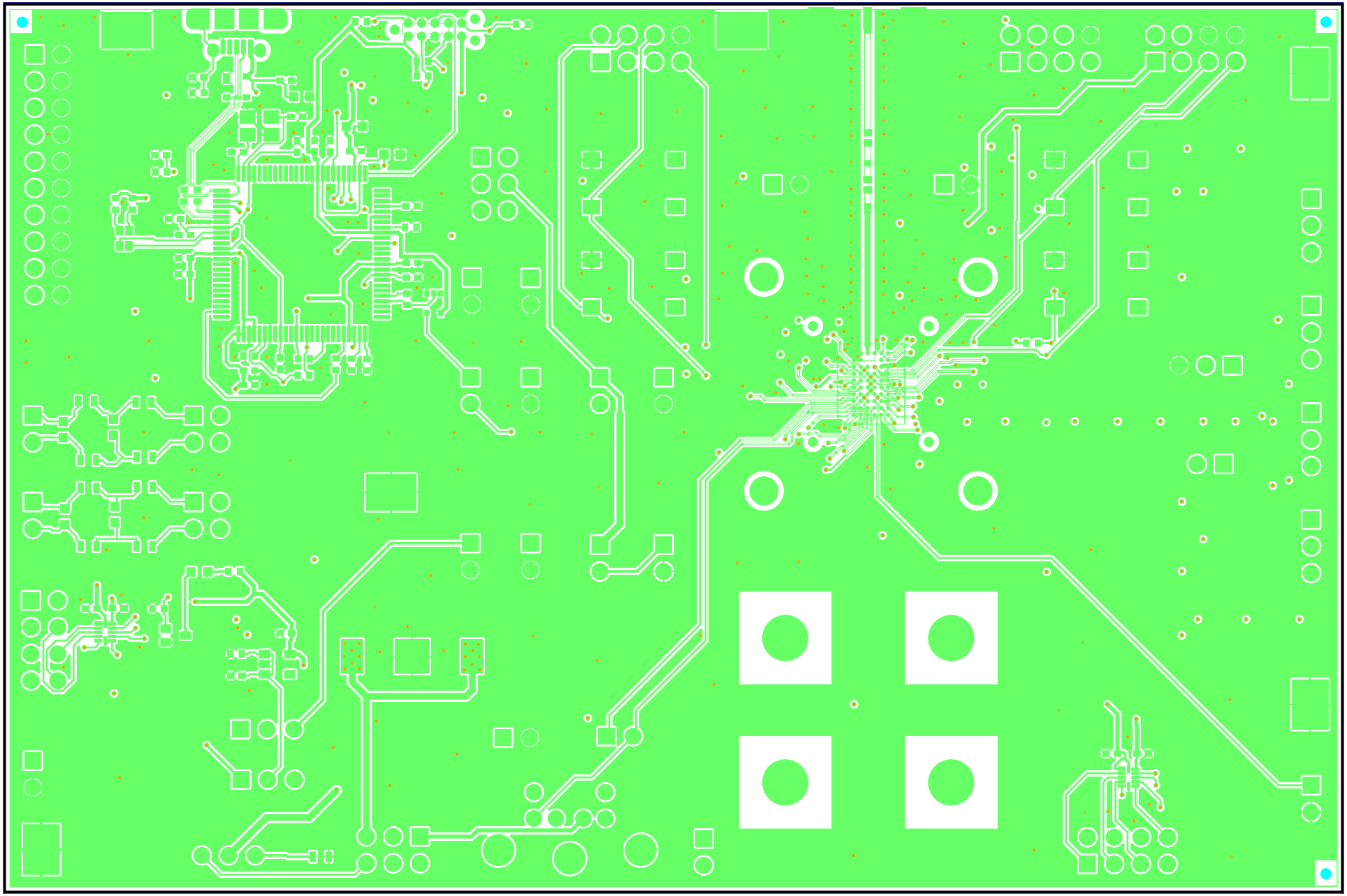
TITLE
Ezairo 7160SL HDB

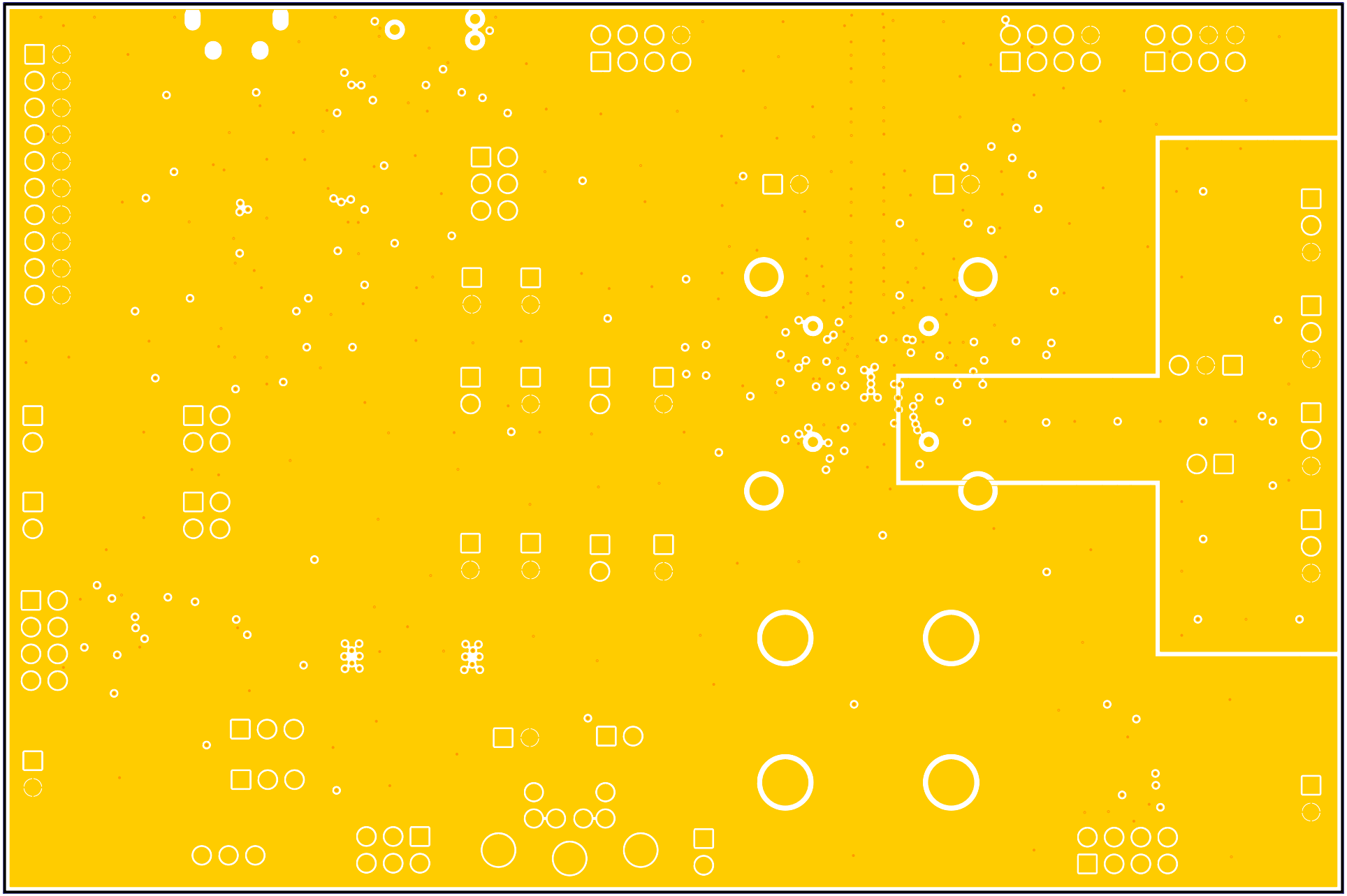
SIZE	NUMBER	REV
B	TBD	V1.1

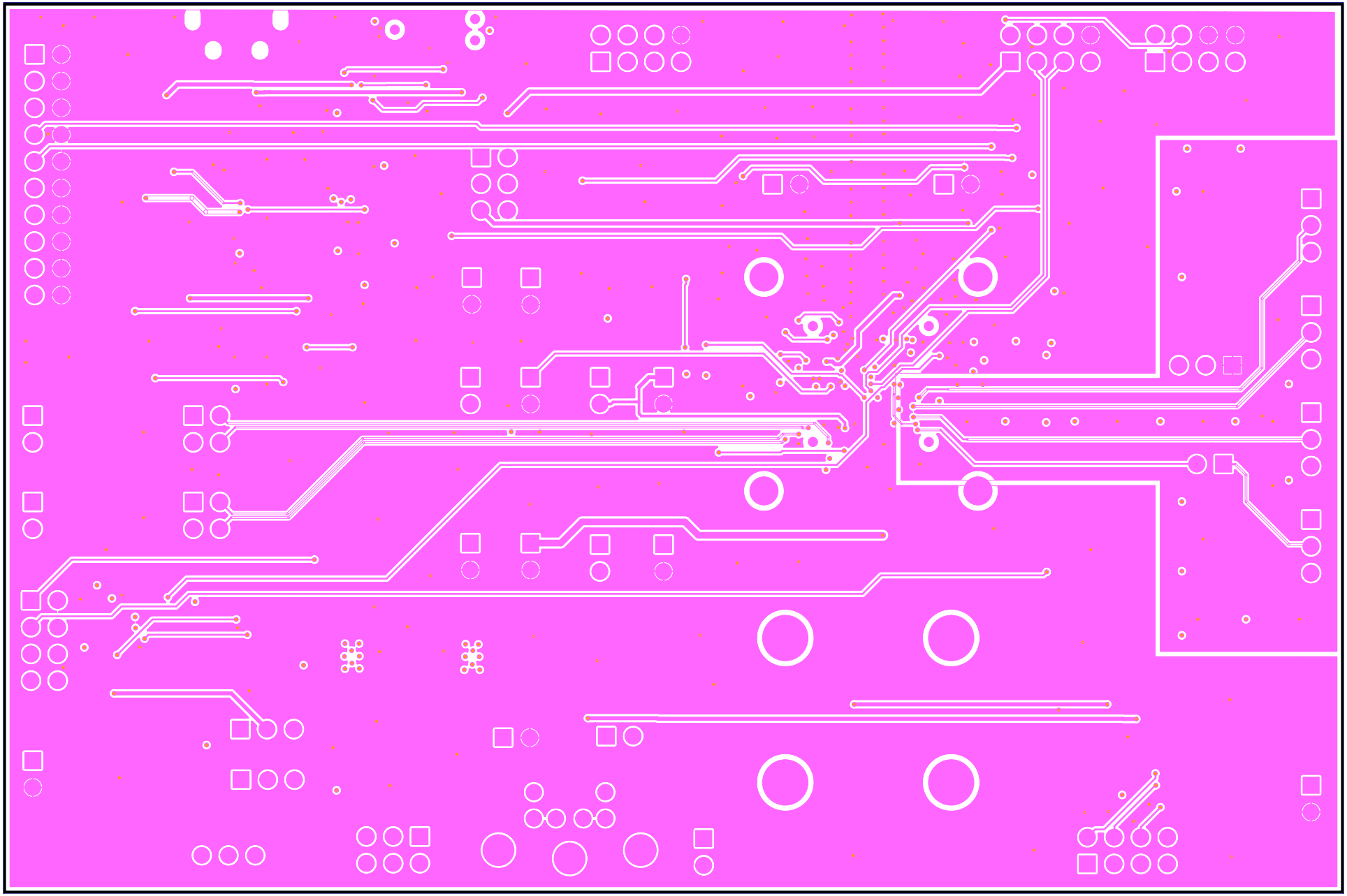
Drawn By		DATE	SHEET
Marius C.	Fabrication Drawing	21-Mar-2018	1 of 1

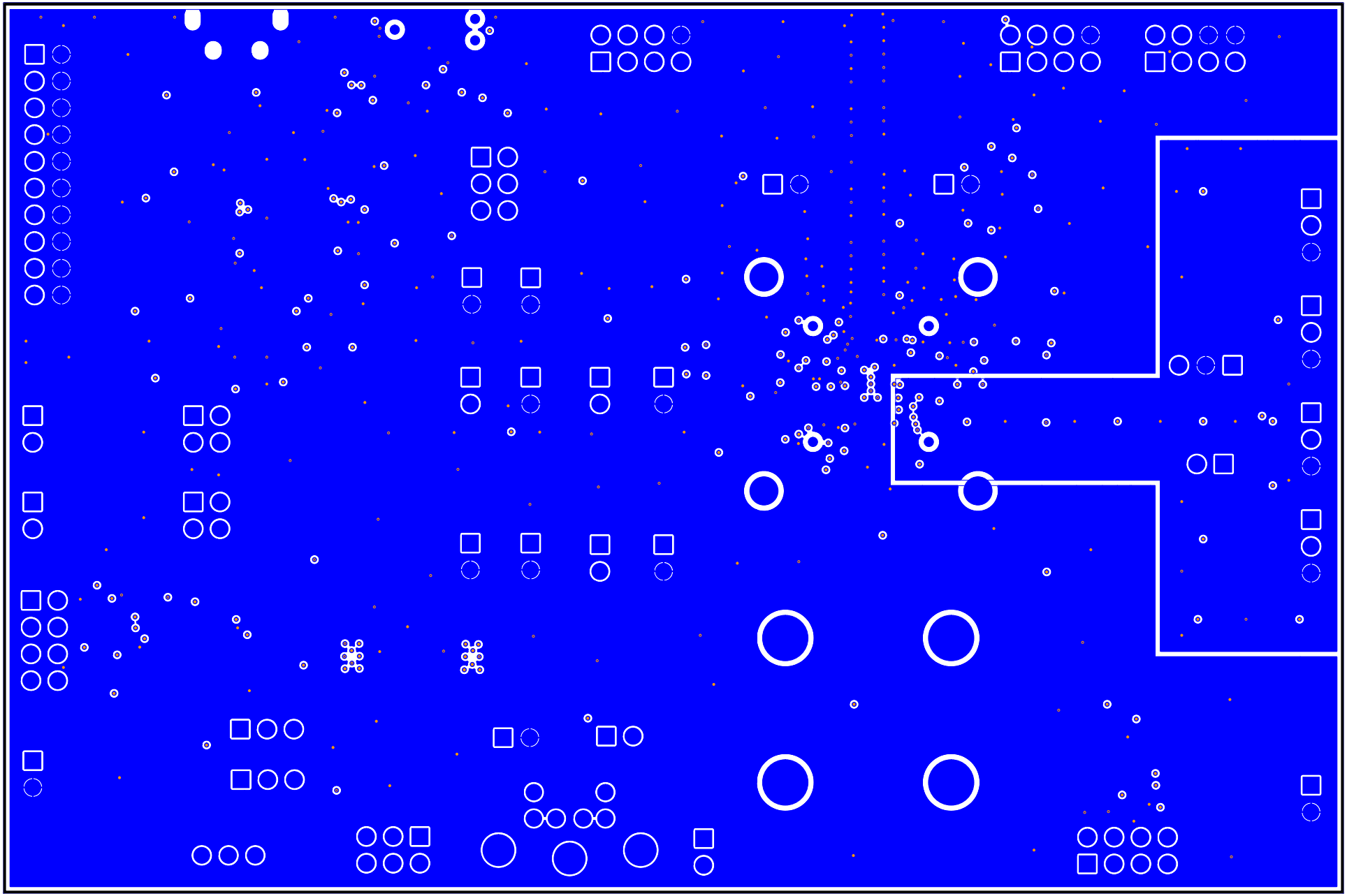

Board Edge
J2
J3
J1
GND1
GND2
GND5
GND3
GND4
GND6
DIO3
DIO1
RFIO
J-LINK
U3
U7
U1
U2
U5
U6
U8
X1
D1
D4
T1
VDDO2-SEL
VDDO2
EXT-VDDO2
SW1
SW2
SW3
SW4
AOUT
EN-TEST
AI0H
AI1H
AI2H
AI3H
MIC-GND
AI3-CAP
OUT0
OUT1
FILTEN0
FILTEN1
RFNRESET
NRESET
RCVR-EN
RCVR-BAT
VDBL
VREG
VBAT-I
VBAT
BATT
FRONT
Clamp Side
DEBUG
VDD-AT-SEL
5V-SEL
EXT-PSU
CAA-GND
CAA
I2C
VSENSE
ON-OFF
ON
OFF
PSU-SEL
LEVEL-SHIFTER
EXTCLK
ON Semiconductor
Ezairo 7160SL
Hybrid Demonstrator Board
10-04-2018 V1.1

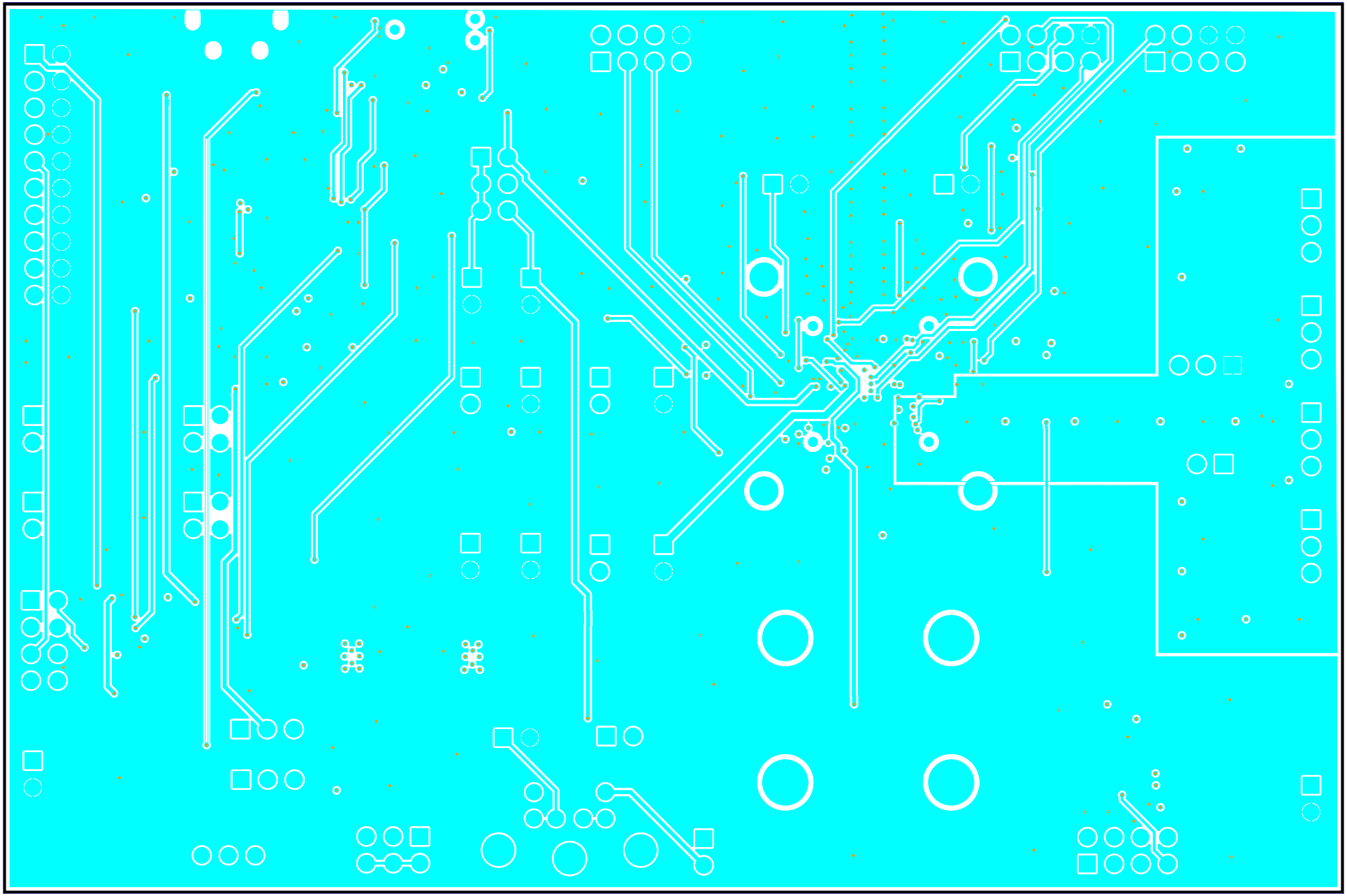
Y1
C26
C18
C17
C9
C16
C8
C10
L1
R2
L2

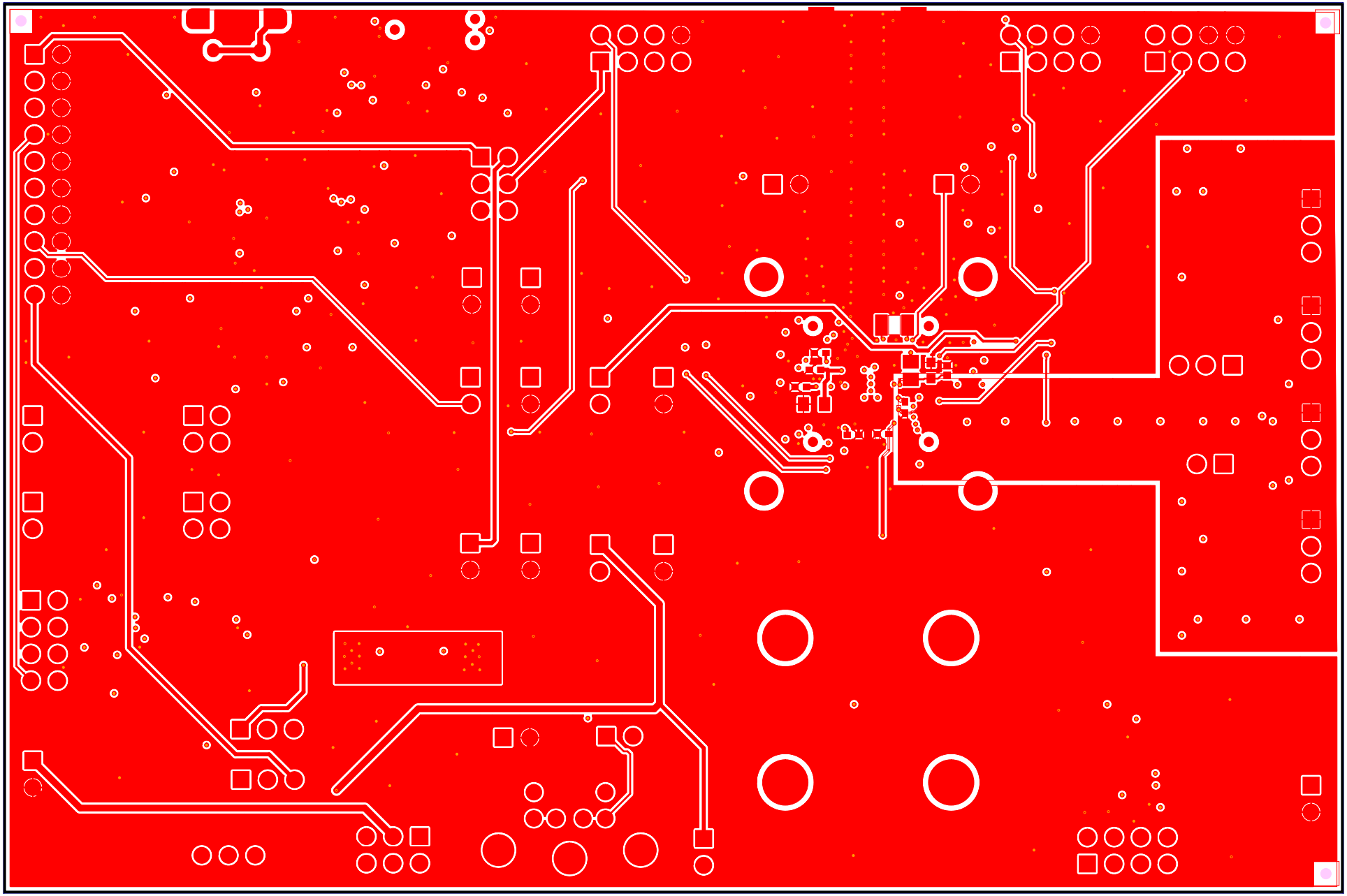


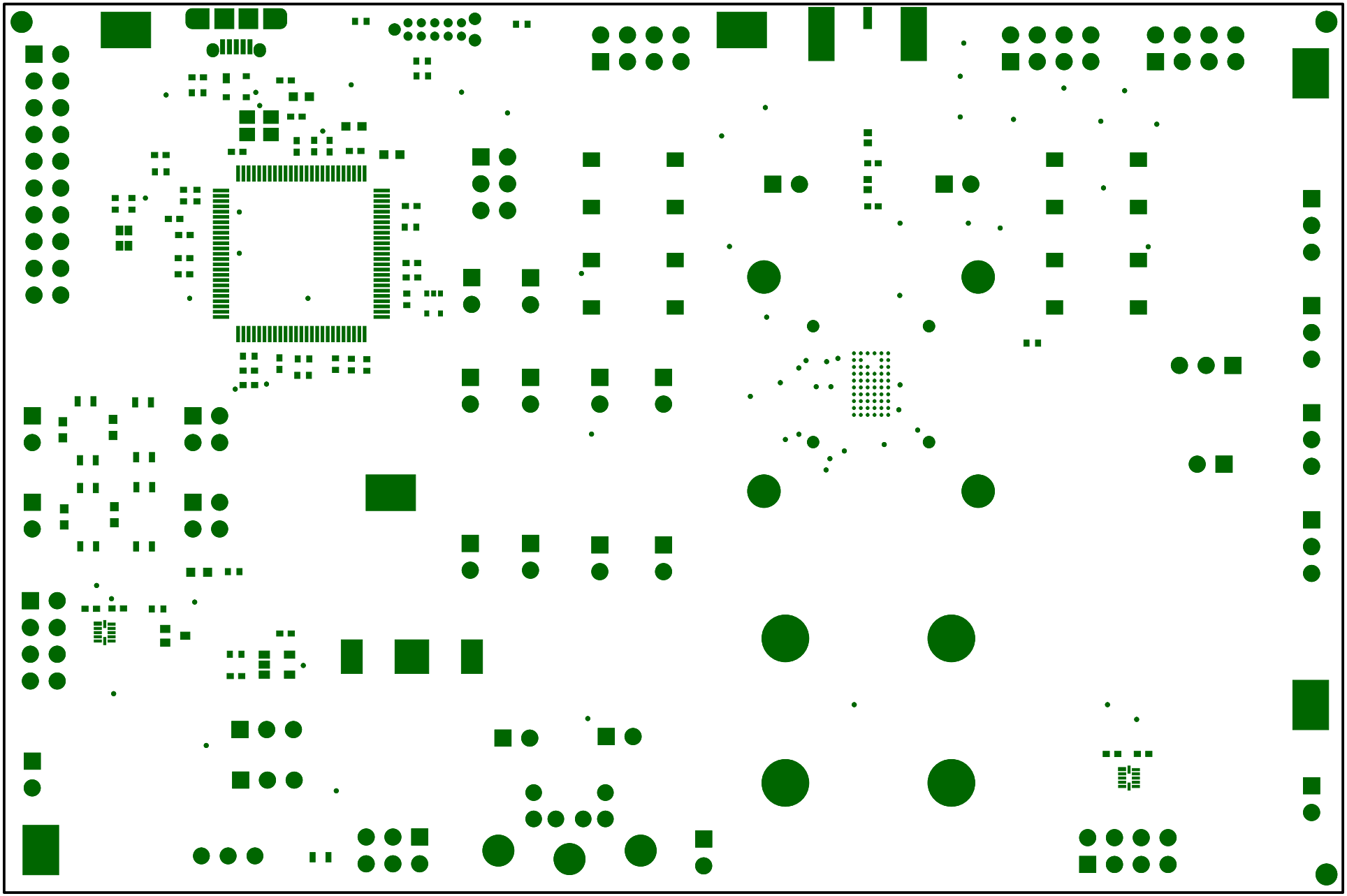


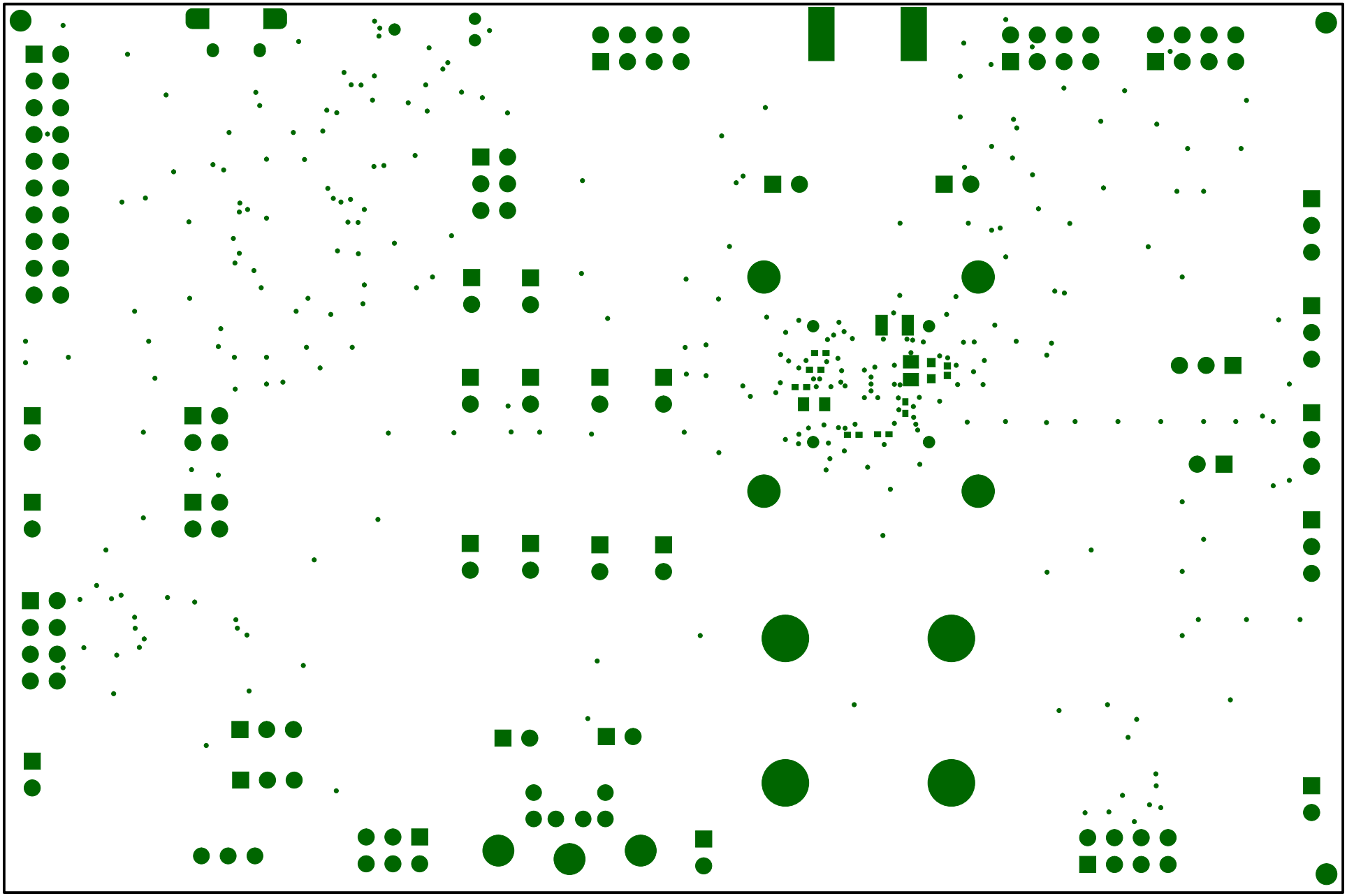


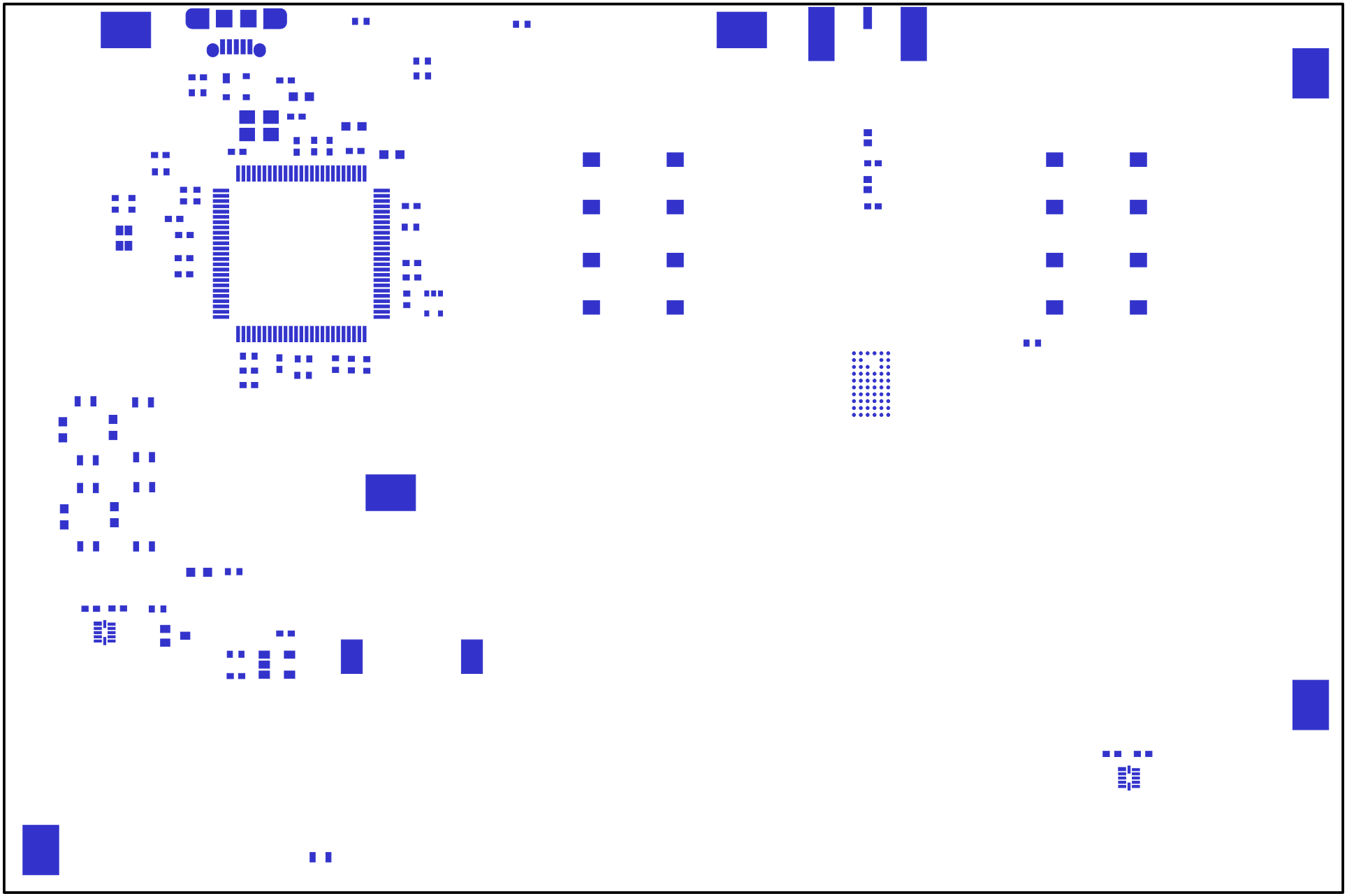


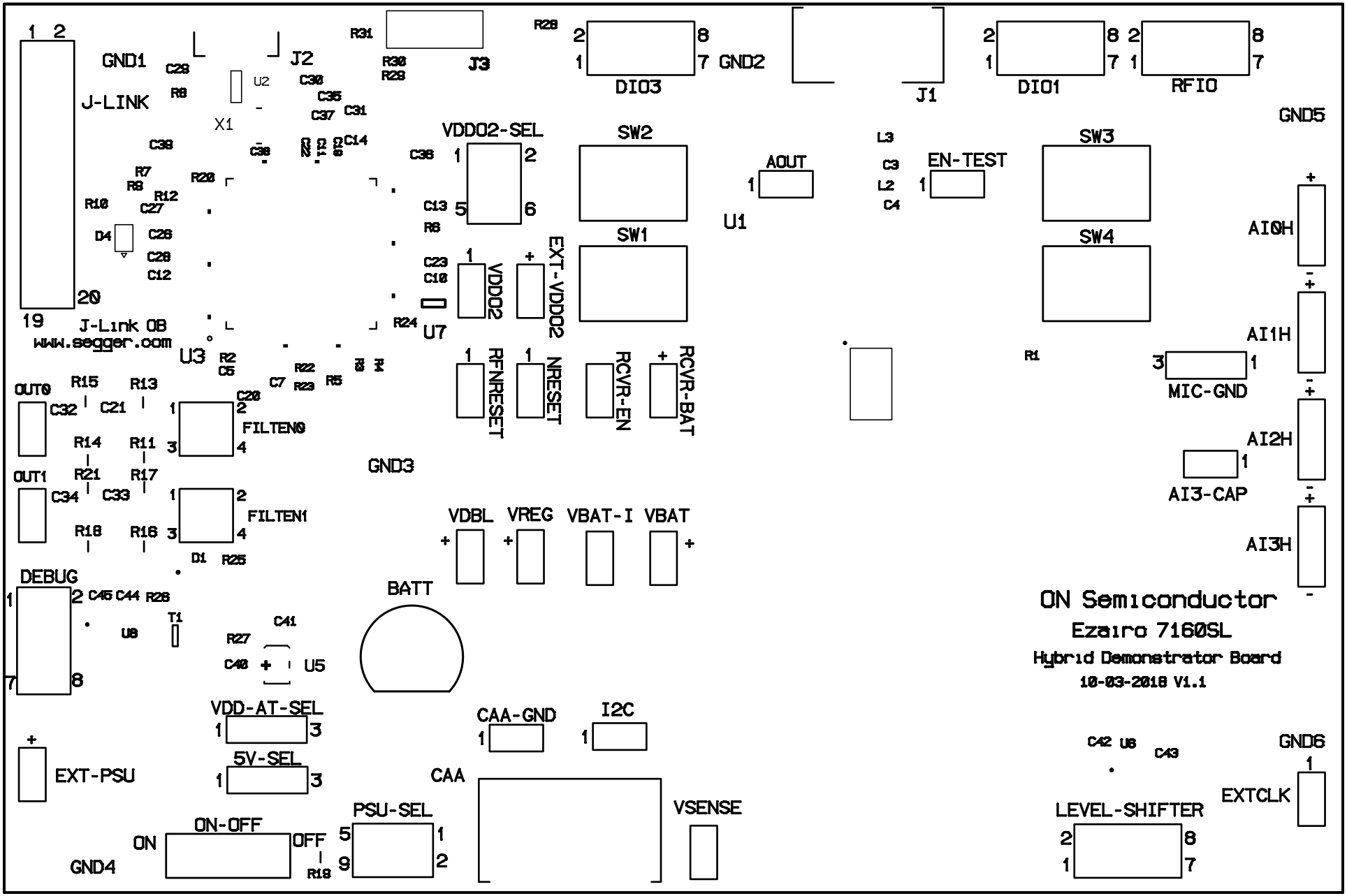











J-LINK
GND1
J2
J3
DIO3
GND2
J1
DIO1
RFIO
GND5
VDDO2-SEL
SW2
SW1
SW3
SW4
AOUT
EN-TEST
U1
AI0H
AI1H
AI2H
AI3H
MIC-GND
AI3-CAP
J-Link OB
www.segger.com
U3
U7
VDDO2
EXT-VDDO2
RFNRESET
NRESET
RCVR-EN
RCVR-BAT
OUT0
OUT1
FILTEN0
FILTEN1
GND3
VDBL
VREG
VBAT-I
VBAT
DEBUG
BATT
U5
VDD-AT-SEL
5V-SEL
CAA-GND
I2C
CAA
VSENSE
EXT-PSU
ON-OFF
ON
OFF
GND4
PSU-SEL
LEVEL-SHIFTER
GND6
EXTCLK
ON Semiconductor
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Y1
C2
C4
L1
C26
C18
C17
C8
C16
C15
C6