Dynamic Test Solution's

FABRICATION SPECIFICATION

for

FULL GOLD PLATED PCBs

DTS-FAB-SPEC REV F

REV	ECO	DESCRIPTION	CHK	DATE	APP
A	RELEASE	RELEASE TO PRODUCTION	KLR	4/4/05	KRE
B		Addition of Plating Types	KLR	4/15/05	KRE
C		New Logo and File Name	KLR	9/8/06	KRE
D		Additional Desiccant Requirements	KLR	12/11/06	KLR
E		Additional Specifications	KMC	19/12/14	KMC
F		Change Isolation Resistance Requirement. Added Copper Thieving	CIT	21/09/2017	ENO
G		Added Drilling Information	RDP/MD	06/12/2018	ENO

Purpose. This document establishes general requirements for fabrication and inspection of full-gold plated printed circuit boards (PCBs). The intent of this specification is to promote a common understanding of PCB requirements between Dynamic Test Solution's Design Groups, Purchasing, Quality, and the supplier base

Scope. The requirements of this specification apply to all PCBs purchased by Dynamic Test Solutions unless exceptions are noted on the purchase order or the PCB fabrication drawing.

Order of Precedence. The purchase of PCBs is controlled by several different types of data and documents. In the event of a conflict, the following order of precedence applies:

Purchase Order
PCB Fabrication Drawing
PCB Fabrication Specification (this document)
IPC specifications and standards
PCB supplier's standard practice

Specifications.

Interpret this drawing in accordance with IPC-D-325A.
Board fabrication and quality per IPC-6012, Class 2.
All specifications used shall be their latest revisions.
Parenthetical information is for reference only.

Functional Requirements

Data Changes. Absolutely no changes are to be made to our data without our knowledge and consent, excepting, country of origin changes to silkscreen when necessary.

Bow and Twist. Bow and twist shall be limited to 0.005 inch per linear inch as measured per IPC-TM-650, method 2.4.22. In addition, overall board flatness may be specified on the PCB fabrication drawing as a functional requirement for vacuum applications.

Interpretation. All dimensions shall be interpreted in accordance with ASME Y14.5M-1994. All dimensions shall apply after plating.

Hole Location. All drilled holes shall be located per Dynamic Test Solution's supplied drill file and shall fall within 0.003 in. of true position, as measured per IPC-TM-650 section 2.2.10. Hole chart quantities on the PCB fabrication drawing are for reference only.

Inside Corner Radius shall be held to 0.125 in. maximum.

Tolerances. Dimensional tolerances shall be interpreted as follows: two place decimals ± 0.010 in. three place decimals ± 0.005 in. four place decimals ± 0.0005 in. angles ± 0.5° Drilled hole tolerances shall be as specified on the fabrication drawing.

Construction. Printed circuit board fabrication shall be in general accordance with IPC-A-600G. Board edges shall be clean with no chipping or cracking. All burrs and sharp edges shall be removed, 0.015" max radius. Chamfer and Bevel at edge of contacts shall be smooth and clean with no burrs attached to contacts.

Controlled Impedance. PCBs or individual signal layers designated as controlled impedance on the PCB fabrication drawing shall be fabricated to achieve target impedance within ± 10%. A TDR reading will be performed by the vendor for each controlled impedance layer with an additional reading for any 100 ohm differential pair layer. A TDR report will be provided by the vendor for each PCB.

Overall Thickness. Accumulation of individual inner layer thickness and tolerances shall be optimized to achieve overall thickness as specified on the PCB fabrication drawing, when measured over lands and/or conductors not covered by soldermask (metal-metal).

PCB Materials will be specified on the fabrication drawing. Individual layer material usage will be the vendor's choice as long as impedance requirements and overall thickness can be met. Fabrication drawings may call out dielectric thickness for individual layers, which supersedes vendor's option. Conductive layers shall consist of flame retardant, glass-based epoxy resin with 1 oz. copper cladding on external layers and ½ oz. copper cladding on internal layers (All copper weights are finished), per IPC-4101A. Pre-impregnated "B" stage epoxy glass cloth per IPC-4101A shall be used for adhesive layers. If any PCB does not meet the end users requirements, then a detailed stacking will be required to verify PCB construction.

Lamination Integrity shall prevent voids and de-lamination as measured in accordance with IPC-TM-650 section 2.1.1.

Layer-to-Layer Registration shall be held to ± 0.003 inch overall, as measured per IPC-TM-650 section 2.1.1 and 2.1.11.

Trace Width shall be held to within ± 10% of Gerber data on internal layers and to within ± 15% of Gerber data on external layers, as measured per IPC-TM-650 section 2.2.9.

Copper Thieving (Solid) allowed on all inner layers per Fab Vendors recommendation.

- Thieving Shape- Square
- Thieving Size- 30mils
- Thieving Pitch- 50mils
- Thieving to any board feature-50mils

Plating.

Standard Gold Plating 1 (Light Gold):
External conductive surfaces shall be plated to a minimum thickness of 200 µin. with low- stress sulfamate nickel or tin-nickel per QQ-N-290. These surfaces shall then be finish plated to a thickness of 5-10µ in. with hard bright gold per MIL-G-45204, Type II, Class I.

Standard Gold Plating 2 (Hard Gold):
External conductive surfaces shall be plated to a minimum thickness of 200 µin. with low- stress sulfamate nickel or tin-nickel per QQ-N-290. These surfaces shall then be finish plated to a minimum thickness of 50 µin. and a maximum thickness of 70µin. with hard bright gold per MIL-G-45204, Type II, Class I.

Selective Gold Plating:
External conductive surfaces shall be plated to a minimum thickness of 200 µin. with low-stress sulfamate nickel or tin-nickel per QQ-N-290. These surfaces shall then be finish plated to a minimum thickness of 5 µin. and a maximum thickness of 10 µin. with hard bright gold per MIL-G-45204, Type II, Class I. Selectively plate areas indicated using provided data to a minimum thickness of 50 µin. and a maximum thickness of 70 µin. with hard bright gold per MIL-G-45204, Type II, Class I.

Barrel plating (through-hole).
Through-holes shall be plated to a minimum thickness of 0.001 in. as measured per IPC-TM-650 section 2.1.1 (or 2.2.13.1).

Annular Rings.
Annular rings shall be plated to a minimum width of 0.002 in. on all layers as measured per IPC-TM-650 sections 2.2.7, 2.1.1, and 2.1.11. No plating breakout shall be allowable.

Drilling Information
Drill table information located at Fabrication Drawing is for finished hole size.

Soldermask. Liquid photo-Imageable (LPI) soldermask, per IPC-SM-840, Class T, color green, shall be applied to a finished thickness of 0.001 in. minimum, 0.003 in. maximum (mask over circuitry). There shall be no foreign material under the mask, no exposed copper, and no solder mask bleed out onto solder pads. Selected material shall be compatible with rosin flux and Allied Signal Genesolv® cleaning solvents. Application shall conform to manufacturer's specifications.

NO DRY FILM SHALL BE USED ON ANY BOARD NEW OR REORDER REGARDLESS OF FABRICATION DRAWING'S SPECIFICATIONS. ONLY LPI (AS DETAILED ABOVE.)

FOR HOLES PLUGGED WITH MASK FOR VACUUM APPLICATION, SR1000 (WET MASK) SHALL BE USED TO PLUG THE HOLES WHICH SHALL THEN BE COVERED WITH LPI.

Legend shall be silkscreened on finished board per supplied Gerber file(s) using permanent white non-conductive epoxy ink. Markings may extend onto plated surfaces as long as the layer-to-layer registration requirement is met. If needed, additional legend colors may be requested on the fabrication drawing.

Vendor Markings. Vendor logos are not permitted. Date Codes shall be written in 6 digits XX/XX/XX. First two digits are month, Second two digits are day, Third two digits are year.

Test/QA

Test methods shall be in compliance with IPC-TM-650

Boards must be tested 100% using the following parameters:

Continuity Resistance of 5 Ohm maximum.

100% through-hole continuity test on all exposed (non-tented) vias.

Isolation Resistance of ≥10 mega ohm.

Isolation Resistance of ≥100 mega ohm (LOW LEAKAGE APPLICATION).

Test Impedance of at least one trace from each trace layer on every board.

Overall Thickness as specified on the PCB fabrication drawing, when measured between outside solder masked surfaces (mask-mask). If soldermask is not required then it shall be measured between outside plated surfaces (metal-metal.)

Leakage on printed circuit boards shall not exceed 2nA / Volt on power to ground and signals.

Each board shall be stamped with non-conductive ink after passing electrical test.

Cosmetic Quality is required to be good on all boards. No scratches, foreign material, finger prints, voids in soldermask, discoloration of soldermask, and inconsistencies in gold plating are permitted.

Repair of PCB defects is not permitted.

Ionic Contamination

Printed Circuit Boards shall be cleaned after etching. Surface contamination including flux activators, fingerprints, etching or plating salts shall be below 7.0 micrograms. Certifications are requested as long as they are not cost adders.

Packaging

Finished PCB's shall be individually packaged in plastic bags (anti-static if possible.) A single one-gram pouch of Desiccant is required in each individual sealed bag.

Quantities greater than 10 parts must be bubble wrapped in lots of 10.

All shipments must be bubble wrapped.

Leave a minimum space of one inch between the product and each side of the box (board/boards). Use adequate amount of bubble wrap or equivalent protection to ensure protection from damage while in transit.

Attach a packing slip to the outside of the shipping container. If more than one container is required, number the containers, i.e. 1/6

Packing slips shall contain the purchase order number, item number, quantity being shipped, and date of shipment along with method of transportation. Packing slips must be numbered.

Sampling/Certification Requirements

Required for every order:

Certificate of Conformance shall assert that the following information specified in the DTS purchase order and /or specification is in conformance.

- Customer Name
- PO number
- Part Number
- Revision
- Quantity
- Date code
- Quality Representative signature

Electrical Test Certification shall contain verification that test and parameter values have been performed in accordance with the tests listed below and include the following information.

- Customer name
- Part Number
- Revision level
- Date tested
- Representative signature

Test Parameters

- Voltage
- Continuity Resistance
- Isolation Resistance
- Leakage

XRF Test Results – Plating and Coating Thickness (representative sampling)

- Au/Ni/Cu

First Article Report – Complete measurements results taken from drawing and verified with all values obtained.

- Hole sizes (Counter sink, Counterbore, Depth Drill, Slots)
- Mechanical Dimensions (Actual Dimensional Measurement)
- Overall Thickness – Finished Thickness Mask-Mask (Metal-Metal when Mask is not present)
- Bow and Twist Results
- Drawing Notes – Verified