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FSL5x8 Application Note
Design example: 12V/8W

Application Engineer

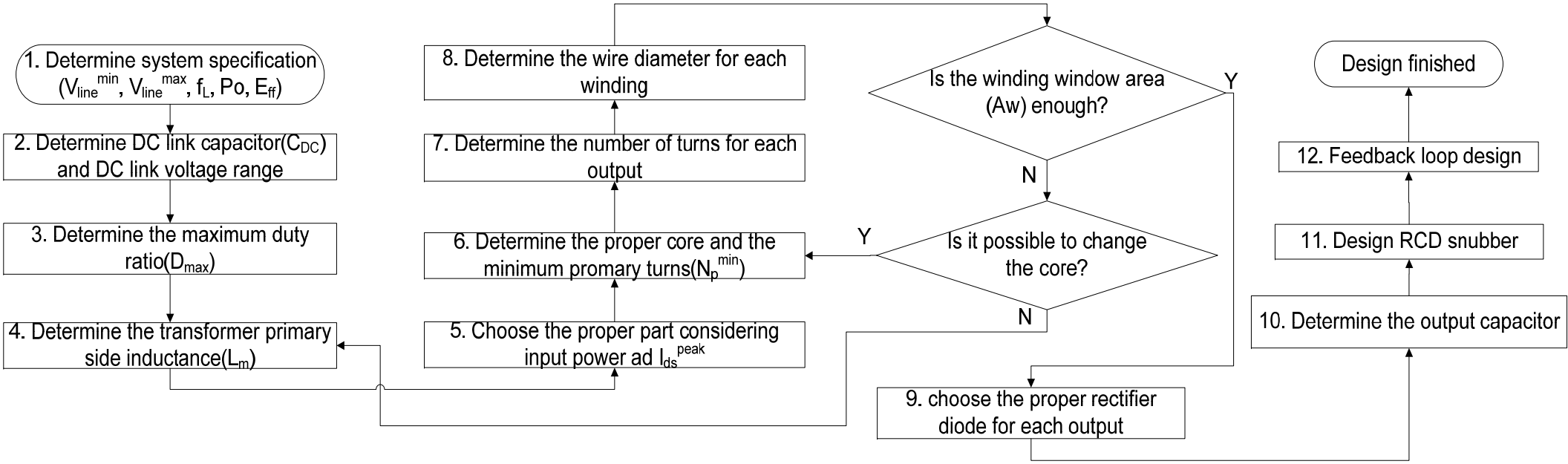
ON Semiconductor®

Internal Use Only

Content

1. The application note is defined for user understanding design tool guideline and procedure
2. Through “Design flow” chart to understand design tool procedure
3. Please input specification or value into Blue Cell and calculation result will present in Red Cell.
4. Design example with12V/8W Isolation type.
   - ❑ DN05123: 8W auxiliary power for white goods and industrial equipment with FSL518APG (https://www.onsemi.com/pub/Collateral/DN05123.PDF)

Design flow



Define the system specifications (Design example: 12V/8W)

1. Define the system specifications									
Minimum Line voltage (V_{line}^{min})	90	V.rms							
Maximum Line voltage (V_{line}^{max})	264	V.rms							
Line frequency (f_L)	60	Hz							
Part Selection	FSL518A								
	$V_{O(n)}$		$I_{O(n)}$		$P_{O(n)}$		$K_{L(n)}$		
1st output for feedback	12	V	0.67	A	8	W	100	%	
2nd output	0	V	0.00	A	0	W	0	%	
3rd output	0	V	0.00	A	0	W	0	%	
4th output	0	V	0.00	A	0	W	0	%	
5th output	0	V	0.00	A	0	W	0	%	
6th output	0	V	0.00	A	0	W	0	%	
Full load output power (P_o) =	8.0	W							
Estimated efficiency (E_{ff})	84	%							
Full load input power (P_{in}) =	9.6	W							

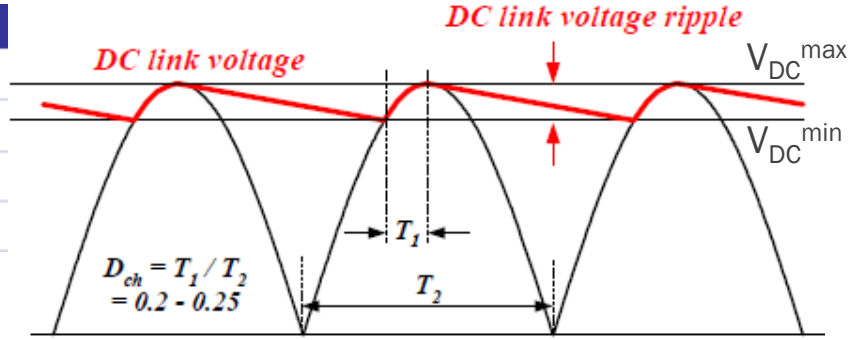
Blue Cell : Key-in specification or value

Red Cell : Calculation result

-Line voltage range(V_{line}^{min} and V_{line}^{max}): input line voltage information for system design definition
Line frequency(f_L): input line voltage frequency
-Part Selection: Choice one of FSL5x8 part for design
-Maximum output power(Po): Summation of all outputs power
-Load occupying factor for n-th output $K_L(n)$
-Estimated efficiency(E_{ff}): Estimate the power conversion efficiency to calculate maximum input power

Determine DC link capacitor and DC link voltage range

2. Determine DC link capacitor and DC link voltage range		
DC link capacitor (C_{DC})	18	uF
Bulk capacitor charging duty ratio (D_{CH})	0.2	
Minimum DC link voltage (V_{DC}^{min}) =	95	V
Maximum DC link voltage (V_{DC}^{max})=	373	V



-DC link capacitor(C_{DC}): Using 2~3uF per output wattage

-Bulk capacitor charging duty ratio(D_{CH}): D_{CH} is the DC link capacitor charging duty ratio, typical is 0.2

-V_{DC}^{min}= the minimum DC link voltage

-V_{DC}^{max}= the maximum DC link voltage

Adjusted C_{DC} base-on output power, and considering V_{DC}^{min} level.

Determine Maximum duty ratio

3. Determine Maximum duty ratio (Dmax)			
Output voltage reflected to primary (V_{RO})	80.0 V		
Maximum duty ratio for CCM at full loading($D_{max.ccm}$) =	0.456		
Maximum duty ratio at full loading (D_{max})	0.395	--->DCM operation	
Max nominal MOSFET voltage (V_{ds}^{nom}) =	453 V		

-Output voltage reflected to primary(V_{RO}): determine the turn ratio from Vo*(Np/Ns)

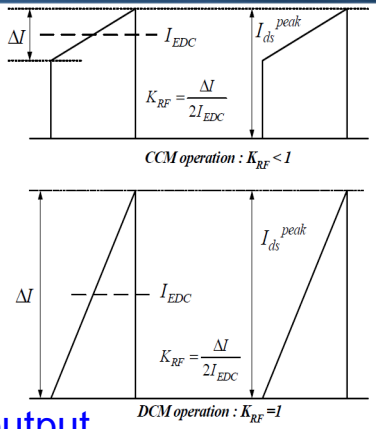
-Maximum duty ratio at full loading: $D_{max.ccm}$ been calculated by V_{RO}/(Vdc_min+V_{RO}), you can determine the maximum duty in your system.

-Maximum nominal MOSFET voltage(V_{ds}^{nom}): MOSFET maximum voltage with spike by (V_{dc_max} + V_{RO})

Selected V_{RO} with proper range (recommend range: 70V~110V), and set D_{max} to determine operation mode with CCM or DCM. If D_{max}=$D_{max.ccm}$, the operation will be CCM, otherwise will be DCM. Notice the D_{max} would be smaller than 68%(D_{MAX} min. value).

Determine transformer Primary Inductance (Lm) -1

4. Determine transformer primary inductance (Lm)			
Switching frequency of FSL5x8 (f_s)	100	kHz	
Ripple factor (K_{RF})	1		--->ok
Primary side inductance (L_m) =	743	uH	
Distribution of L_m	5	%	
Maximum peak drain current (I_{ds}^{peak}) =	0.551	A	
RMS drain current (I_{ds}^{rms}) =	0.18	A	
Maximum DC link voltage in CCM (V_{DC}^{CCM}) =	71	V	



-Switching frequency(fs): It follows the part you selected

-Ripple factor(K_{RF}): The ripple factor is defined by $K_{RF} = {}^{\Delta I}/_{2I_{EDC}}$, where Io is the maximum output current. For DCM operation, K_{RF}= 1 and for CCM operation K_{RF}< 1.

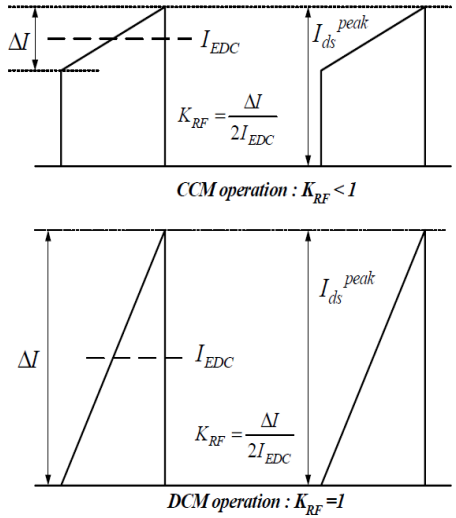
- When designing the flyback converter to operate in CCM, it is reasonable to set K_{RF} = 0.25 ~ 0.5 for the universal input range and K_{RF} = 0.4 ~ 0.8 for the European input range.

-Primary side inductance(Lm): Lm is obtained as $$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in} f_s K_{RF}}$$

-Maximum Drain peak current(I_{ds}^{peak}): $$I_{ds}^{peak} = I_{EDC} + \frac{\Delta I}{2} \quad where \quad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \quad \Delta I = \frac{V_{DC}^{min} D_{max}}{L_m f_s}$$

Determine transformer Primary Inductance (Lm) -2

4. Determine transformer primary inductance (Lm)			
Switching frequency of FSL5x8 (f_s)	100	kHz	
Ripple factor (K_{RF})	1		--->ok
Primary side inductance (L_m) =	743	uH	
Distribution of L_m	5	%	
Maximum peak drain current (I_{ds}^{peak}) =	0.551	A	
RMS drain current (I_{ds}^{rms}) =	0.18	A	
Maximum DC link voltage in CCM (V_{DC}^{CCM}) =	71	V	



-RMS drain current(I_{ds}^{rms}): $$I_{ds}^{rms} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{max}}{3}}$$

-Maximum DC link voltage in CCM(V_{DC}^{CCM}): $$V_{DC}^{CCM} = \left(\frac{1}{\sqrt{2L_m f_s P_{in}}} - \frac{1}{V_{RO}}\right)^{-1}$$

Maximum DC link voltage in CCM(V_{DC}^{CCM}): The maximum input voltage guaranteeing CCM in the full load condition.

Choose the proper part considering input power and peak drain current

5. Choose the proper FPS considering the input power and current limit							
Typical current limit of FSL5x8 (I_{LIM})	0.61	A					
Minimum I_{LIM} considering tolerance of 7%	0.567	A	>	0.551	I_{ds}^{peak}	A	
	->O.K.						

-Typical current limit of FSL5x8 (I_{LIM}): The current limit is defined by selected part

- Minimum I_{LIM} considering tolerance of 7%: checking MOSFET maximum peak current(I_{ds}^{peak}) is below current limit(I_{LIM}).

Part Number	Current Limit (A)
FSL518H	0.46
FSL538H	0.66
FSL518A	0.61
FSL538A	0.86

Determine the proper core and the minimum primary turns

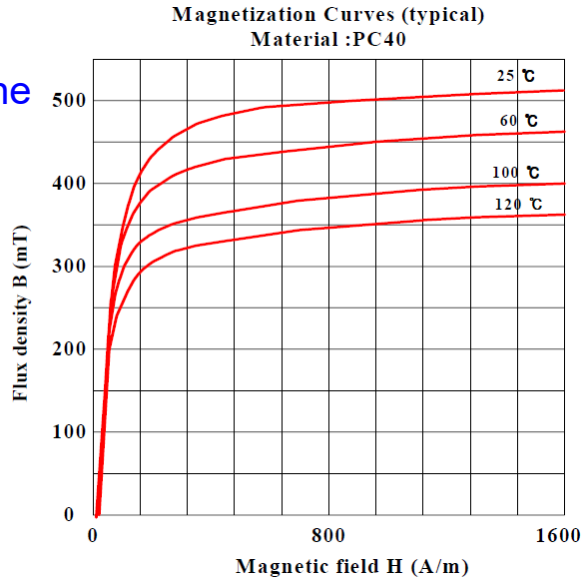
6. Determine the proper core and the minimum primary turns		
Maximum flux density (B_{max})	0.32	T
Cross sectional area of core (A_e)	23	mm^2
Minimum primary turns (N_p^{min})=	**69.1**	T

-Maximum flux density(B_{max}): B_{max} is the maximum flux density in tesla. Since the saturation flux density (B_{SAT}) decreases as the temperature goes high, the high temperature characteristics should be considered. Use B_{max}=0.3~0.35T.

- Refer the 100°C behavior in B-H characteristics curve, B_{SAT} is around 390mT. Recommended designing B_{max} between 0.3~0.35T to have enough margin for avoiding saturation.

-Cross sectional area of core(Ae): refer the manufacture core data book

- Minimum primary turns(N_p^{min}): $N_P{}^{min} = \frac{L_m I_{LIM}}{B_{sat} A_e} \times 10^6$ (turns)



Typical B-H characteristics of ferrite core (TDK/PC40)

Determine the number of turns for each output - 1

7. Determine the number of turns for each output

	$V_{o(n)}$		$V_{F(n)}$				# of turns	
Vcc (Use Vcc start voltage)	11	V	1.3	V	10.9	=>	11	T
1st output for feedback	12	V	0.4	V	11	=>	11	T
2nd output	0	V	0	V	0.0	=>	0	T
3rd output	0	V	0	V	0.0	=>	0	T
4th output	0	V	0	V	0.0	=>	0	T
5th output	0	V	0	V	0.0	=>	0	T
6th output	0	V	0	V	0.0	=>	0	T
VF : Forward voltage drop of rectifier diode			Primary turns (N_p)=				71	T
			--->enough turns					
Ungapped AL value (AL)	1140	nH/T^2						
Gap length (G) ; center pole gap =	0.170603265	mm						

-In V_{RO} parameter, we determine the turn ratio(n) from V_{RO}= Vo(Np/Ns) where Np/Ns=n.

-Input Ns to satisfy the Np>Np^{min} (→enough turns).

-V_F(n): Rectifier diode forward voltage on each output.

- Vcc(Use Vcc start voltage): input determine Vcc voltage and forward voltage of auxiliary winding rectifier diode. Then get the Na of auxiliary winding turns.

-1st output for feedback: input the forward voltage of rectifier diode and turns.

$$n = \frac{N_P}{N_{S1}} = \frac{V_{R0}}{V_{o1} + V_{F1}} \qquad N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \qquad N_a = \frac{V_{cc}^{*} + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1}$$

Determine the number of turns for each output - 2

7. Determine the number of turns for each output

	$V_{o(n)}$		$V_{F(n)}$				# of turns	
Vcc (Use Vcc start voltage)	11	V	1.3	V	10.9	=>	11	T
1st output for feedback	12	V	0.4	V	11	=>	11	T
2nd output	0	V	0	V	0.0	=>	0	T
3rd output	0	V	0	V	0.0	=>	0	T
4th output	0	V	0	V	0.0	=>	0	T
5th output	0	V	0	V	0.0	=>	0	T
6th output	0	V	0	V	0.0	=>	0	T
VF : Forward voltage drop of rectifier diode			Primary turns (N_p)=				71	T
			--->enough turns					
Ungapped AL value (AL)	1140	nH/T^2						
Gap length (G) ; center pole gap =	0.170603265	mm						

-Primary turns(Np): Primary turns recommended (the number of) primary winding turns at least.

- When $\frac{V_{RO}}{V_o+V_F} \times N_S > N_{Pmin}$, enough turns is showed.

-Un-gapped A_L value(A_L): refer the manufacture core data book

-Gap length(G); center pole gap: calculated core gap length for transformer production, where A_L is the A_L-value with no gap in nH/turns^2. A_e is the cross sectional area of the core. L_m and N_p are obtained previously.

$$G = 40\pi A_e\left(\frac{N_P{}^2}{1000L_m} - \frac{1}{A_L}\right)$$

Determine the wire diameter for each winding

8. Determine the wire diameter for each winding

	Diameter		Strand		$I_{D(n)}^{rms}$		(A/mm²)
Primary winding	0.22	mm	1	T	0.184	A	4.85
Vcc winding	0.18	mm	1	T	0.005	A	0.22
1st output winding	0.5	mm	2	T	1.471	A	3.7
2nd output winding	0	mm	0	T	#DIV/0!	A	#DIV/0!
3rd output winding	0	mm	0	T	#DIV/0!	A	#DIV/0!
4th output winding	0	mm	0	T	#DIV/0!	A	#DIV/0!
5th output winding	0	mm	0	T	#DIV/0!	A	#DIV/0!
6th output winding	0	mm	0	T	#DIV/0!	A	#DIV/0!

-Input the wire diameter to check current density, typically less than **6-10A/mm²** is accept.

-Strand: input how many wires do you want to winding in each output.

-For higher output current, using parallel windings with multiple strands of thinner wire to minimize skin effect.

Judgment proper core size

Actual window area of core (A_w)	39.85	mm^2	
Copper area (A_c) =	7.29	mm^2	
Fill factor (K_F)	0.2		
Required window area (A_{wr})	36.47	mm^2	->O.K.

-Required window area(A_{wr}) < Actual window area of core(A_w): Check the winding window area(A_w) is enough to accommodate the wires.

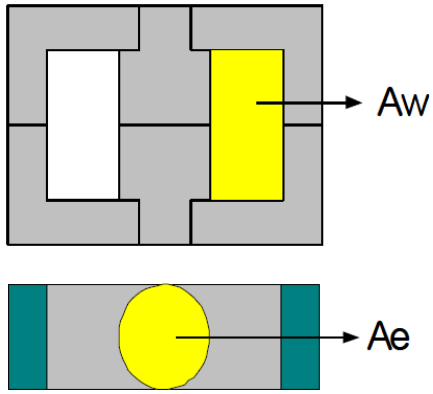
-A_w: Winding window area (mm^2), refer core dimension to calculate it.

-A_c: Copper area (mm^2), calculate all copper wire diameter

-Fill factor(K_F): K_F is the fill factor.

-typically is **0.2~0.25 for single output**, **0.15~0.2 for multiple outputs**.

-A_{wr}: calculation result base-on selected copper wire, turns and strand numbers.



Choose the rectifier diode in the secondary side

9. Choose the rectifier diode in the secondary side

	$V_{D(n)}$		$I_{D(n)}^{rms}$	
Vcc diode	89	V	0.008	A
1st output diode	91	V	2.207	A
2nd output diode	0	V		A
3rd output diode	0	V		A
4th output diode	0	V		A
5th output diode	0	V		A
6th output diode	0	V		A

- Vcc diode: Auxiliary winding diode is determined $V_{D(n)} = V_{o(n)} + \frac{V_{DC}^{max} \cdot (V_{o(n)} + V_{F(n)})}{V_{RO}}$

-1st output diode: output rectifier diode voltage rating is determined with

- output rectifier diode current rating is determined with $I_{D(n)}^{rms} = I_{ds}^{rms} \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{RO} K_{L(n)}}{(V_{o(n)} + V_{F(n)})}$

where K_L is $K_{L(n)} = \frac{P_{o(n)}}{P_o}$ $P_{o(n)}$ is the n-th output power and P_o is output power.

-The typical voltage and current margins for rectifier diode is $V_{RRM} > 1.3 * V_{D(n)}$, $I_F > 1.5 * I_{D(n)}^{rms}$

Determine the output capacitor

10. Determine the output capacitor								
	$C_{o(n)}$		$R_{C(n)}$		$I_{cap(n)}$		$\Delta V_{o(n)}$	
1st output capacitor	1000	uF	250	mΩ	1.310	A	0.891	V
2nd output capacitor		uF		mΩ		A		V
3rd output capacitor		uF		mΩ		A		V
4th output capacitor		uF		mΩ		A		V
5th output capacitor		uF		mΩ		A		V
6th output capacitor		uF		mΩ		A		V

-output capacitor($C_{o(n)}$) is obtained: $$I_{cap(n)}^{\ rms} = \sqrt{(I_{D(n)}^{\ rms})^2 - I_{o(n)}^{\ 2}}$$

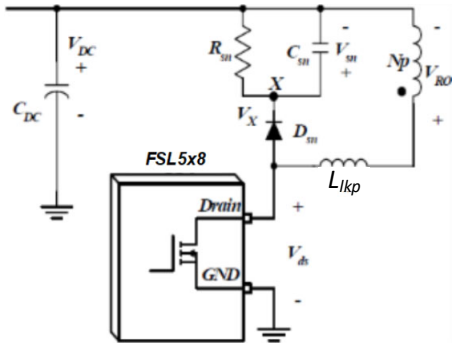
where Io(n) is the load current of n-th output and ID(n)rms is obtained on last page.

-The voltage ripple on the n-th output is $$\Delta V_{o(n)} = \frac{I_{o(n)} D_{max}}{C_{o(n)} f_s} + \frac{I_{ds}^{\ peak} V_{RO} R_{C(n)} K_{L(n)}}{(V_{o(n)} + V_{F(n)})}$$

where $C_{o(n)}$ is the capacitance, $R_{c(n)}$ is the effective series resistance(ESR)

Design RCD snubber for primary side

11. Design RCD snubber for primary side Drain			
Primary side leakage inductance (L_{lkp})	15	uH	
Maximum Voltage of snubber capacitor (V_{sn})	200	V	O.K
Maximum snubber capacitor voltage ripple	10	%	
Snubber resistor (R_{sn})=	105.5	KΩ	
Snubber capacitor (C_{sn})=	0.9	nF	
Power loss in snubber resistor (P_{sn})=	0.4	W	
Peak drain current at V_{DC}^{max} (I_{ds2}) =	0.51	A	DCM operation at Vlinemax
Max Voltage of Csn at V_{DC}^{max} (V_{sn2})=	188	V	
Max Voltage stress of MOSFET (V_{ds}^{max})=	562	V	



-Primary side leakage inductance(L_{lkp}): input the measurement leakage inductance

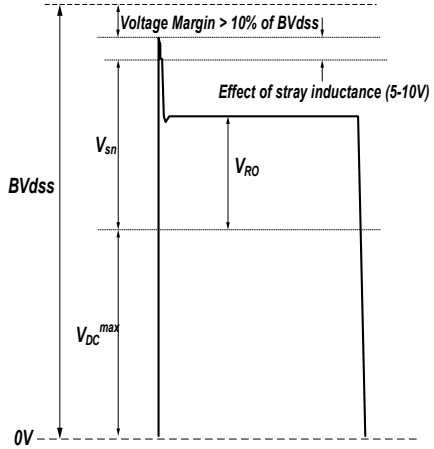
-Maximum voltage of snubber capacitor(Vsn): 2~2.5 times of V_{RO}

-Maximum snubber capacitor voltage ripple: 5~10% is reasonable

-Snubber resistor(R_{sn}): V_{sn}^2 / P_{sn}

where $P_{sn} = \frac{(V_{sn})^2}{R_{sn}} = \frac{1}{2} f_s L_{lK} (I_{ds}^{peak})^2 \frac{V_{sn}}{V_{sn} - V_{RO}}$

$V_{sn2} = \frac{V_{RO} + \sqrt{(V_{RO})^2 + 2R_{sn}L_{lk}f_s(I_{ds2})^2}}{2}$



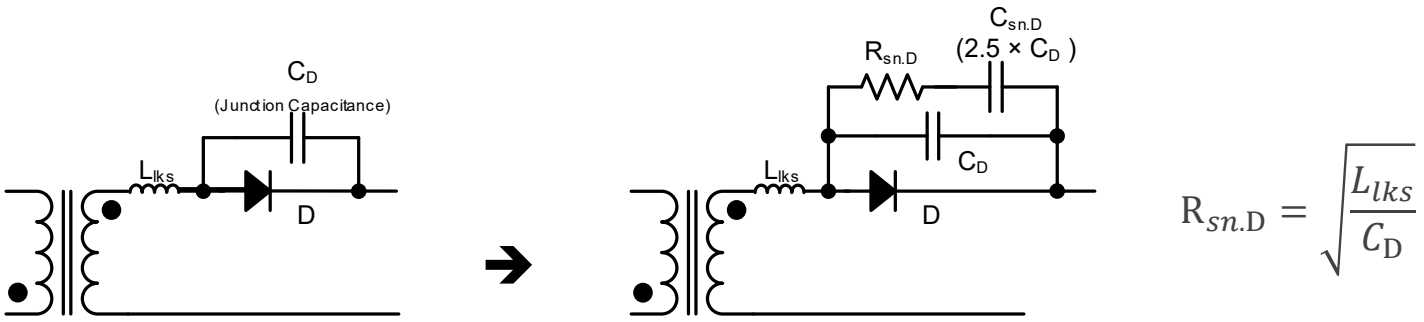
Design snubber for secondary side

12. Design snubber for Output Diode

	L_{lks}		C_D		$R_{sn.D}$		$C_{sn.D}$	
Snubber for 1st output diode	1	uH	60	pF	129	Ω	150	pF
Snubber for 2nd output diode		uH		pF		Ω	0	pF
Snubber for 3rd output diode		uH		pF		Ω	0	pF
Snubber for 4th output diode		uH		pF		Ω	0	pF
Snubber for 5th output diode		uH		pF		Ω	0	pF
Snubber for 6th output diode		uH		pF		Ω	0	pF

-Snubber for 1st output diode: input leakage inductance of secondary winding and rectifier diode junction capacitance.

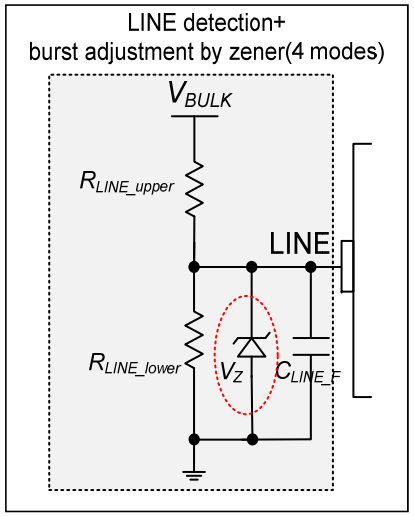
- Calculate $R_{sn.D}$ and $C_{sn.D}$ for secondary side rectifier diode snubber.



$$R_{sn.D} = \sqrt{\frac{L_{lks}}{C_D}}$$

Burst threshold adjustment - Enable LINE Detection

13. Burst threshold adjustment			
Choose LINE pin connection type(A or B)	A		->Burst threshold voltage setting by zener diode
Target of threshold Voltage for Entering Burst Mode(V_{BURL})	0.6	V	->Please set 0.4,0.5, or 0.6
External component connection for type A(V_Z)	7.50	V	
External component connection for type B(R_{BURST})	N/A	KΩ	
Target of threshold Voltage for leaving Burst Mode(V_{BURH})	0.70	V	
Minimum peak drain current of each switching	0.153	A	
Burst-mode Entering Power	0.216	W	



	Line Detection Enable/Disable	V_{LINE} (V)	V_{BURH}/V_{BURL}(V)
Architecture A	**Enable**	12.4 V < V_Z	0.5/0.4
		9.3 V < V_Z < 10.6 V	0.6/0.5
		V_Z < 7.9 V	0.7/0.6

-Choose LINE pin connection type(A or B):

A: Enable LINE detection

B: Disable LINE detection

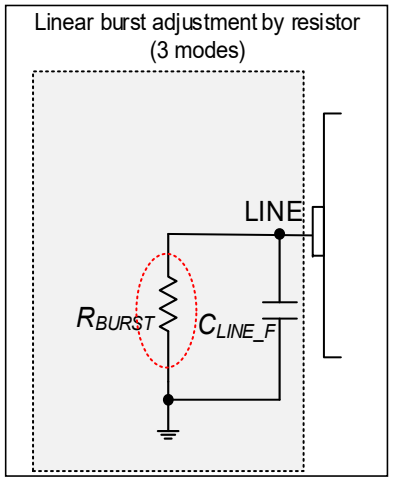
-Target of threshold voltage for entering Burst Mode(V_{BURL}): setting with 0.4V, 0.5V or 0.6V

-External Component(Zener diode) connection for type A: setting zener Vz

Burst threshold adjustment – Disable Line Detection

13. Burst threshold adjustment			
Choose LINE pin connection type(A or B)	A		->Burst threshold voltage setting by zener diode
Target of threshold Voltage for Entering Burst Mode(V_{BURL})	0.6	V	->Please set 0.4,0.5, or 0.6
External component connection for type A(V_Z)	7.50	V	
External component connection for type B(R_{BURST})	N/A	KΩ	
Target of threshold Voltage for leaving Burst Mode(V_{BURH})	0.70	V	
Minimum peak drain current of each switching	0.153	A	
Burst-mode Entering Power	0.216	W	

	Line Detection Enable/Disable	V_{LINE} (V)	V_{BURH}/V_{BURL}(V)
Architecture B	Disable	0.9 V< I_{BURST}× R_{BURST} <1.2 V	0.5/0.4
		1.2 V < I_{BURST}× R_{BURST} <3.6 V	$A_{V\text{-}BURST}$× (I_{BURST}× R_{BURST})+0.1 /$A_{V\text{-}BURST}$× (I_{BURST}× R_{BURST})



-Choose LINE pin connection type(A or B):

A: Enable LINE detection

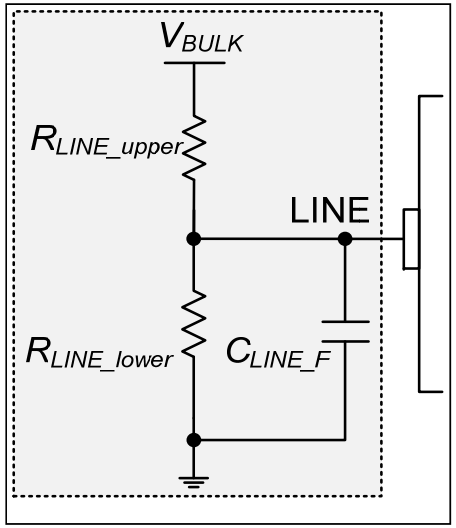
B: Disable LINE detection

- External component connection for type B: setting R_{BURST}
- Minimum peak drain current of each switching:
- Burst-mode entering power:

$$P_{in.burst} = \frac{1}{2} L \cdot \left(\frac{V_{BURL}}{4 \cdot 0.6} I_{LIM} \right)^2 \cdot f(V_{BURL})$$

Line detection setting

14. LINE detection(Brown in/out, line OVP)		
Target of brown out AC voltage($V_{AC-BO\,tar}$)	66	Vac
Brown-out (BO) threshold voltage on LINE Pin($V_{LINE-BO}$)	0.85	V
Brown-in (BI) threshold voltage on LINE Pin($V_{LINE-BI}$)	1.00	V
Line OVP threshold voltage on LINE Pin($V_{LINE-OVP}$)	4.50	V
Selected upper side resistor (R_{LINE_upper})	22	MΩ
Recommended LINE pin lower side resistor($R_{LINE\_lower.rec}$)	202.2	KΩ
Selected lower side resistor (R_{LINE_lower})	200	KΩ
Recommended minimum LINE pin filter capacitor(C_{LINE_F})	0.803	nF
Brown in AC voltge level(V_{AC-BI})	78	Vac
Brown out AC voltge level(V_{AC-BO})	67	Vac
Line OVP AC voltge level($V_{AC-LOVP}$)	353	Vac
Maximum power loss on LINE sense resistors	6.3	mW



-Target of brown-out AC voltage($V_{AC-BO\,tar}$): input design target of brown-out voltage.

-Selected upper side resistor(R_{LINE_upper}): input upper divide resistor

-Recommended minimum LINE pin filter capacitor(C_{LINE_F}): at least using 1nF to avoid interference on LINE pin.

-Maximum power loss on LINE sense resistors: Divide resistor power consumption on LINE pin.

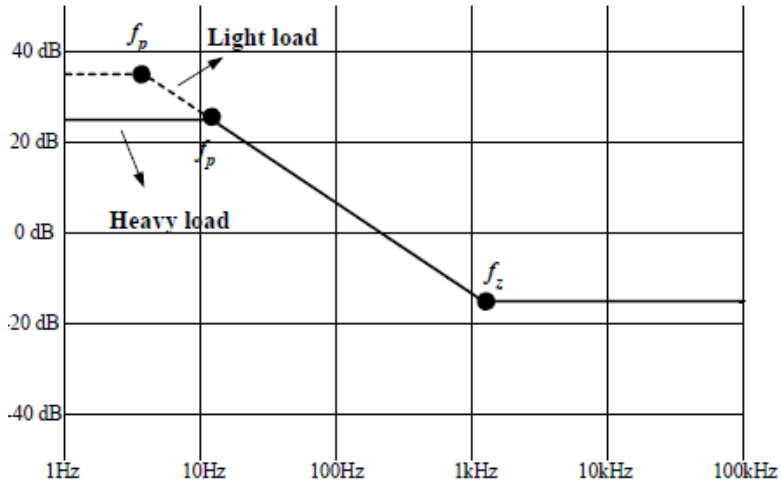
Please select these dividing resistors upto 20Mega Ohm due to power loss of LINE sense resistors consideration.

Design feedback control loop(Isolation) - 1

15. Design Feedback control loop (Isolation)						
Operation mode =	DCM					
Control-to-output DC gain =	6					
Control-to-output zero (w_z) =	4000	rad/s =>	f_z=	637	Hz	
Control-to-output RHP zero (w_{rz})=	##########	rad/s =>	f_{rz}=	##########	Hz	
Control-to-output pole (w_p)=	112	rad/s =>	f_p=	18	Hz	

-Determine the crossover frequency (fc). For CCM mode, set fc below 1/3 of right half plane zero to minimize the effect if the RHP zero. For DCM mode, fc can be placed at higher frequency, since there is no RHP zero.

-When add LC filter, the crossover frequency should be placed below 1/3 of corner frequency of the LC filter.



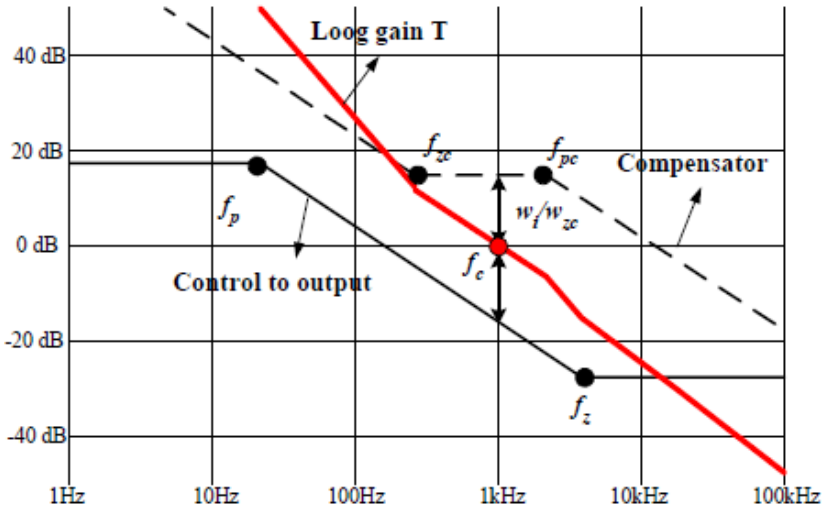
Design feedback control loop(Isolation) - 2

15. Design Feedback control loop (Isolation)							
Operation mode =	DCM						
Control-to-output DC gain =	6						
Control-to-output zero (w_z) =	4000	rad/s =>	f_z=	637	Hz		
Control-to-output RHP zero (w_{rz})=	###########	rad/s =>	f_{rz}=	###########	Hz		
Control-to-output pole (w_p)=	112	rad/s =>	f_p=	18	Hz		

-Determine DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at fc

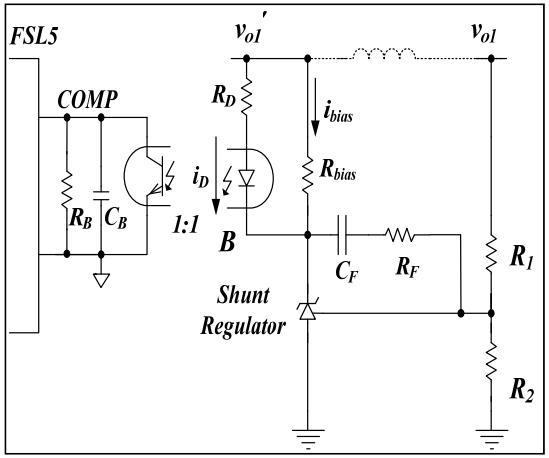
-Place a compensator zero(f_{zc}) around fc/3.

-Place a compensator pole(f_{pc}) above 3fc



Design feedback control loop(Isolation) - 3

15. Design Feedback control loop (Isolation)							
Voltage divider resistor (R_1)	180.0	KΩ					
Voltage divider resistor (R_2)=	47.4	KΩ					
Opto coupler diode resistor (R_D)	5.1	KΩ					
KA431 Bias resistor (R_{bias})	5.1	KΩ					
COMP pin capacitor (C_B)	1	nF					
COMP pin resistor (R_B)	100	KΩ					
Feedback Capacitor (C_F)	6.8	nF					
Feedback resistor (R_F)	1000	KΩ					
Feedback integrator gain (w_I) =	15997	rad/s =>	f_I=	2,547	Hz		
Compensator zero (w_{zc})=	125	rad/s =>	f_{zc}=	20	Hz		
Compensator pole (w_{pc})=	10014	rad/s =>	f_{pc}=	1,595	Hz		



-For CCM operation, the control-to-output transfer function of flyback is:

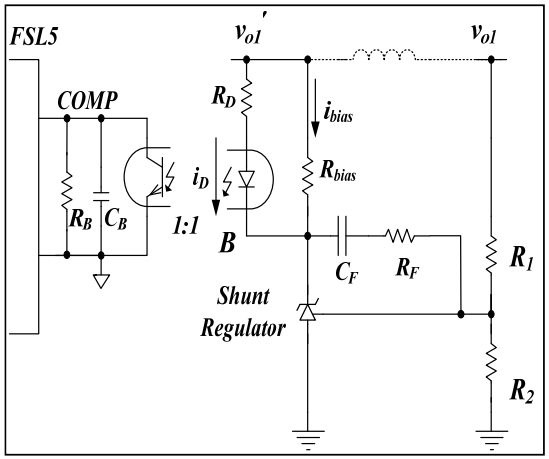
$$G_{VC} = \frac{\hat{V}_{O1}}{\hat{V}_{COMP}} = \frac{K \times R_L \times V_{DC}\left({}^{N_P}/_{N_{S1}}\right)}{2V_{RO} + \mathrm{V_{DC}}} \cdot \frac{\left(1 + {}^{S}/_{W_Z}\right)\left(1 - {}^{S}/_{W_{rz}}\right)}{1 + {}^{S}/_{W_P}}$$

$$W_Z = \frac{1}{R_{C1}C_{O1}} \qquad W_{rz} = \frac{R_L(1-D^2)}{DL_m\left({}^{N_{S1}}/_{N_P}\right)^2} \qquad W_P = \frac{(1+D)}{R_L C_{O1}}$$

- R_B selection range is recommended from 60 kΩ~100 kΩ.

Design feedback control loop(Isolation) - 4

15. Design Feedback control loop (Isolation)						
Voltage divider resistor (R_1)	180.0	KΩ				
Voltage divider resistor (R_2)=	47.4	KΩ				
Opto coupler diode resistor (R_D)	5.1	KΩ				
KA431 Bias resistor (R_{bias})	5.1	KΩ				
COMP pin capacitor (C_B)	1	nF				
COMP pin resistor (R_B)	100	KΩ				
Feedback Capacitor (C_F)	6.8	nF				
Feedback resistor (R_F)	1000	KΩ				
Feedback integrator gain (w_i) =	15997	rad/s =>	f_i=	2,547	Hz	
Compensator zero (w_{zc})=	125	rad/s =>	f_{zc}=	20	Hz	
Compensator pole (w_{pc})=	10014	rad/s =>	f_{pc}=	1,595	Hz	



-For DCM operation, the control-to-output transfer function of flyback is:

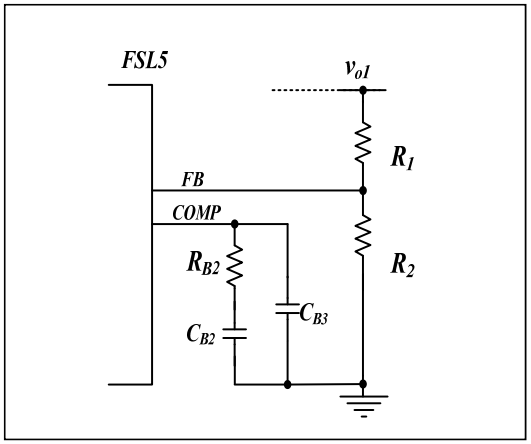
$$G_{VC} = \frac{\hat{V}_{O1}}{\hat{V}_{COMP}} = \frac{V_{O1}}{V_{COMP}} \cdot \frac{\left(1 + {}^{S}/_{W_Z}\right)}{\left(1 + {}^{S}/_{W_P}\right)} \quad \text{where} \quad W_Z = \frac{1}{R_{C1}C_{O1}} \quad W_P = \frac{2}{R_L C_{O1}}$$

- The feedback compensation network transfer function is:

$$\frac{\hat{V}_{COMP}}{\hat{V}_{O1}} = -\frac{W_i}{S} \cdot \frac{\left(1 + {}^{S}/_{W_{ZC}}\right)}{\left(1 + {}^{S}/_{W_P}\right)} \quad \text{where} \quad W_i = \frac{R_B}{R_1 R_D C_{O1}} \quad W_{zc} = \frac{R_L(1-D^2)}{(R_F + R_1)C_F} \quad W_{PC} = \frac{1}{R_B C_B}$$

Design feedback control loop(non-Isolation)

16. Design Feedback control loop (Non-Isolation)						
COMP pin capacitor (C_{B2})	22	nF				
COMP pin resistor (R_{B2})	360	KΩ				
COMP pin capacitor (C_{B3})	0.47	nF				
Feedback integrator gain (w_{i2}) =	2781	rad/s =>	f_{i2}=	443	Hz	
Compensator zero (w_{zc2})=	126	rad/s =>	f_{zc2}=	20	Hz	
Compensator pole (w_{pc2})=	6036	rad/s =>	f_{pc2}=	961	Hz	



-The feedback compensation network transfer function is:

$$\frac{\hat{V}_{COMP}}{\hat{V}_{O1}} = -\frac{W_i}{S} \cdot \frac{\left(1 + {}^{S}/_{W_{ZC}}\right)}{\left(1 + {}^{S}/_{W_{PC}}\right)}$$

Where $w_{i2}= (G_M*R_1/(R_1+R_2)) / (C_{B2}+C_{B3}) *10^3$

$w_{zc2}= 1 / (C_{B2}+R_{B3}) *10^6$

$w_{pc2}= (1/R_{B2})*(1/C_{B2}+1/C_{B3}) *10^6$