

固定/可変電流制限付き パワー・スイッチ

NCP380, NCV380

NCP380は、大容量負荷や短絡が発生しやすいアプリケーション向けに設計されたハイサイドパワー・スイッチです。このデバイスには、55 mΩ (DFNパッケージ)のPチャネルMOSFETを集積しています。出力負荷が電流制限スレッシュホールドを超えるか、短絡が発生した場合、デバイスは定電流安定化モードに切り替わって出力電流を目的のレベルに制限します。電流制限スレッシュホールドは、外部抵抗で500 mA ~ 2.1 Aの範囲でユーザが調整可能とするかまたは内部固定とするかを選択できます。パワー・スイッチの立ち上がり時間と立ち下がり時間を制御することによって、スイッチング中の電流リングを抑えます。

出力電圧が入力電圧を超えた場合、スイッチの入力側のデバイスを保護するために、内部逆電圧検出コンパレータがパワー・スイッチをディセーブルします。

過電流、逆電圧、または過熱状態が発生している間、**FLAG**ロジック出力はローにアサートされます。スイッチはロジック・イネーブル入力をアクティブ・ハイまたはローにすることによって制御されます。

特長

- 2.5 V ~ 5.5 Vの動作範囲
- 70 mΩのハイサイドMOSFET
- 電流制限：
 - ◆ 500 mA ~ 2.1 Aの範囲でユーザが調整可能
 - ◆ 固定500 mA、1 A、1.5 A、2 A、2.1 A
- 低電圧ロックアウト(UVLO)
- ソフトスタート機能内蔵
- サーマル保護
- ソフト・ターンオフ
- 逆電圧保護
- 接合部温度範囲：-40°C ~ 125°C
- アクティブ・ハイまたはローのイネーブル(ENまたは \overline{EN})
- IEC61000-4-2(レベル4)に準拠
 - ◆ 8.0 kV (接触放電)
 - ◆ 15 kV (気中放電)
- UL マーク E343275認定済み
- 車載向け、および場所と制御の変更を必要とする他のアプリケーション向けNCVプリフィックス
- 鉛フリー・パッケージを提供

代表的アプリケーション

- ラップトップPC
- USBポート/ハブ
- TV



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UDFN6
CASE 517AB



TSOP-5
CASE 483

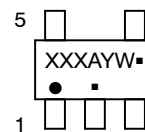


TSOP-6
CASE 318G

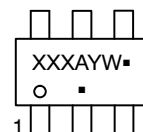
MARKING DIAGRAMS



UDFN6



TSOP-5



TSOP-6

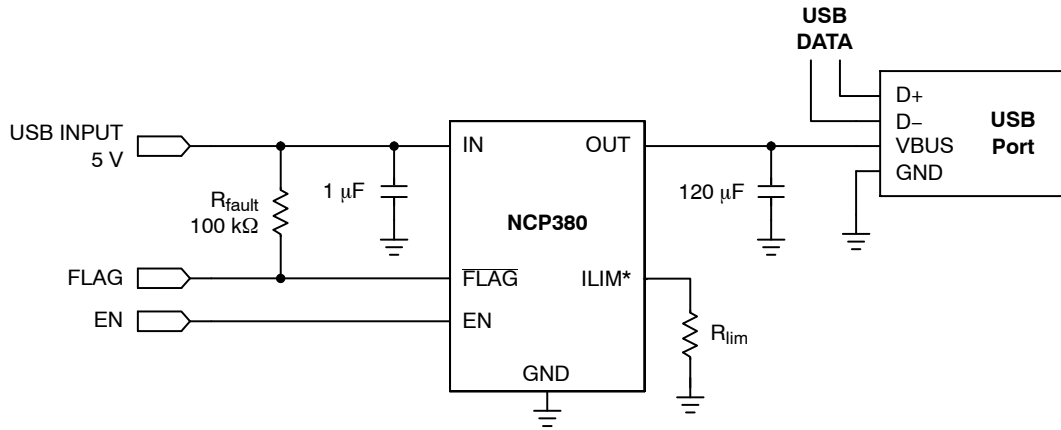
XXX = Specific Device Code
A = Assembly Location
M = Date Code
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

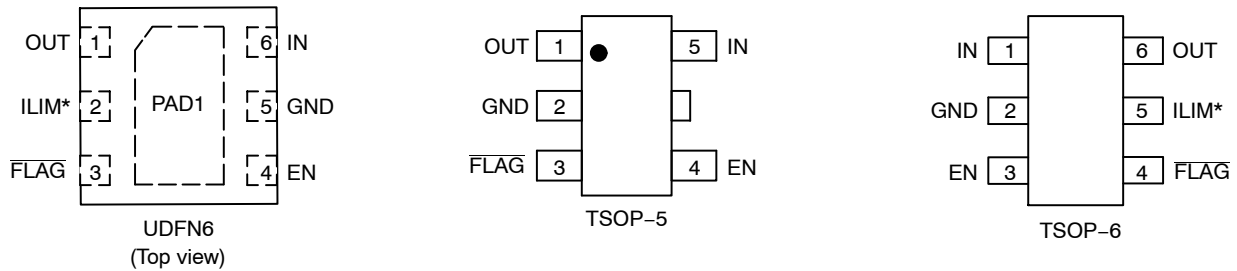
See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

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*For Adjustable Version Only.

Figure 1. Typical Application Circuit



*For adjustable version only, otherwise not connected.

Figure 2. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Type	Description
EN	INPUT	Enable input, logic low/high (i.e. \overline{EN} or EN) turns on power switch
GND	POWER	Ground connection;
IN	POWER	Power-switch input voltage; connect a 1 μ F or greater ceramic capacitor from IN to GND as close as possible to the IC.
FLAG	OUTPUT	Active-low open-drain output, asserted during overcurrent, overtemperature or reverse-voltage conditions. Connect a 10 k Ω or greater resistor pull-up, otherwise leave unconnected.
OUT	OUTPUT	Power-switch output; connect a 1 μ F ceramic capacitor from OUT to GND as close as possible to the IC is recommended. A 1 μ F or greater ceramic capacitor from OUT to GND must be connected if the USB requirement (i.e. 120 μ F capacitor minimum) is not met.
ILIM*	INPUT	External resistor used to set current-limit threshold; recommended $5 \text{ k}\Omega < R_{ILIM} < 250 \text{ k}\Omega$.
PAD1**	THERMAL	Exposed Thermal Pad: Must be soldered to PCB Ground plane

*(For adjustable version only, otherwise not connected.

**For DFN version only.

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Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
From IN to OUT Pins: Input/Output (Note 1)	V_{IN}, V_{OUT}	-7.0 to +7.0	V
IN, OUT, EN, ILIM, FLAG, Pins: Input/Output (Note 1)	$V_{EN}, V_{ILIM}, V_{FLAG}, V_{IN}, V_{OUT}$	-0.3 to +7.0	V
FLAG Sink Current	I_{SINK}	1	mA
I_{LIM} Source Current	I_{LIM}	1	mA
ESD Withstand Voltage (IEC 61000-4-2) (Output Only, when Bypassed with 1.0 μ F Capacitor Minimum)	ESD IEC	15 Air, 8 Contact	kV
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2,000	V
Machine Model (MM) ESD Rating (Notes 2 and 3)	ESD MM	200	V
Latch-up Protection (Note 4) Pins IN, OUT, EN, ILIM, FLAG	LU	100	mA
Maximum Junction Temperature Range (Note 6)	T_J	-40 to +TSD	$^{\circ}$ C
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}$ C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

(参考訳)

最大定格を超えるストレスは、デバイスにダメージを与える危険性があります。これらの定格値を超えた場合は、デバイスの機能性を損ない、ダメージが生じたり、信頼性に影響を及ぼす危険性があります。

- According to JEDEC standard JESD22-A108.
- This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ± 2.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) ± 200 V per JEDEC standard: JESD22-A115 for all pins.
- Except EN pin, 150 V.
- Latch up Current Maximum Rating: ± 100 mA per JEDEC standard: JESD78 class II.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
- A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		2.5	-	5.5	V
V_{EN}	Enable Voltage		0	-	5.5	
T_A	Ambient Temperature Range		-40	25	+85	$^{\circ}$ C
T_J	Junction Temperature Range		-40	25	+125	$^{\circ}$ C
R_{ILIM}	Resistor from ILIM to GND Pin		5.0	-	250	k Ω
I_{SINK}	FLAG Sink Current		-	-	1.0	mA
C_{IN}	Decoupling Input Capacitor		1.0	-	-	μ F
C_{OUT}	Decoupling Output Capacitor	USB Port per Hub	120	-	-	μ F
$R_{\theta JA}$	Thermal Resistance Junction-to-Air	UDFN-6 Package (Notes 7 and 8)	-	120	-	$^{\circ}$ C/W
		TSOP-5 Package (Notes 7 and 8)	-	305	-	$^{\circ}$ C/W
		TSOP-6 Package (Notes 7 and 8)	-	280	-	$^{\circ}$ C/W
I_{OUT}	Maximum DC Current	UDFN-6 Package	-	-	2.1	A
		TSOP-5, TSOP-6 Package	-	-	1.0	A
P_D	Power Dissipation Rating (Note 9)	$T_A \leq 25^{\circ}$ C				
		UDFN-6 Package	-	830	-	mW
		TSOP-5 Package	-	325	-	mW
		TSOP-6 Package	-	350	-	mW
		$T_A = 85^{\circ}$ C				
		UDFN-6 Package	-	325	-	mW
		TSOP-5 Package	-	130	-	mW
		TSOP-6 Package	-	145	-	mW

- A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
- The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2" \times 2" NCP380EVB board. It is a 2 layers board with 2-ounce copper traces on top and bottom of the board. Exposed pad is connected to ground plane for UDFN-6 version only.
- The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

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Table 4. ELECTRICAL CHARACTERISTICS

(Min & Max Limits apply for T_A between -40°C to $+85^\circ\text{C}$ and T_J up to $+125^\circ\text{C}$ for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^\circ\text{C}$ and $V_{IN} = 5\text{ V}$.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
POWER SWITCH								
$R_{DS(on)}$	Static Drain-source On-state Resistance	DFN Package	$V_{IN} = 5\text{ V}$	$-40^\circ\text{C} < T_J < 125^\circ\text{C}$	–	55	75	$\text{m}\Omega$
			$2.5\text{ V} < V_{IN} < 5.5\text{ V}$	$-40^\circ\text{C} < T_J < 125^\circ\text{C}$	–	–	110	
	TSOP Package		$V_{IN} = 5\text{ V}$	$-40^\circ\text{C} < T_J < 125^\circ\text{C}$	–	70	95	$\text{m}\Omega$
			$2.5\text{ V} < V_{IN} < 5.5\text{ V}$	$-40^\circ\text{C} < T_J < 125^\circ\text{C}$	–	–	135	
T_R	Output Rise Time	$C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 100\ \Omega$ (Note 10)	$V_{IN} = 5\text{ V}$	0.3	1.0	1.5	ms	
			$V_{IN} = 2.5\text{ V}$	0.2	0.65	1.0		
T_F	Output Fall Time		$V_{IN} = 5\text{ V}$	0.1	–	0.5		
			$V_{IN} = 2.5\text{ V}$	0.1	–	0.5		
ENABLE INPUT EN OR $\overline{\text{EN}}$								
V_{IH}	High-level Input Voltage		1.2	–	–	V		
V_{IL}	Low-level Input Voltage		–	–	0.4	V		
I_{EN}	Input Current	$V_{EN} = 0\text{ V}$, $\overline{V_{EN}} = 5\text{ V}$	–0.5	–	0.5	μA		
T_{ON}	Turn On Time	$C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 100\ \Omega$ (Note 11)	2.0	3.0	4.0	ms		
T_{OFF}	Turn Off Time		1.0	–	3.0	ms		
CURRENT LIMIT								
I_{OCP}	Current-limit Threshold (Maximum DC Output Current I_{OUT} Delivered to Load)	$V_{IN} = 5\text{ V}$	$R_{ILIM} = 20\ \text{k}\Omega$ (Note 11)	1.02	1.20	1.38	A	
			$R_{ILIM} = 40\ \text{k}\Omega$ (Notes 11 and 13)	0.595	0.700	0.805		
			Fixed 0.5 A (Note 12)	0.5	0.58	0.65		A
			Fixed 1.0 A (Note 12)	1.0	1.15	1.3		
			Fixed 1.5 A (Note 12)	1.5	1.75	1.9		
			Fixed 2.0 A (Note 12)	2.0	2.25	2.5		
			Fixed 2.1 A (Note 12)	2.1	2.25	2.5		
T_{DET}	Response Time to Short Circuit	$V_{IN} = 5\text{ V}$	–	2.0	–	μs		
T_{REG}	Regulation Time		1.8	3.0	4.0	ms		
T_{OCP}	Overcurrent Protection Time		14	20	26	ms		
REVERSE-VOLTAGE PROTECTION								
V_{REV}	Reverse-voltage Comparator Trip Point ($V_{OUT} - V_{IN}$)		–	100	–	mV		
T_{REV}	Time from Reverse-voltage Condition to MOSFET Switch Off & FLAG Low	$V_{IN} = 5\text{ V}$	4.0	6.0	9.0	ms		
T_{RREV}	Re-arming Time		7.0	10	15	ms		
UNDERVOLTAGE LOCKOUT								
V_{UVLO}	IN Pin Low-level Input Voltage	V_{IN} Rising	2.0	2.3	2.4	V		
V_{HYST}	IN Pin Hysteresis	$T_J = 25^\circ\text{C}$	25	–	60	mV		
T_{RUVLO}	Re-arming Time		7.0	10	15	ms		
SUPPLY CURRENT								
I_{NOFF}	Low-level Output Supply Current	$V_{IN} = 5\text{ V}$, No Load on OUT, Device OFF $V_{EN} = 0\text{ V}$ or $\overline{V_{EN}} = 5\text{ V}$	–	1.0	2.1	μA		
I_{INON}	High-level Output Supply Current	$V_{IN} = 5\text{ V}$, Device Enable 2 A and 2.1 A Versions 1 A and 1.5 A Current Versions 0.5 A Current Version	–	–	90	μA		
			–	–	80			
			–	–	70			
I_{REV}	Reverse Leakage Current	$V_{OUT} = 5\text{ V}$, $V_{IN} = 0\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1.0	μA	

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Table 4. ELECTRICAL CHARACTERISTICS (continued)

(Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ and T_J up to $+125^{\circ}\text{C}$ for V_{IN} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{IN} = 5 \text{ V}$.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FLAG PIN						
V_{OL}	FLAG Output Low Voltage	$I_{FLAG} = 1 \text{ mA}$			400	mV
I_{LEAK}	Off-state Leakage	$V_{FLAG} = 5 \text{ V}$			1.0	μA
T_{FLG}	FLAG Deglitch	FLAG De-assertion Time due to Overcurrent or Reverse Voltage Condition	4.0	6.0	9.0	ms
T_{FOCP}	FLAG Deglitch	FLAG Assertion due to Overcurrent	6.0	8.0	12	ms

THERMAL SHUTDOWN

T_{SD}	Thermal Shutdown Threshold			140		$^{\circ}\text{C}$
T_{SDOCP}	Thermal Regulation Threshold			125		$^{\circ}\text{C}$
T_{RSD}	Thermal Shutdown Rearming Threshold			115		$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(参考訳)

製品パラメータは、特別な記述が無い限り、記載されたテスト条件に対する電気的特性で示しています。異なる条件下で製品動作を行った時には、電気的特性で示している特性を得られない場合があります。

10. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground, See Figure 3.

11. Adjustable current version, R_{LIM} tolerance $\pm 1\%$.

12. Fixed current version.

13. Not production test, guaranteed by characterization.

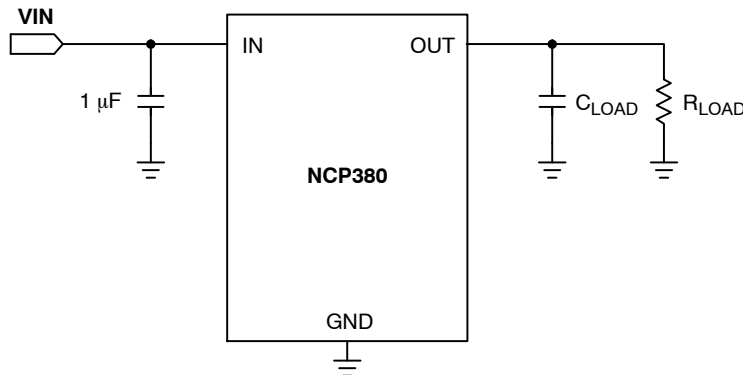


Figure 3. Test Configuration

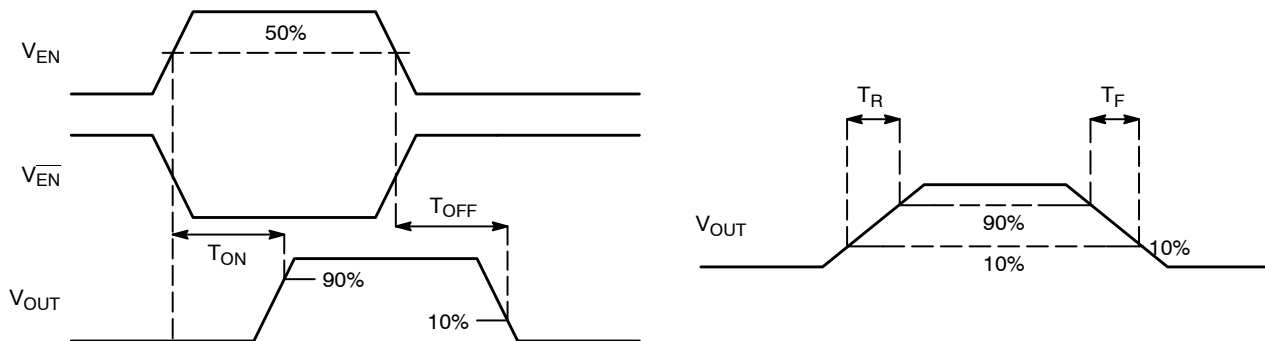
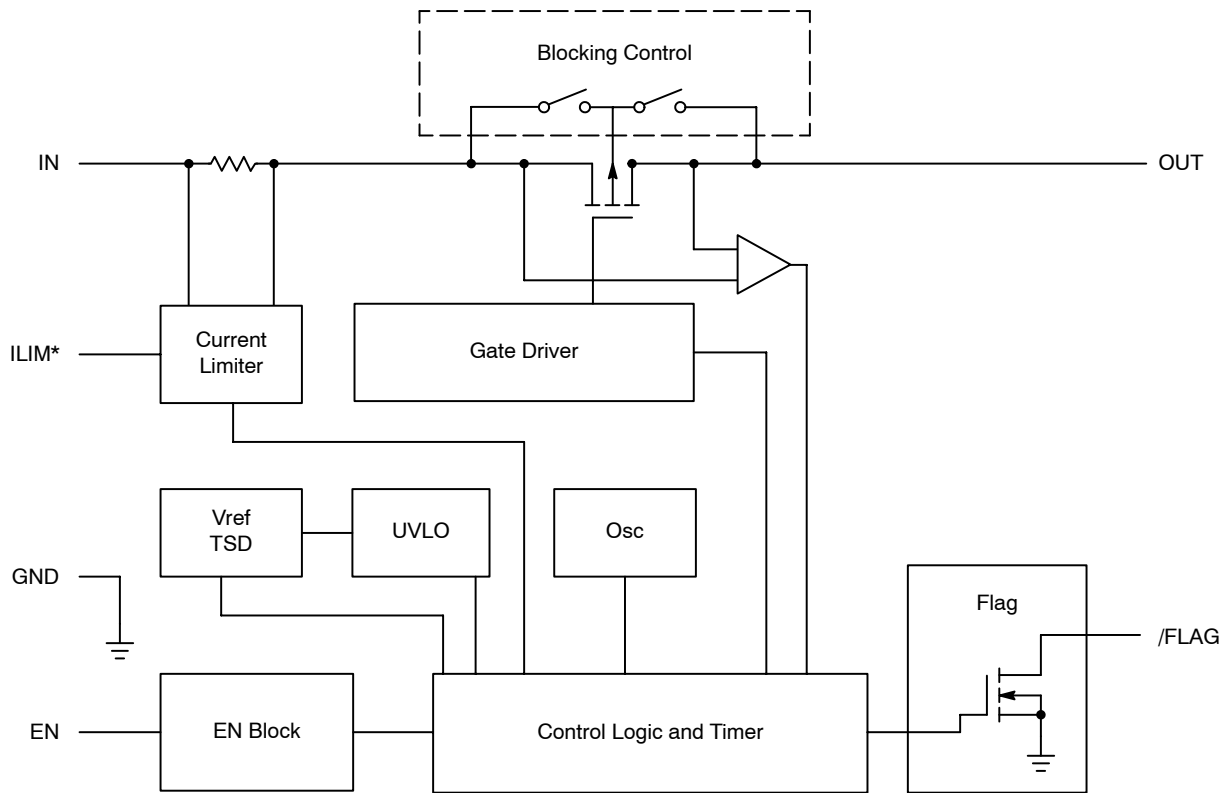


Figure 4. Voltage Waveform

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BLOCK DIAGRAM



*For adjustable version only, otherwise not connected.

Figure 5. Block Diagram

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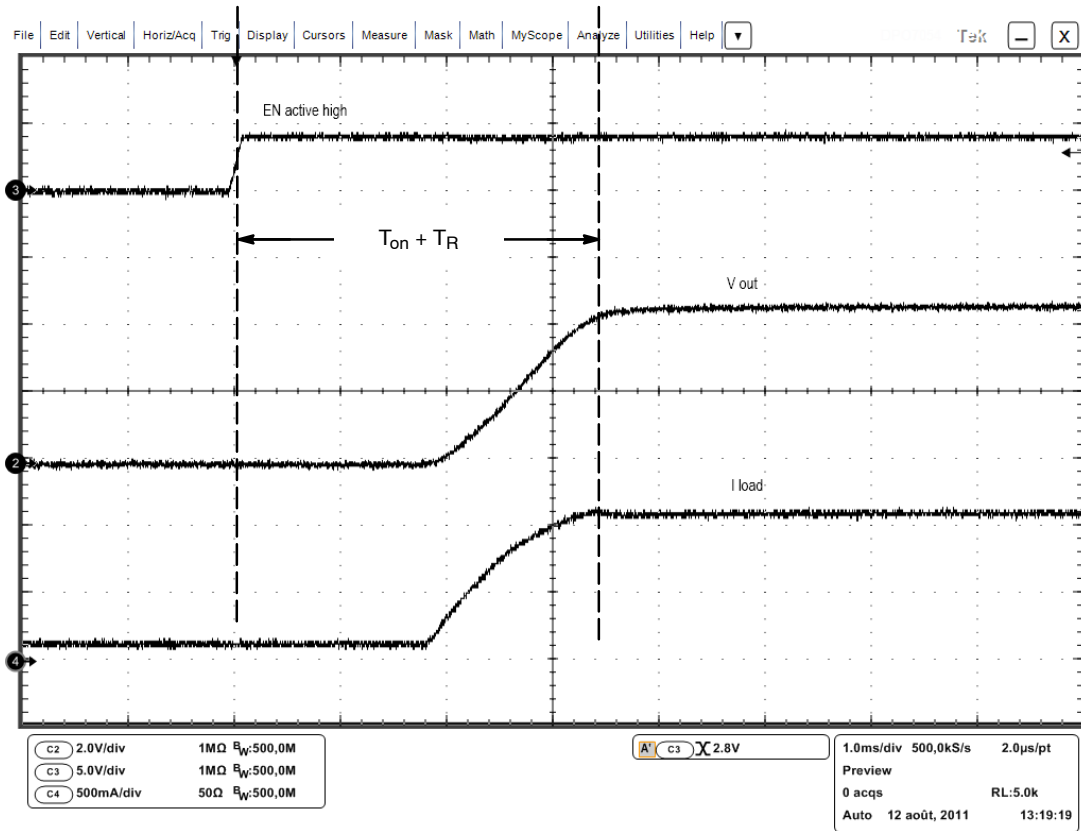


Figure 6. T_{on} Delay and T_{rise} Time

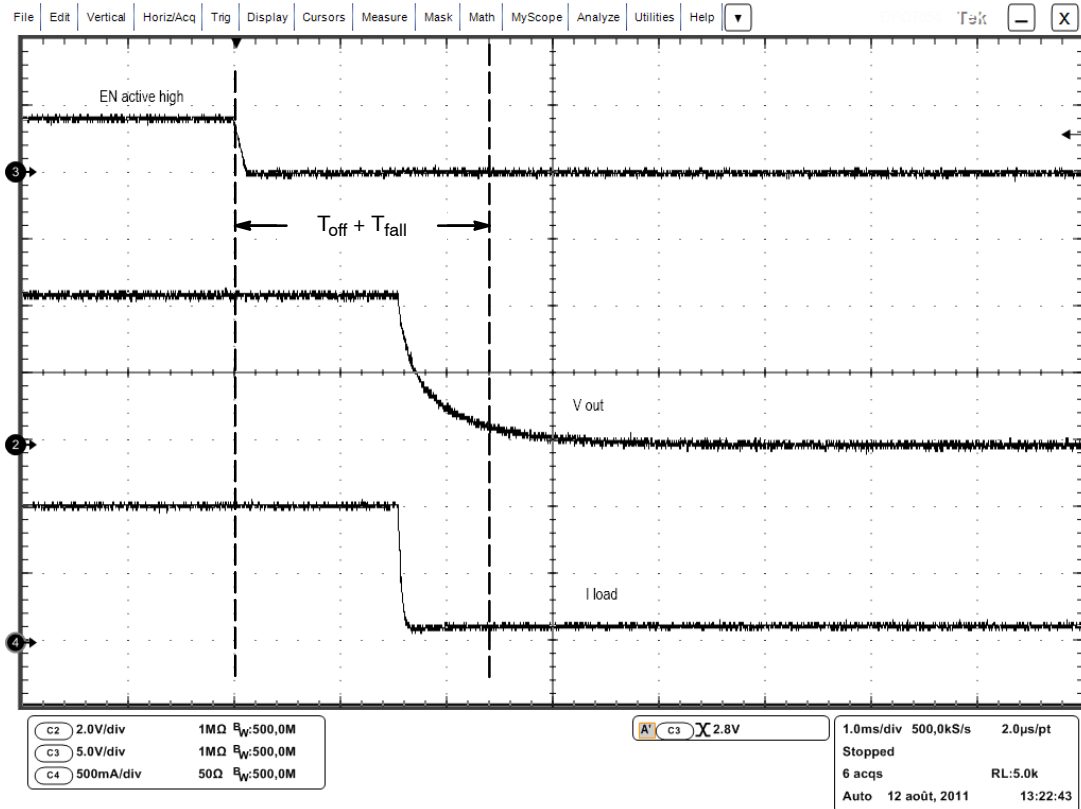


Figure 7. T_{off} Delay and T_{fall}

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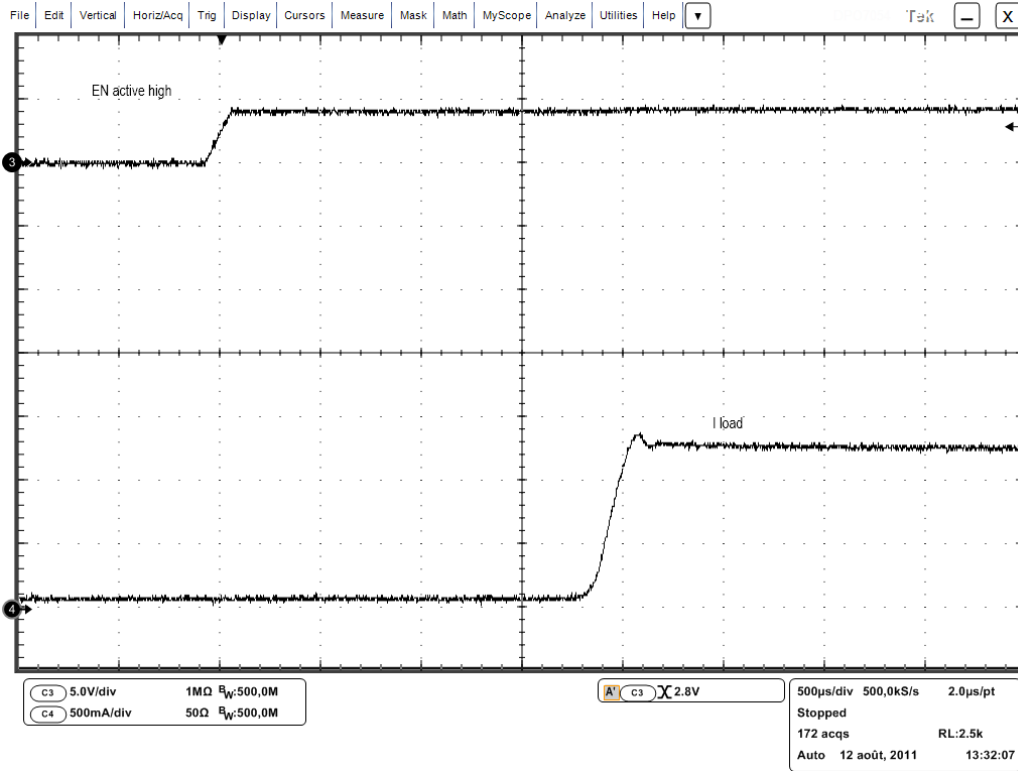


Figure 8. Turn On a Short

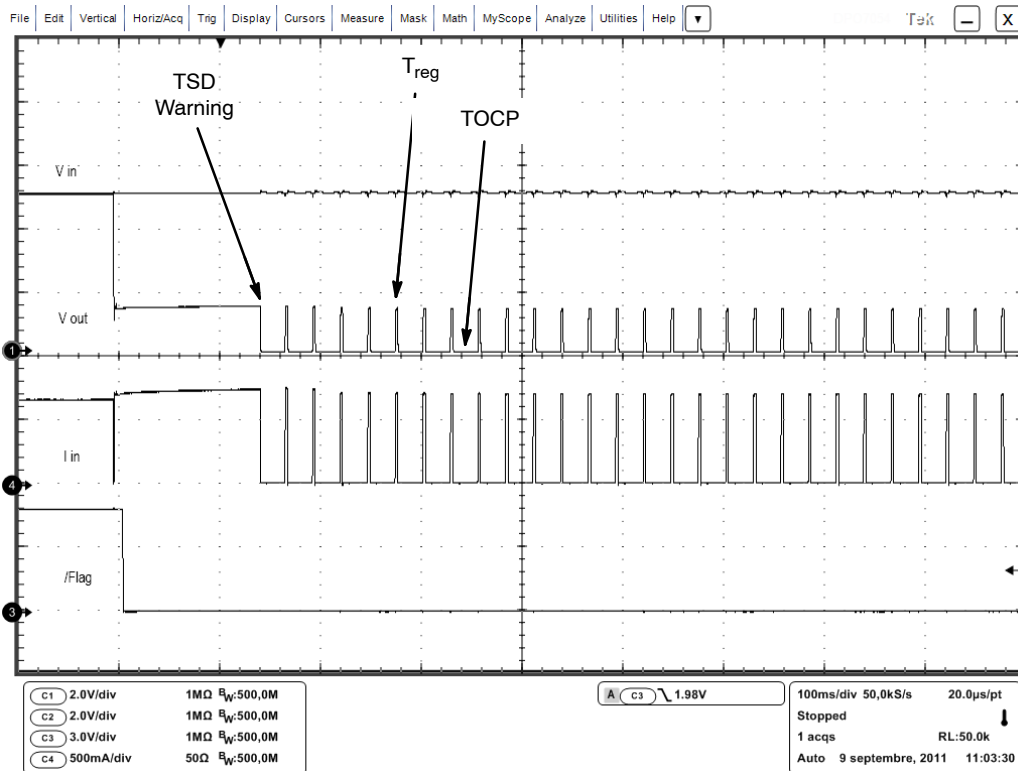


Figure 9. 2 Ω Short on Output. Complete Regulation Sequence

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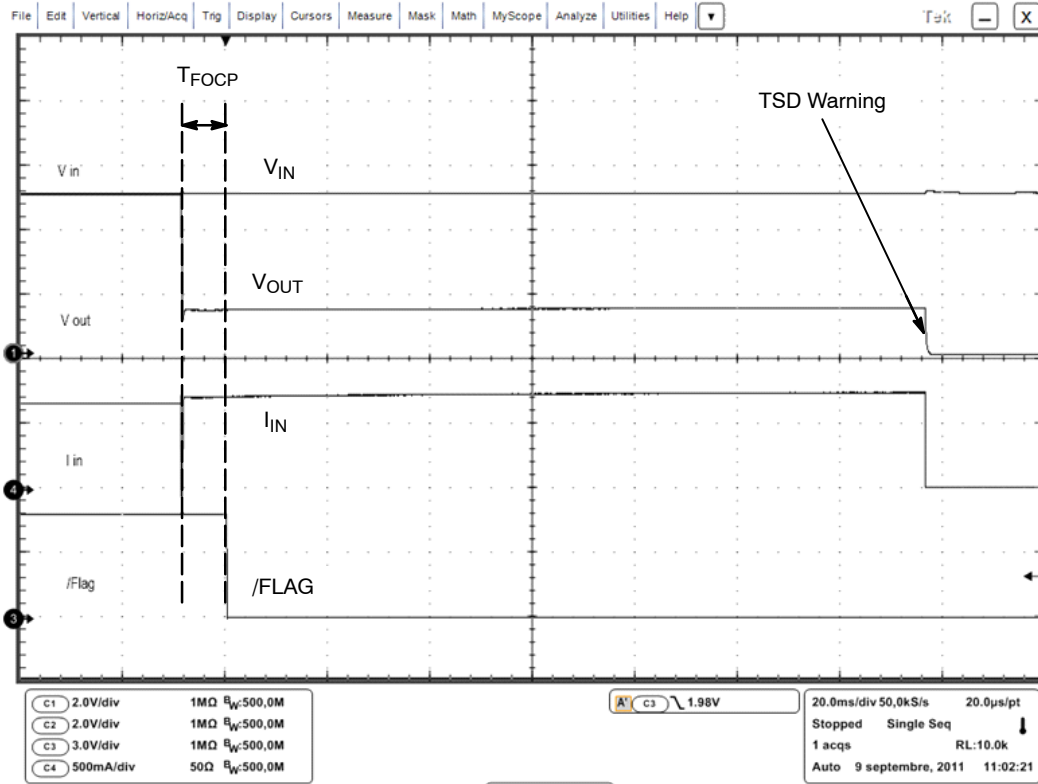


Figure 10. OCP Regulation and TSD Warning Event

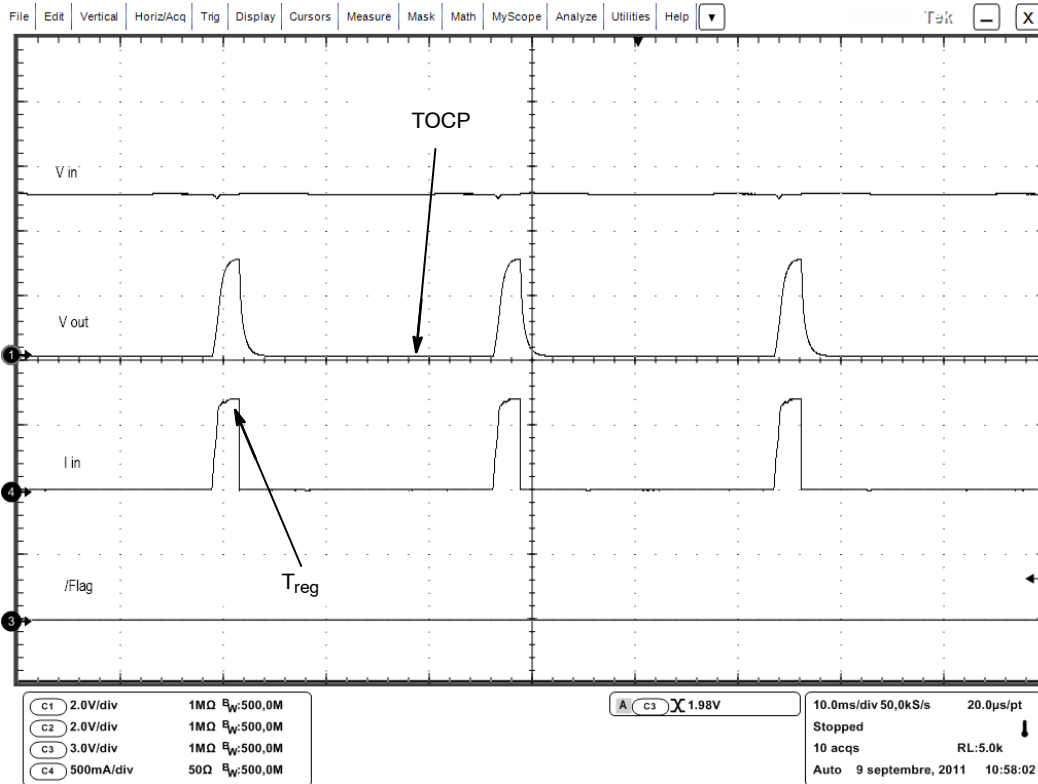


Figure 11. Timer Regulation Sequence During 2 Ω Overload

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Figure 12. Direct Short on OUT Pin



Figure 13. From Timer Regulation to Load Removal Sequence

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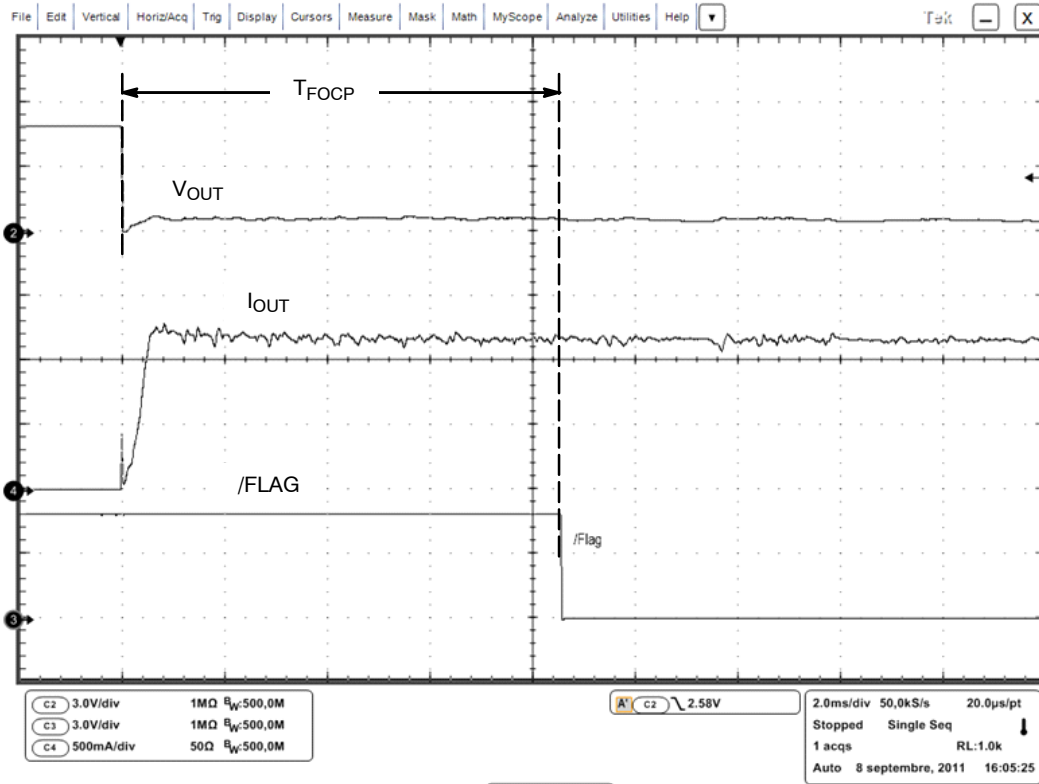


Figure 14. From No Load to Direct Short Circuit

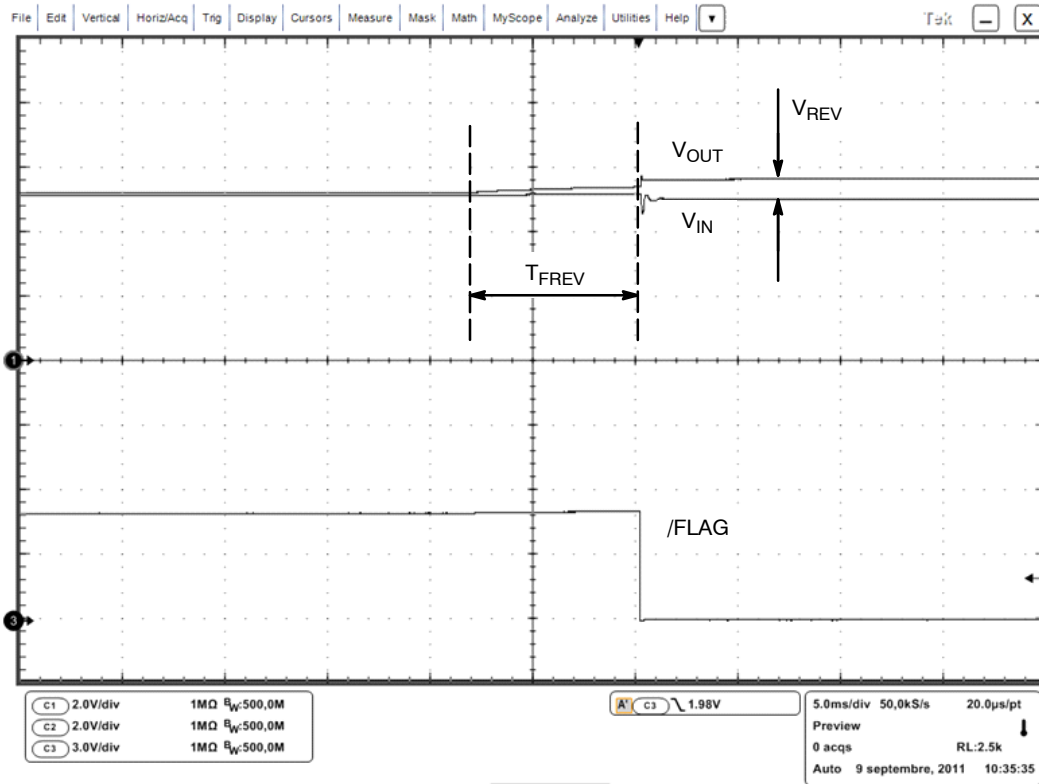


Figure 15. Reverse Voltage Detection

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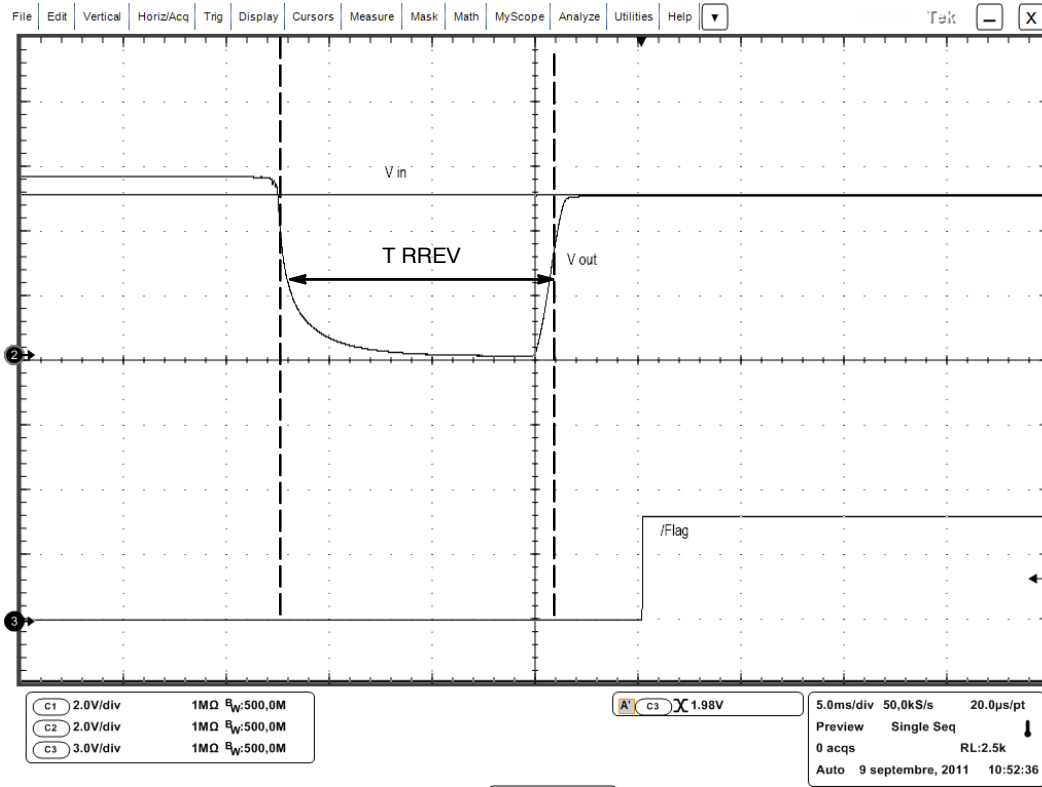


Figure 16. Reverse Voltage Removal

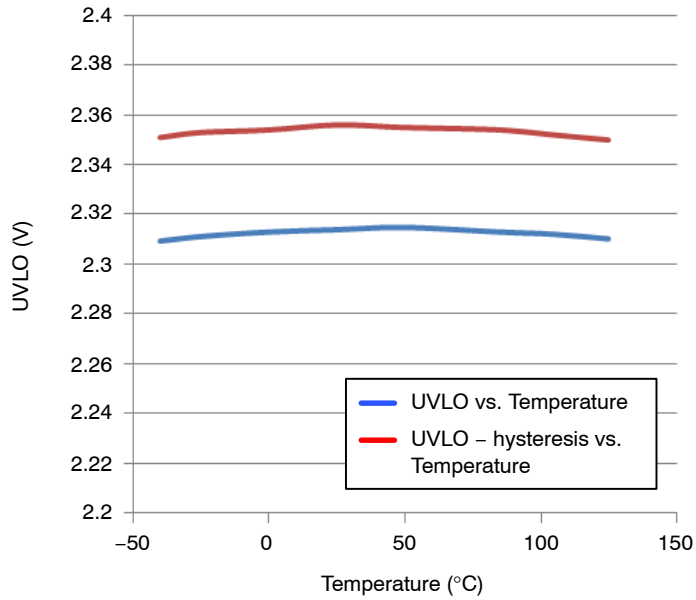


Figure 17. Undervoltage Threshold (Falling) and Hysteresis

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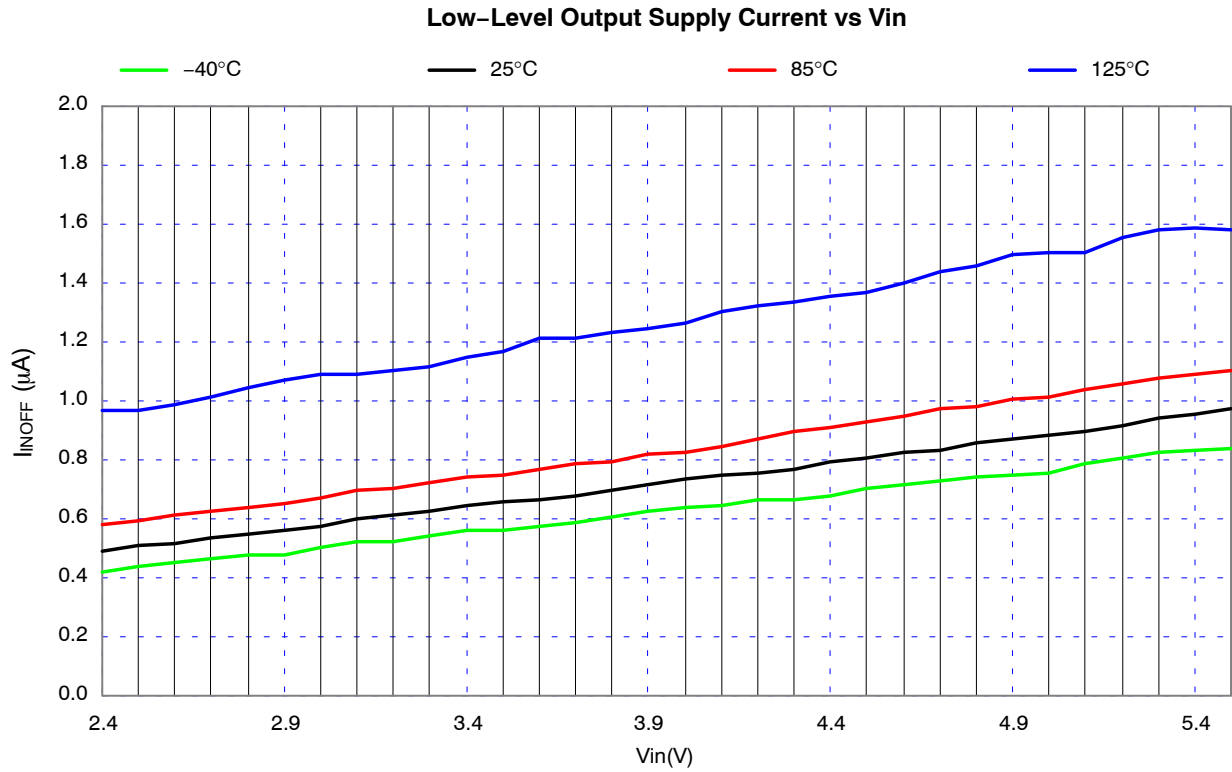


Figure 18. Standby Current vs Vin

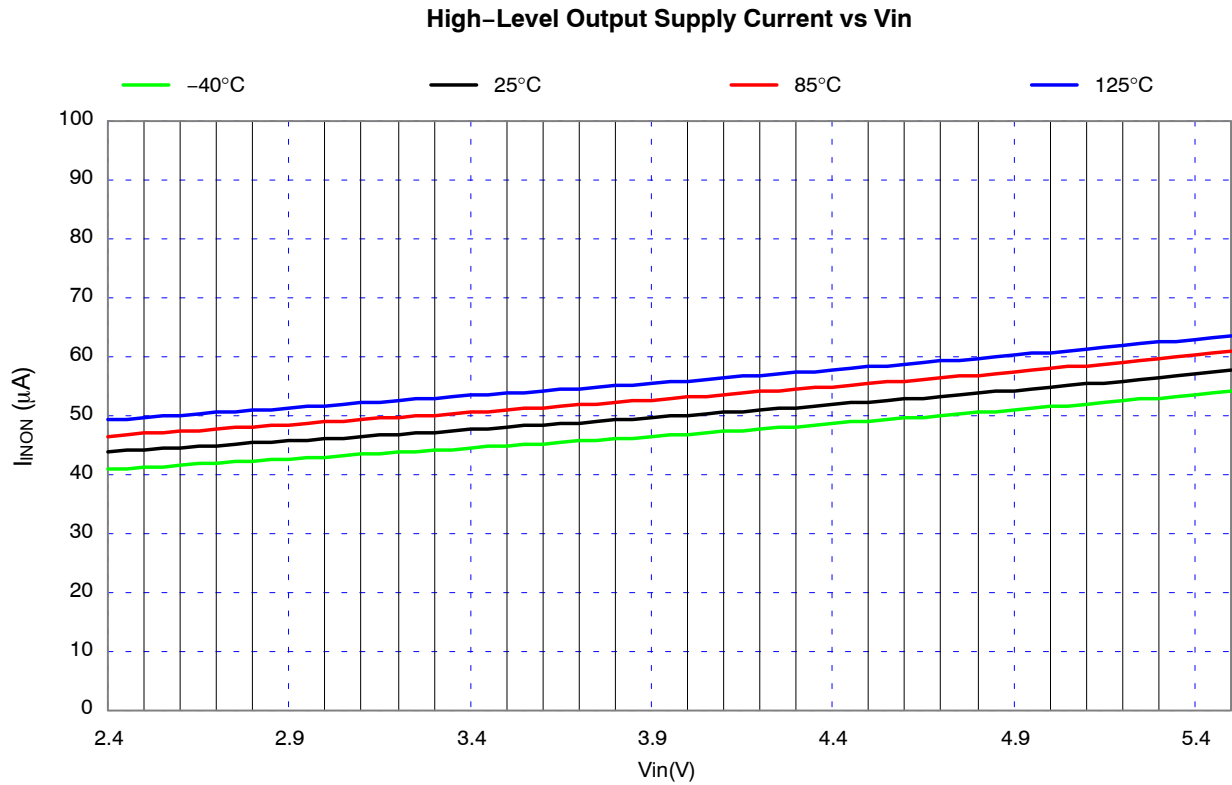


Figure 19. Quiescent Current vs Vin

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TSOP Package

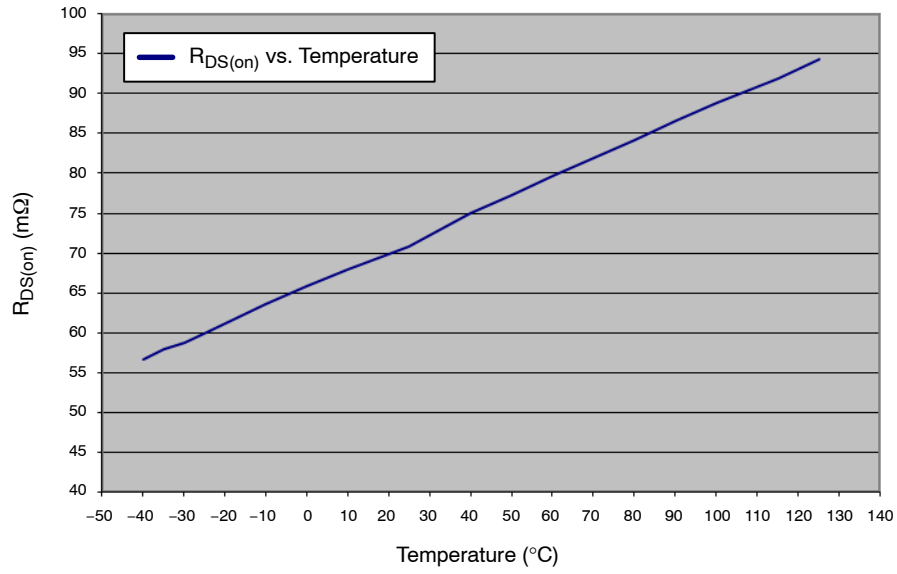


Figure 20. $R_{DS(on)}$ vs Temperature, TSOP Package

μ DFN Package

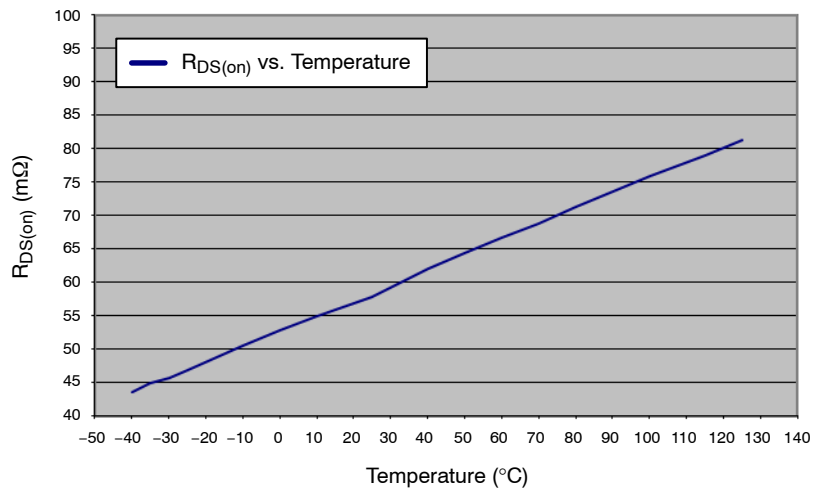


Figure 21. $R_{DS(on)}$ vs Temperature, μ DFN Package

機能説明

概要

NCP380は、大容量負荷、短絡、または過電流の場合に入力供給電圧を保護するために設計された、ハイサイドPチャネルMOSFETパワー・スイッチです。加えて、ハイサイドMOSFETは、低電圧、サーマル・シャットダウン、または逆電圧状態の発生中にターンオフされます。可変バージョンでは、外部抵抗を使用して電流制限スレッシュホールドをプログラムすることができます。NCP380は、ソフトスタート回路によって大電流および電圧サージを抑制できます。

過電流保護

NCP380は、出力電流が I_{OCP} スレッシュホールドを超えると、定電流安定化モードに切り替わります。出力電圧は負荷に応じて低下します。

- 大容量負荷を伴うホット・プラグの場合、出力電圧はコンデンサ電圧まで低下します。NCP380は、コンデンサの充電が完了するまで電流を I_{OCP} スレッシュホールド値に制限します。

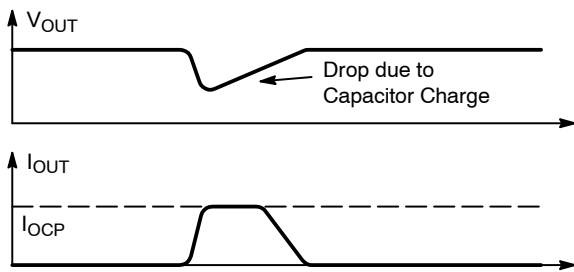


Figure 22. Heavy capacitive load

- 過負荷時、電流は I_{OCP} の値に制限され、電圧値は負荷に応じ、次式に従って低下します。

$$V_{OUT} = R_{LOAD} \times I_{OCP} \quad (\text{eq. 1})$$

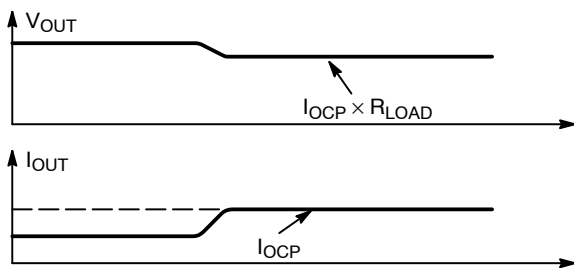


Figure 23. Overload

- 短絡や大きな負荷が発生した場合、電流は短絡が除去されるまで T_{DET} 時間内に I_{OCP} 値に制限されます。出力が短絡されるか非常に低い電圧に接続されると、チップの接合部温度が T_{SDOCP} 値を超え、デバイスはサーマル・シャットダウン(MOSFETがターンオフ)に入ります。

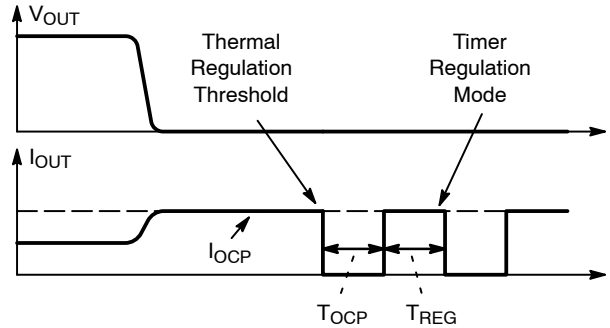


Figure 24. Short circuit

次にデバイスは、次に示す2フェーズのタイマ安定化モードに入ります。

- オフフェーズ：パワーMOSFETは時間 T_{OCP} の間オフになり、ダイ温度が低下します。
- オンフェーズ：時間 T_{REG} の間は安定化電流モードです。電流は I_{OCP} レベルに安定化されます。

タイマ安定化モードでは高熱の放散(短絡の場合など)を処理し、温度動作条件内に抑えることができます。

過電流状態が取り除かれるかイネーブル・ピンが切り替えられるまで、NCP380はオンフェーズ/オフフェーズ・ループに留まります。

備考：アプリケーションによっては、他の安定化モードを使用することも可能です。ご利用については、オン・セミコンダクターの代理店までお問い合わせください。

FLAGインジケータ

FLAGピンは、過電流、逆電圧、または過熱状態時にはローにアサートされるオープンドレインMOSFETです。電力パスで過電流または逆電圧フォールトが検出された場合、対応するグリッチ除去時間(電気的特性表を参照)が経過した後に、FLAGピンはローにアサートされます。この機能のおかげで、大容量負荷の充電や出力での電圧過渡中に、FLAGピンはローになりません。過電流フォールトに対するグリッチ除去時間は T_{FOCP} 、逆電圧フォールトの場合は T_{REV} です。フォールトが除去されるまで、FLAGピンはローのままです。フォールトが除去された後、 T_{FGL} の終わりに、FLAGピンはハイになります。

低電圧ロックアウト

低電圧ロックアウト(UVLO)回路が内蔵されているため、 V_{IN} の電圧が V_{UVLO} よりも低い間、出力は入力から切断されたままです。 V_{IN} 電圧が V_{UVLO} より高くなると、準備時間 T_{RUVLO} 後に、システムは出力の再接続を試みます。この回路は過渡に対するノイズ耐性を提供する V_{HYST} ヒステリシスを備えています。

熱検知

ダイ温度が T_{SD} を超えた場合、サーマル・シャットダウンがパワーMOSFETをターンオフします。ヒステリシスがあるため、ダイ温度が T_{RSD} に冷却されるまでパワーMOSFETはターンオンしません。

逆電圧保護

T_{REV} 中に、出力電圧が入力電圧より V_{REV} だけ高くなると、逆電圧回路は電源を保護するために出力を切断します。パワーMOSFETを再びターンオンするには、これと同じ時間 $T_{REV} +$ 準備時間 T_{RREV} が必要です。

イネーブル入力

イネーブル・ピンは、ロジック信号(CMOSまたはTTL互換)でドライブするか、GNDまたは V_{IN} に接続する必要があります。 V_{IN} とENは直接接続するべきではありません。 V_{IN} は、ICをイネーブルする前に良好に設定されて、安定していなければなりません。

EN信号の分離が出来ない場合は、 $10\text{ k}\Omega/100\text{ nF}$ のRCネットワークを V_{IN} とENの間に追加して、EN信号を遅延させることが出来ます。ENにロジック・ローまたはハイがあると、デバイスはターンオンします。ENにロジック・ハイまたはローがあるとデバイスはターンオフし消費電力は I_{INOFF} にまで減少します。

ブロッキング制御

ブロッキング制御回路は、パワーMOSFETの大半を切り替えます。デバイスがオフのとき、ボディ・ダイオードでOUTからINに流れるリーク電流 I_{REV} が制限されます。このモードでは、ボディ・ダイオードのアノードがINピンに接続され、カソードがOUTピンに接続されます。動作状態では、ボディ・ダイオードのアノードがOUTピンに接続され、カソードがINピンに接続されて、電源の放電が防止されます。

アプリケーション情報

消費電力

デバイスの接合部温度は、ボード・レイアウト、周囲温度、デバイス環境などの要因によって変化します。しかし、接合部温度に最も影響を与える要因は、パワーMOSFETの消費電力です。このように仮定すると、通常モードでの消費電力と接合部温度は、次式で計算できます。

$$P_D = R_{DS(on)} \times (I_{OUT})^2 \quad (\text{eq. 2})$$

ここで、
 P_D = 消費電力(W)
 $R_{DS(on)}$ = パワーMOSFETのオン抵抗(Ω)
 I_{OUT} = 出力電流(A)
 $T_J = P_D \times R_{\theta JA} + T_A$ (eq. 3)

ここで、
 T_J = 接合部温度($^{\circ}\text{C}$)
 $R_{\theta JA}$ = パッケージの熱抵抗($^{\circ}\text{C}/\text{W}$)
 T_A = 周囲温度($^{\circ}\text{C}$)

安定化モードでの消費電力は、次の関係式に従い、負荷に応じて変化する電圧降下 $V_{IN} - V_{OUT}$ を考慮すると計算できます。

$$P_D = (V_{IN} - R_{LOAD} \times I_{OCP}) \times I_{OCP} \quad (\text{eq. 4})$$

ここで、
 P_D = 消費電力(W)
 V_{IN} = 入力電圧(V)
 R_{LOAD} = 負荷抵抗(Ω)
 I_{OCP} = 出力安定化電流(A)

可変電流制限プログラミング (可変バージョンのみ)

NCP380xMUAJAAとNCP380xSNAJAAはそれぞれ μDFN とTSOP6のパッケージで、エンドカスタマーによって自由に電流制限をかけることが出来ます。さらにアースとプルダウン抵抗を接続するIlimピンが用意されており、それによってしきい値電流の調節が可能です。過電流の精度を確保する為に許容差0.1または1%の抵抗を使用することを強く推奨します。

この抵抗の選択について、ユーザーは、デバイスが保護シーケンスに入ることなく継続使用出来るようにUSB電流を最初に設定する必要があります。重要なルールは、このプルダウン抵抗を選択する際に、上流側のアクセサリに継続して電流供給することが出来るように、下限電流値をUSB電流よりも間違いなく高くすることです。

以下の、メインの選択の表はアクセサリへのUSB電流ポート、標準抵抗選択と標準/最大過電流しきい値を含みます。

NCP380, NCV380

Table 5. RESISTOR SELECTION FOR ADJUSTABLE CURRENT LIMIT VERSION

Min Current Limit Value (A)	Theoric Resistor Value (kΩ)	Selected Resistor Value (kΩ) 1% or 0.1%	Typical OCP Target Value (A)	Maximum Current Value (A)
0.5	44.2	44.2	0.59	0.67
0.6	37.5	37.4	0.71	0.81
0.7	32.2	31.6	0.825	0.95
0.8	27.7	27.4	0.94	1.08
0.9	24.0	23.7	1.06	1.22
1.0	21.0	21	1.18	1.35
1.1	18.5	18.2	1.3	1.49
1.2	16.6	16.5	1.41	1.62
1.3	14.6	14.3	1.53	1.76
1.4	13.0	13	1.65	1.9
1.5	11.4	11.3	1.78	2.05
1.6	10.4	10.2	1.88	2.17
1.7	9.2	9.09	2.01	2.31
1.8	8.3	8.25	2.12	2.438
1.9	7.4	7.32	2.23	2.56
2.0	6.5	6.49	2.36	2.7
2.1	5.6	5.49	2.48	2.85

表の“下限電流値”は過電流起動していない状態でのアクセサリへ供給するDC電流を表しています。

2番目の行は、以下の式から求められた標準電流ターゲットを得るための抵抗理論値です：

$$R_{lim} = -5.2959 \times ILIM^5 + 45.256 \times ILIM^4 - 155.25 \times ILIM^3 + 274.39 \times ILIM^2 - 267.6 \times ILIM + 134.21 \quad (\text{eq. 5})$$

R_{LIM} Versus OCP Average

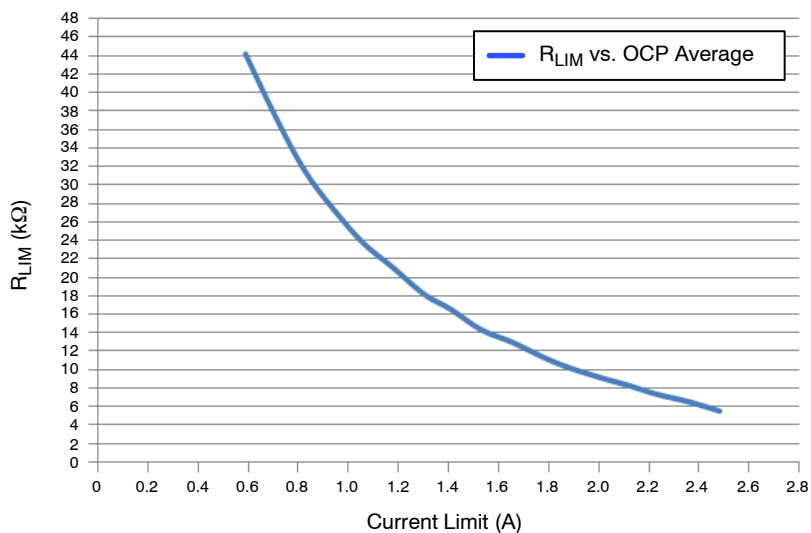


Figure 25. R_{LIM} Curve vs. Current Limit

NCP380, NCV380

ユーザーのアプリケーションに合わせて抵抗が選択されると、過電流しきい値の許容値は以下の式にて求められます：

$$IOCP_{min} = 1.6915129 - 0.0330328 \times R_{lim} + 0.0011207(R_{lim} - 22.375)^2 - 0.0000451 \times (R_{lim} - 22.375)^3 + 0.0000009 \times (R_{lim} - 22.375)^4 \quad (\text{eq. 6})$$

$$IOCP_{max} = 2.2885175 - 0.0446914 \times R_{lim} + 0.0015163(R_{lim} - 22.375)^2 - 0.000061 \times (R_{lim} - 22.375)^3 + 0.0000012 \times (R_{lim} - 22.375)^4 \quad (\text{eq. 7})$$

$$IOCP_{typ} = 1.9900152 - 0.0388621 \times R_{lim} + 0.0013185(R_{lim} - 22.375)^2 - 0.0000531 \times (R_{lim} - 22.375)^3 + 0.0000011 \times (R_{lim} - 22.375)^4 \quad (\text{eq. 8})$$

最小、標準、最大電流カーブは以下のグラフの通りとなります：

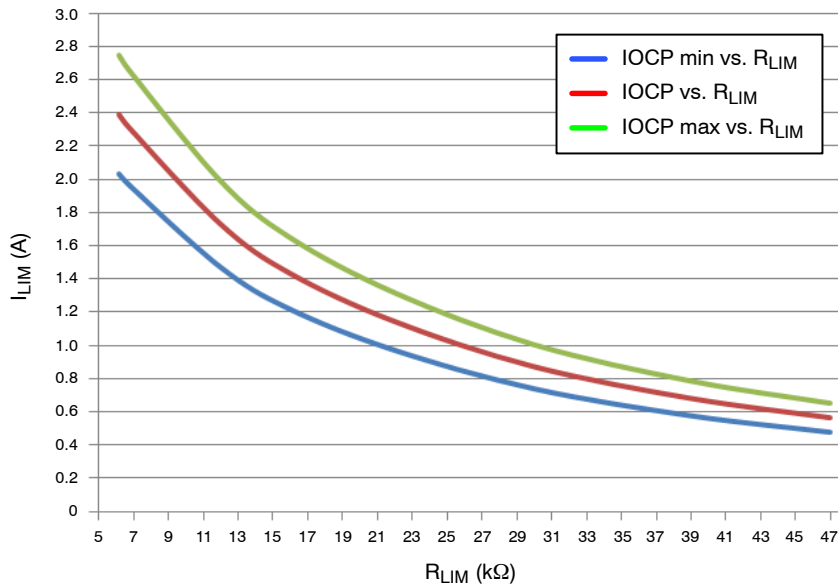


Figure 26. Current Threshold vs. Rlim Resistor

2つ理由から抵抗値6 kΩ–47 kΩの範囲を考慮されることを推奨します。

低い抵抗値の時、電流許容値は高い電流レベルに押し上げられます。内部電力損失性能によって、温度による影響を考慮すると最大2.4 A標準をμDFNパッケージに設定することが出来ます。TSOP6バージョンに関しては、製品が定電流制御モードに入る前にサーマルシャットダウンモードに入る可能性もある為、最大で1.2 Aが推奨値になります。

一方で、もし15%の精度を維持したい時には高い抵抗値で50 kΩまで使用出来ます。高い値の場合、電流しきい値は500 mAよりも低くなります。その為この場合、精度が落ちることがあります。

PCBに関する推奨事項

NCP380は最大定格2 AのPMOSFETを集積しているため、PCBデザイン・ルールを遵守してシリコンからの熱を適切に逃がす必要があります。必要に応じて、熱伝導を高めるためにUDFN6 PAD1をグランド・プレーンに接続してください。このパッドは必ずグランド・プレーンに接続します。PCB面積を増やすことで、パッケージのR_{θJA}を低減できますが、代わり消費電力が増大します。

NCP380, NCV380

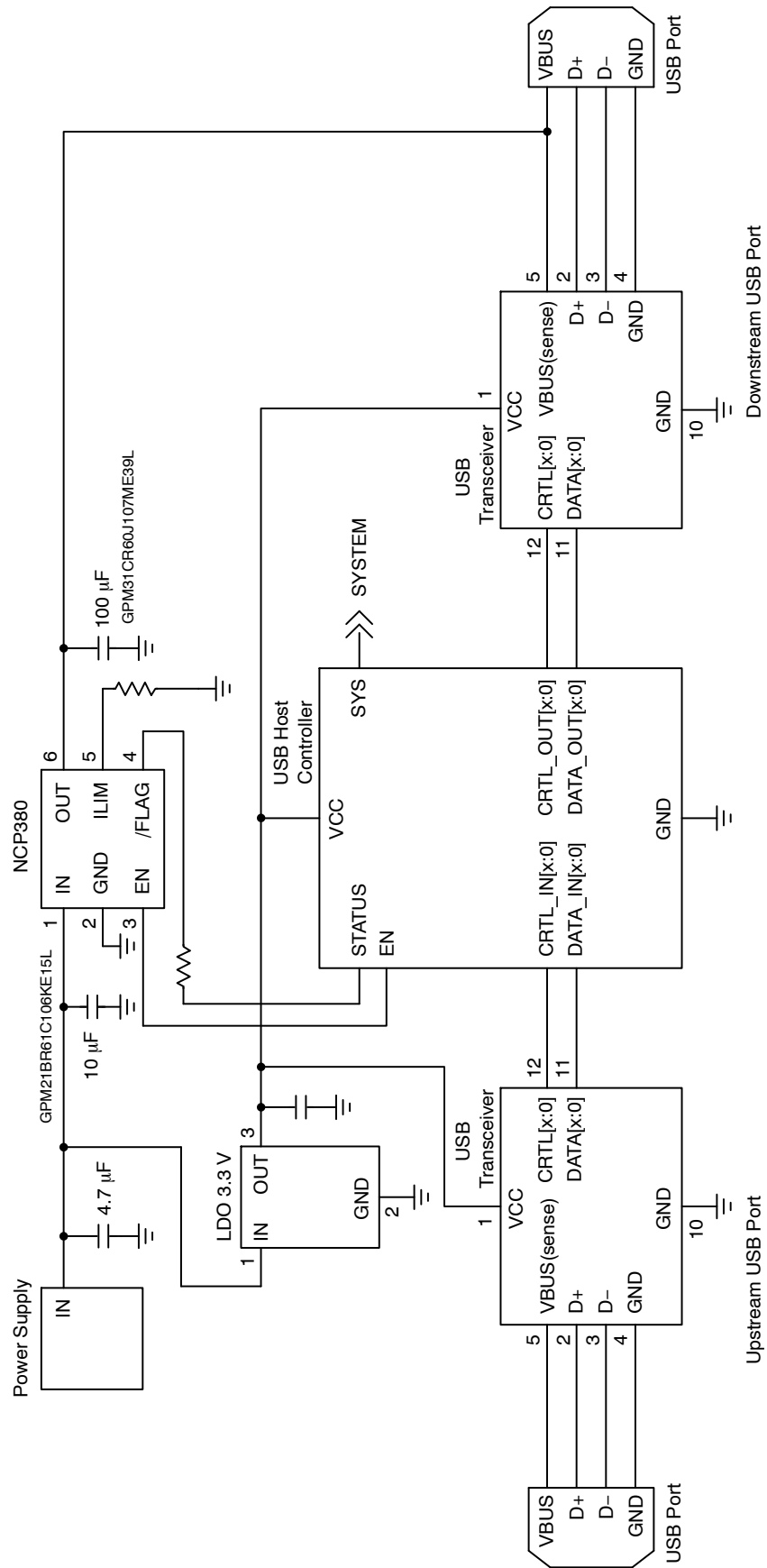


Figure 27. USB Host Typical Application

NCP380, NCV380

Table 6. ORDERING INFORMATION

Device	Marking	Active Enable Level	Over Current Limit	Evaluation Board	UL Listed	CB Scheme	Package	Shipping†
NCP380LSNAJAAT1G	AAC	Low	Adj.	NCP380LSNAJAGEVB	Y	Y	TSOP-6 (Pb-Free)	3,000 Tape / Reel
NCP380LSN05AAT1G	AC5		0.5 A	NCP380LSN05AGEVB	Y	Y	TSOP-5 (Pb-Free)	
NCP380LSN10AAT1G	AC6		1.0 A	NCP380LSN10AGEVB	Y	Y		
NCP380LMUJAATBG	AA		Adj.	NCP380LMUJAGEVB	Y	Y	UDFN6 (Pb-Free)	
NCV380LMUJAATBG*	AN		Adj.	NCP380LMUJAGEVB	Y	Y		
NCP380LMU05AATBG	AE		0.5 A	NCP380LMU05AGEVB	Y	Y		
NCP380HSNAJAAT1G	AAD	High	Adj.	NCP380HSNAJAGEVB	Y	Y	TSOP-6 (Pb-Free)	
NCP380HSN05AAT1G	AC7		0.5 A	NCP380HSN05AGEVB	Y	Y	TSOP-5 (Pb-Free)	
NCP380HSN10AAT1G	ADA		1.0 A	NCP380HSN10AGEVB	Y	Y		
NCP380HMUJAATBG	AC		Adj.	NCP380HMUJAGEVB	Y	Y	UDFN6 (Pb-Free)	
NCV380HMUJAATBG*	AP		Adj.	NCP380HMUJAGEVB	Y	Y		
NCP380HMU05AATBG	AH		0.5 A	NCP380HMU05AGEVB	Y	Y		
NCP380HMU10AATBG	AJ		1.0 A	NCP380HMU10AGEVB	Y	Y		
NCP380HMU15AATBG	AK		1.5 A	NCP380HMU15AGEVB	Y	Y		
NCP380HMU20AATBG	AM		2.0 A	NCP380HMU20AGEVB	Y	Y		
NCP380HMU21AATBG	AU		2.1 A	NCP380HMU21AGEVB	Y	Y		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

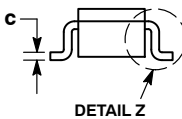
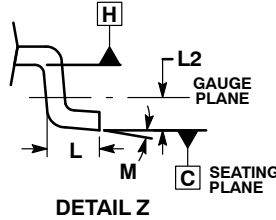
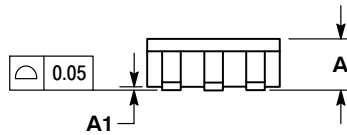
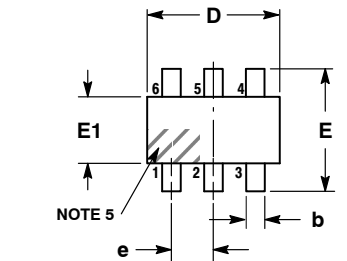
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TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



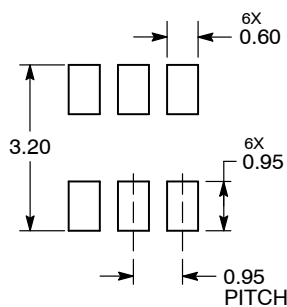
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|----------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- | | |
|--------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| <p>XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package</p> | <p>XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package</p> |
|--------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

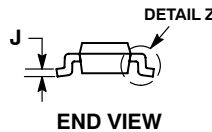
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TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ■ = Pb-Free Package
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

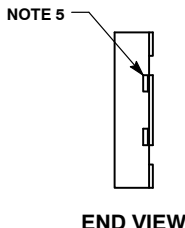
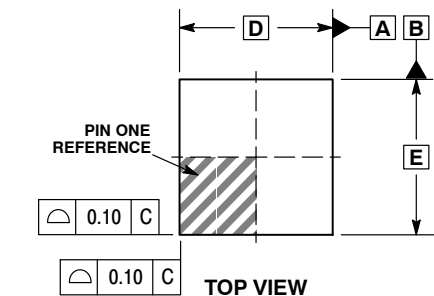
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SCALE 4:1

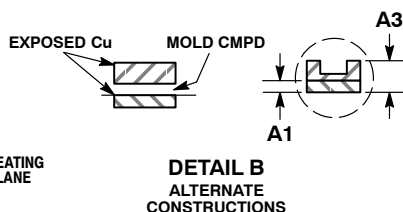
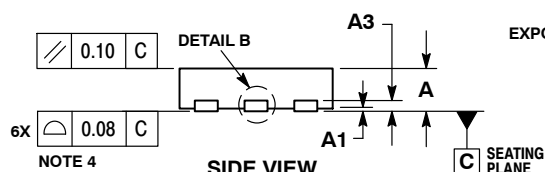
UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C

DATE 10 APR 2013



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15



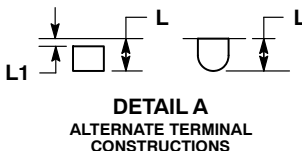
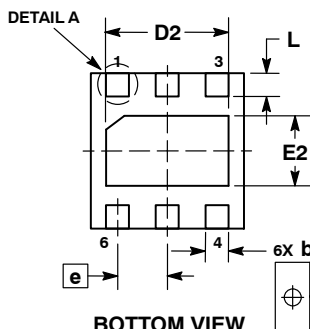
GENERIC MARKING DIAGRAM*



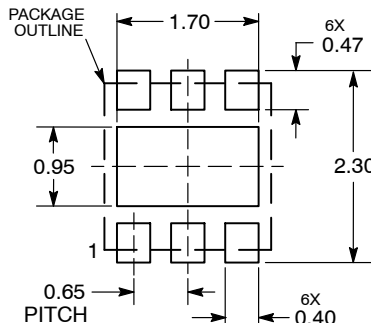
- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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