Notes:

1. Material: UL recognized component 370HR, UL File Number: E41625, relative permitivity 4.2 nominal
2. Controlled impedance of 90 Ohm for the USB and MIPI CSI-2 interface differencial data signals should be carried out. The impedance of particular traces has been designed using exactly Isola 370HR material performance data. Usage of any replacement material is not recommended.
3. Controlled impedance of 50 Ohm for the internal antenna trace within the RSL10 SiP IC should be carried out. The impedance of particular trace has been designed using exactly Isola 370HR material performance data. Usage of any replacement material is not recommended.
4. Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer 1 ÷ 4 µm, gold layer 0.076 ÷ 0.2 µm
5. All vias in SMD pads have to be filled and plated over to allow proper soldering
6. All gerber files generated as a top view
7. Gerber files for internal power planes have to be inverted
8. Fabricate according IPC-A-600
9. Non-conductive epoxy ink recommended for silkscreen
10. Silkscreen should not cover any exposed copper, silkcreen gerber data have to be trimmed eventually
11. All holes diameter refer to final diameter after eventual plating
12. Solder mask tenting is applied on number of vias both on top layer

Gerber file extensions table

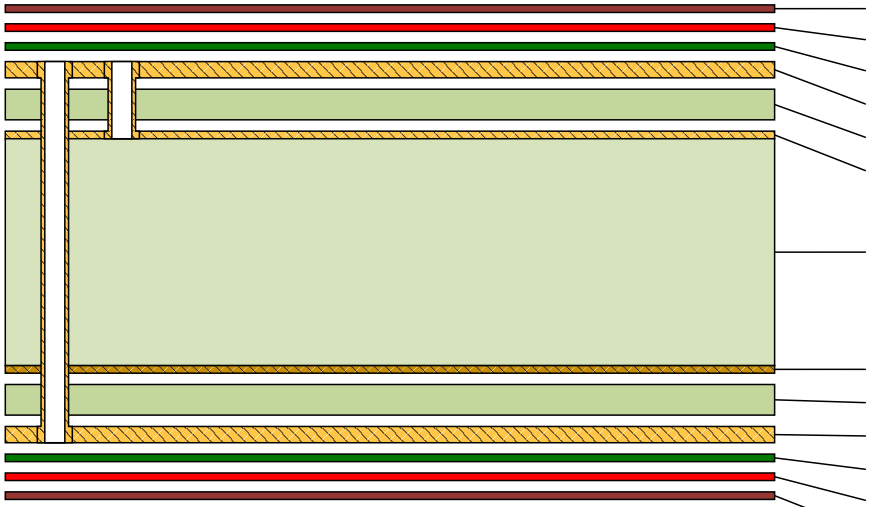
Gerber files	
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	Top layer L1_TOP
.G1	Internal signal layer/ground plane L2_GND
.GP1	Internal power plane L3_PWR - has to be inverted
.GBL	Bottom layer L4_BOTTOM
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Botom side silkscreen
.GBP	Bottom side solder paste mask
.GM1	Board outline

Drill file extensions table

Drill files	
ULP_BLE_Camera-RoundHoles.TXT	Layer pair L1_TOP to L4_BOTTOM - round holes
ULP_BLE_Camera-SlotHoles.TXT	Layer pair L1_TOP to L4_BOTTOM - slot holes
ULP_BLE_Camera-RoundHoles.TXT1	Layer pair L1_TOP to L2_GND - round holes

SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
PCB fabrication notes and requirements		Fabrication document	Sheet 1 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Layer Stack

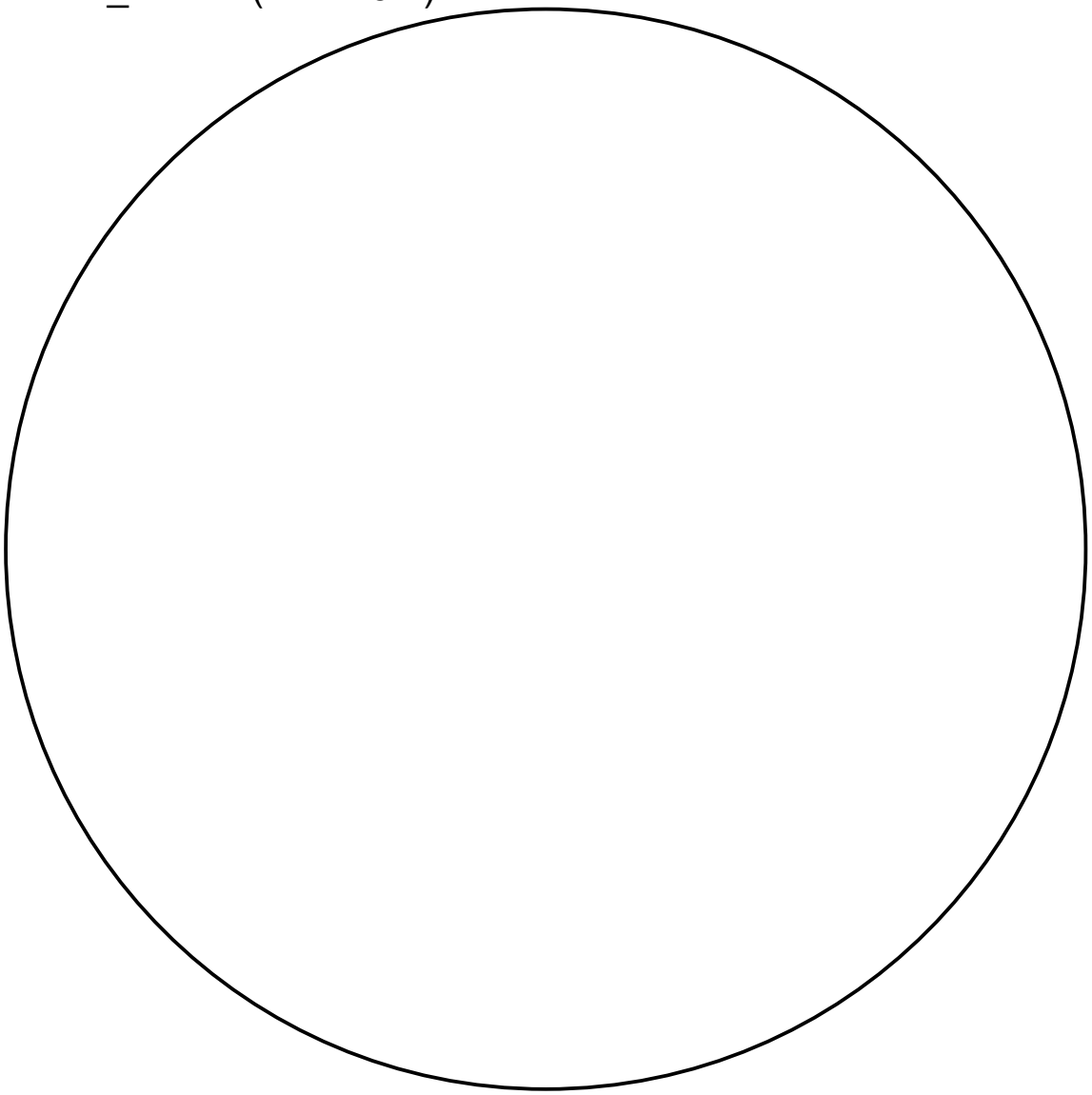


Material	Layer	Thickness	Dielectric Material	Permitivity	Type	Gerber
	Top Paste				Paste Mask	GTP
	Top Overlay				Legend	GTO
Surface Material	Top Solder	0.0150mm(0.591mil)	Solder Resist		Solder Mask	GTS
Copper	L1_TOP	0.0430mm(1.693mil)			Signal	GTL
Prepreg		*0.0810mm(3.189mil)*	*Isola 370HR: 1080-68*	*3.86*	*Dielectric*	
Copper	L2_GND	0.0180mm(0.709mil)			Signal	G1
Core		*1.0670mm(42.008mil)*	*Isola 370HR: 6x7628-42*	*4.36*	*Dielectric*	
Copper	L3_PWR	0.0180mm(0.709mil)			Internal Plane	GP1
Prepreg		*0.0810mm(3.189mil)*	*Isola 370HR: 1080-68*	*4.2*	*Dielectric*	
Copper	L4_BOTTOM	0.0430mm(1.693mil)			Signal	GBL
Surface Material	Bottom Solder	0.0150mm(0.591mil)	Solder Resist		Solder Mask	GBS
	Bottom Overlay				Legend	GBO
	Bottom Paste				Paste Mask	GBP

Total thickness: 1.3810mm(54.372mil)

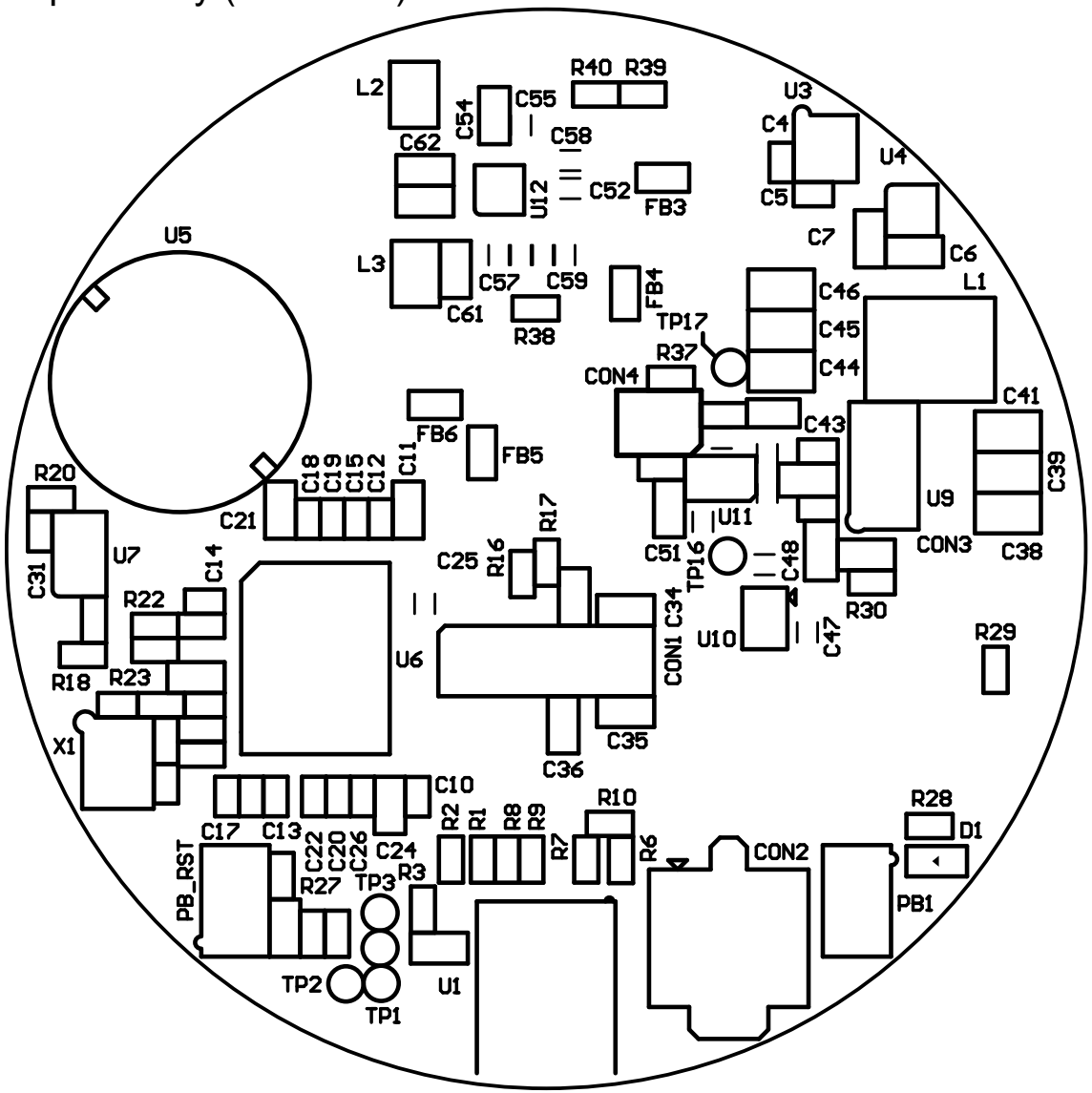
SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Layer stack details		Fabrication document	Sheet 2 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Board_outline (Scale 3:1)



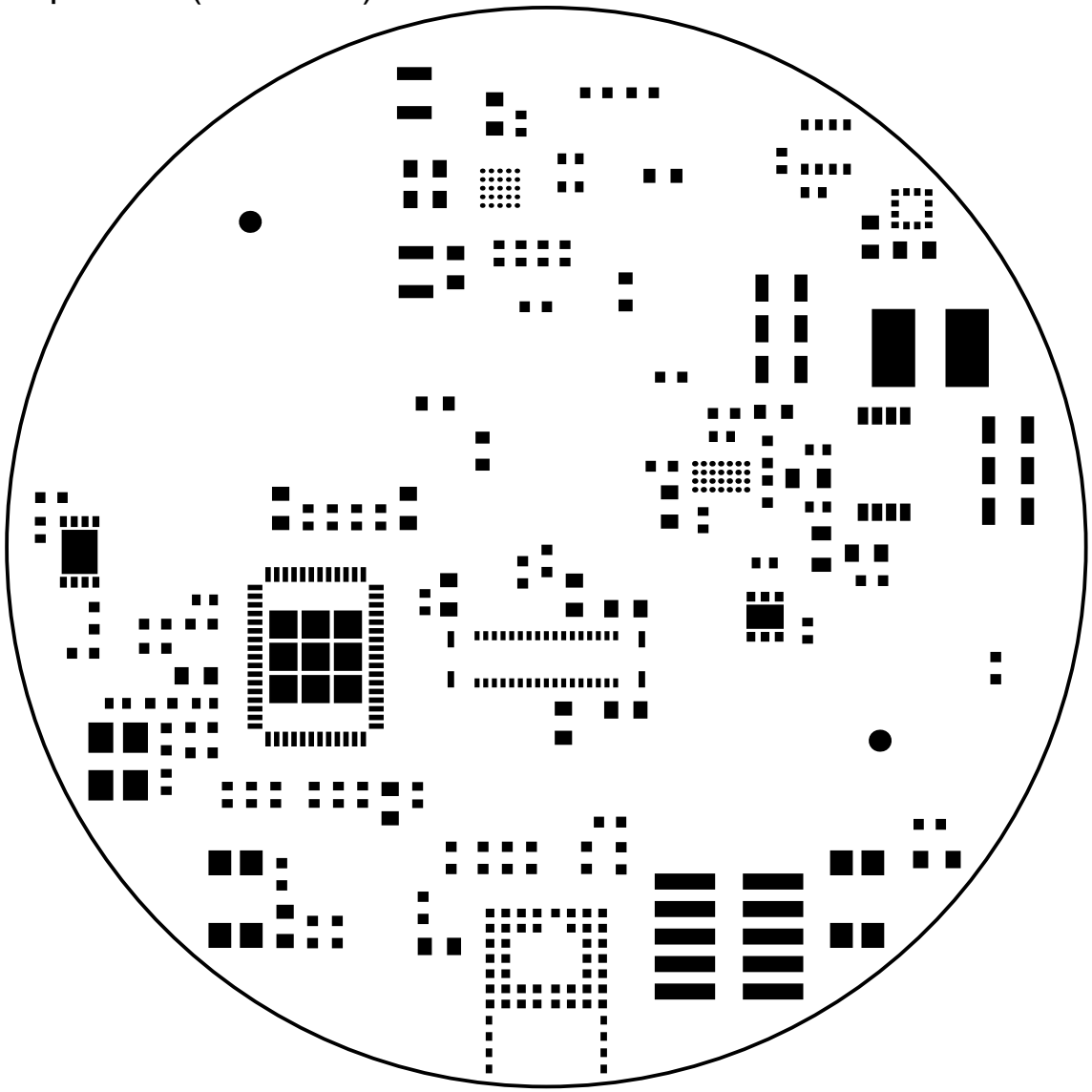
SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Board outline definition - top view 3:1		Fabrication document	Sheet 3 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Top Overlay (Scale 3:1)



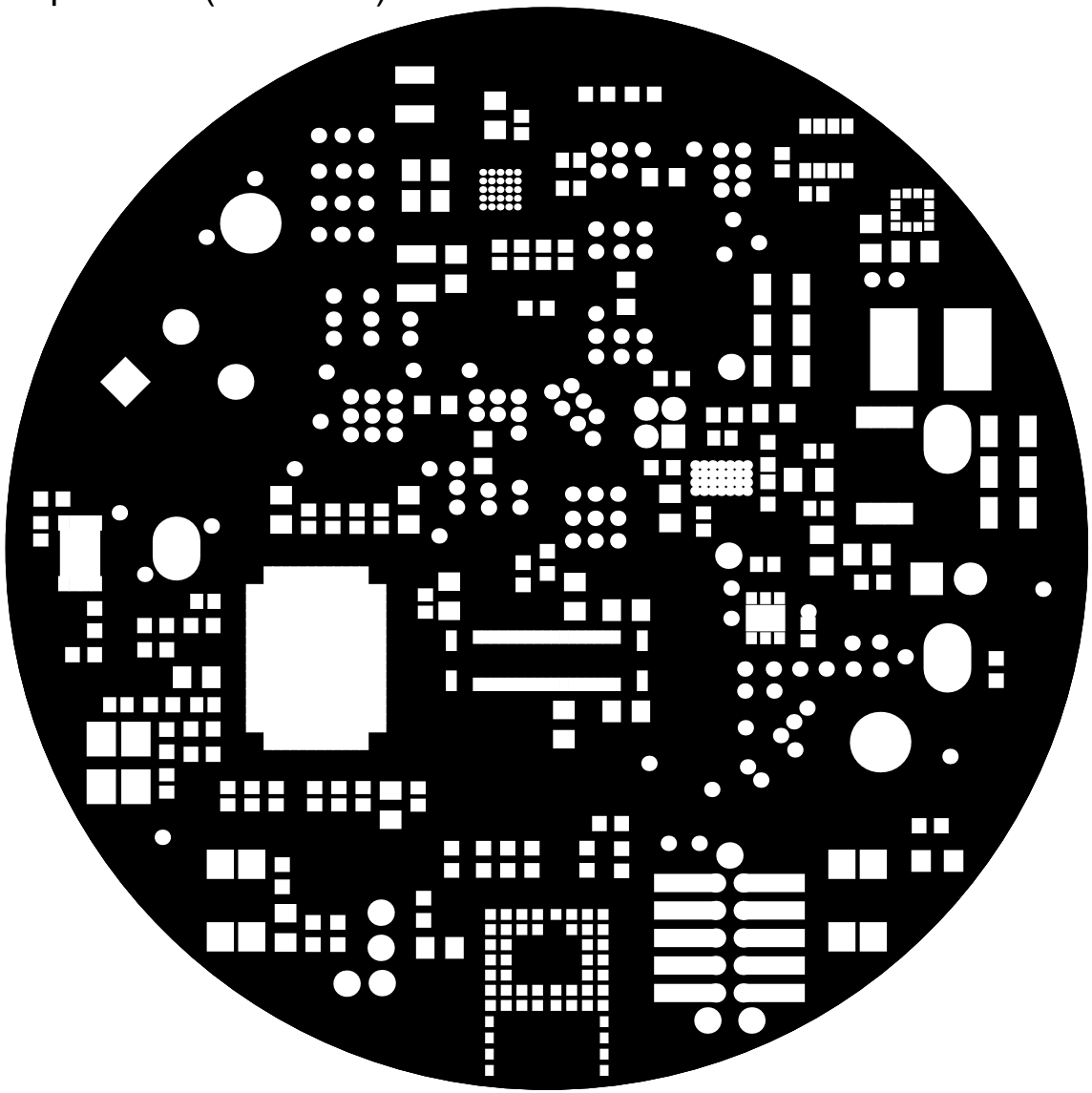
SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Top side silkscreen		Fabrication document	Sheet 4 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Top Paste (Scale 3:1)



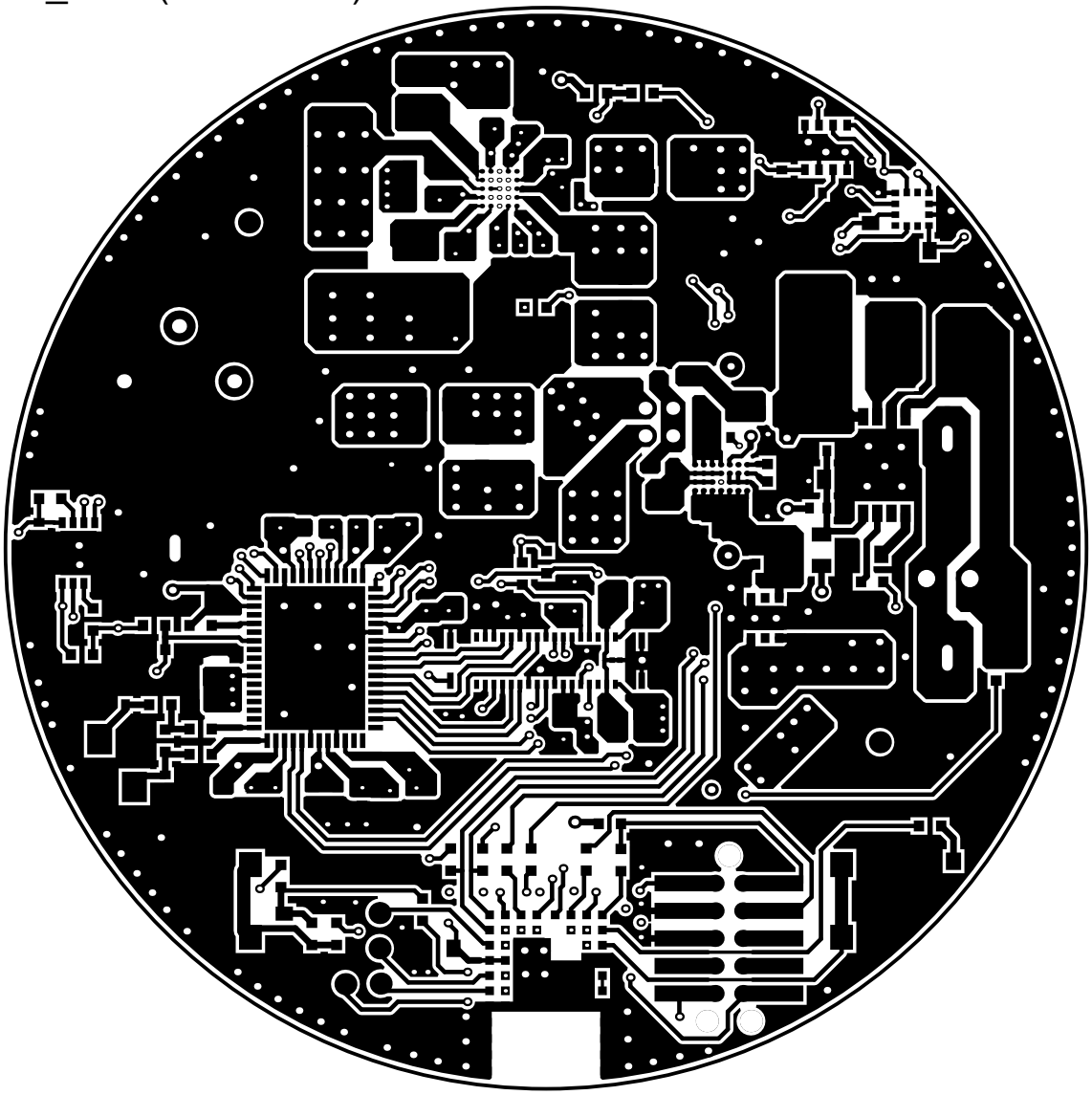
SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Top side solder paste		Fabrication document	Sheet 5 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Top Solder (Scale 3:1)



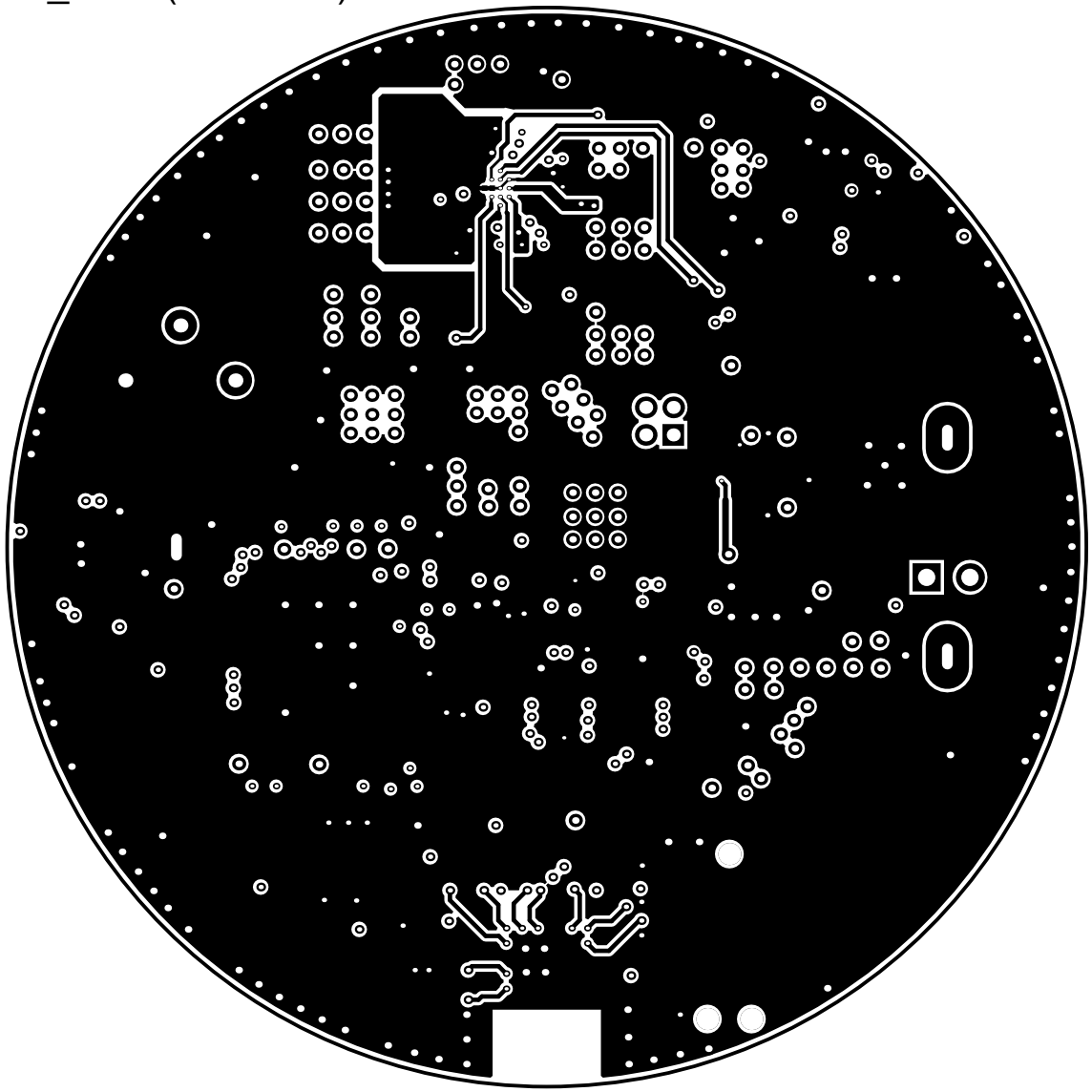
SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Top side solder mask		Fabrication document	Sheet 6 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: Not in repository control			

L1_TOP (Scale =3:1)



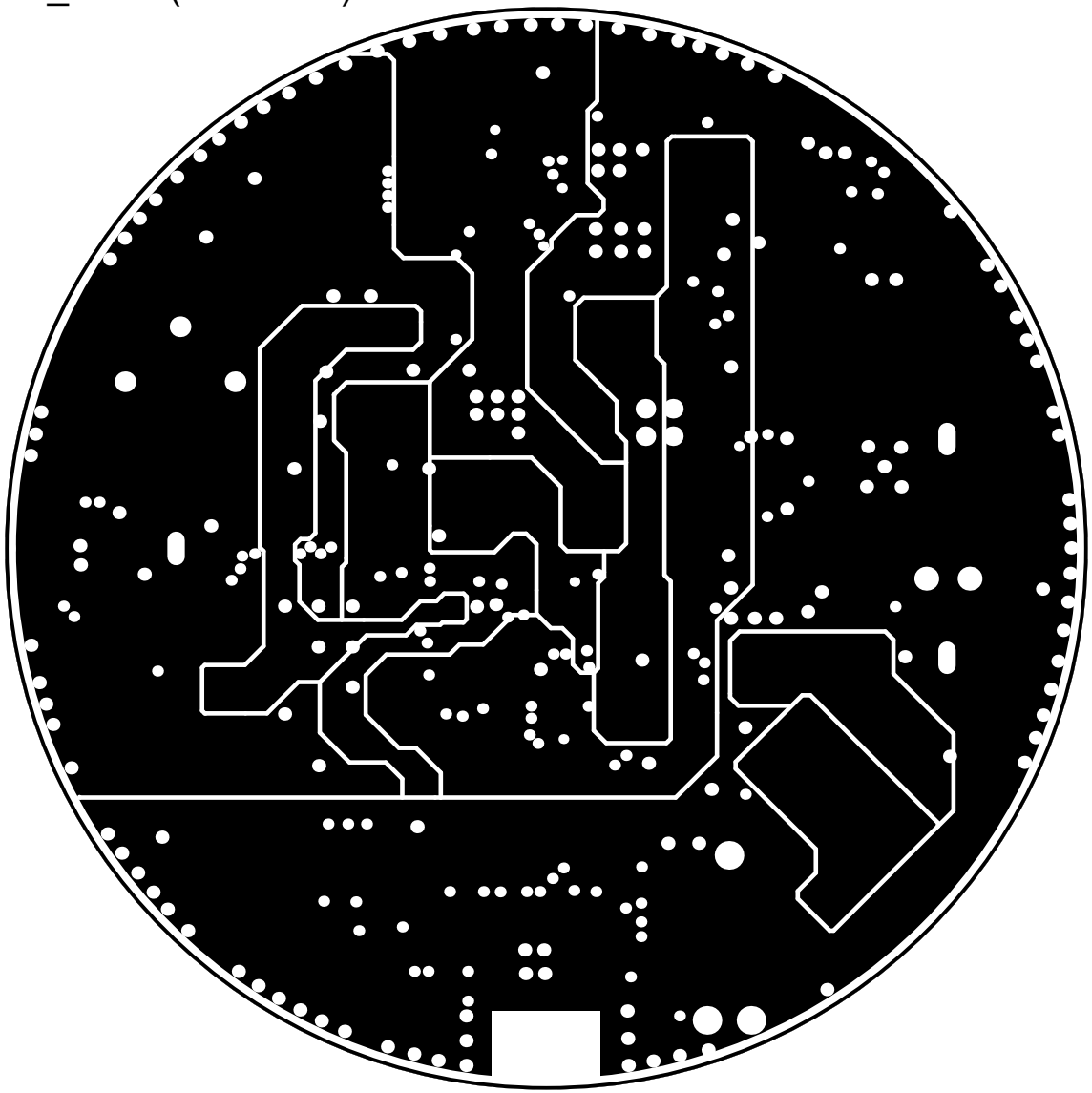
SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Layer L1_TOP		Fabrication document	Sheet 7 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: Not in repository control			

L2_GND (Scale 3:1)



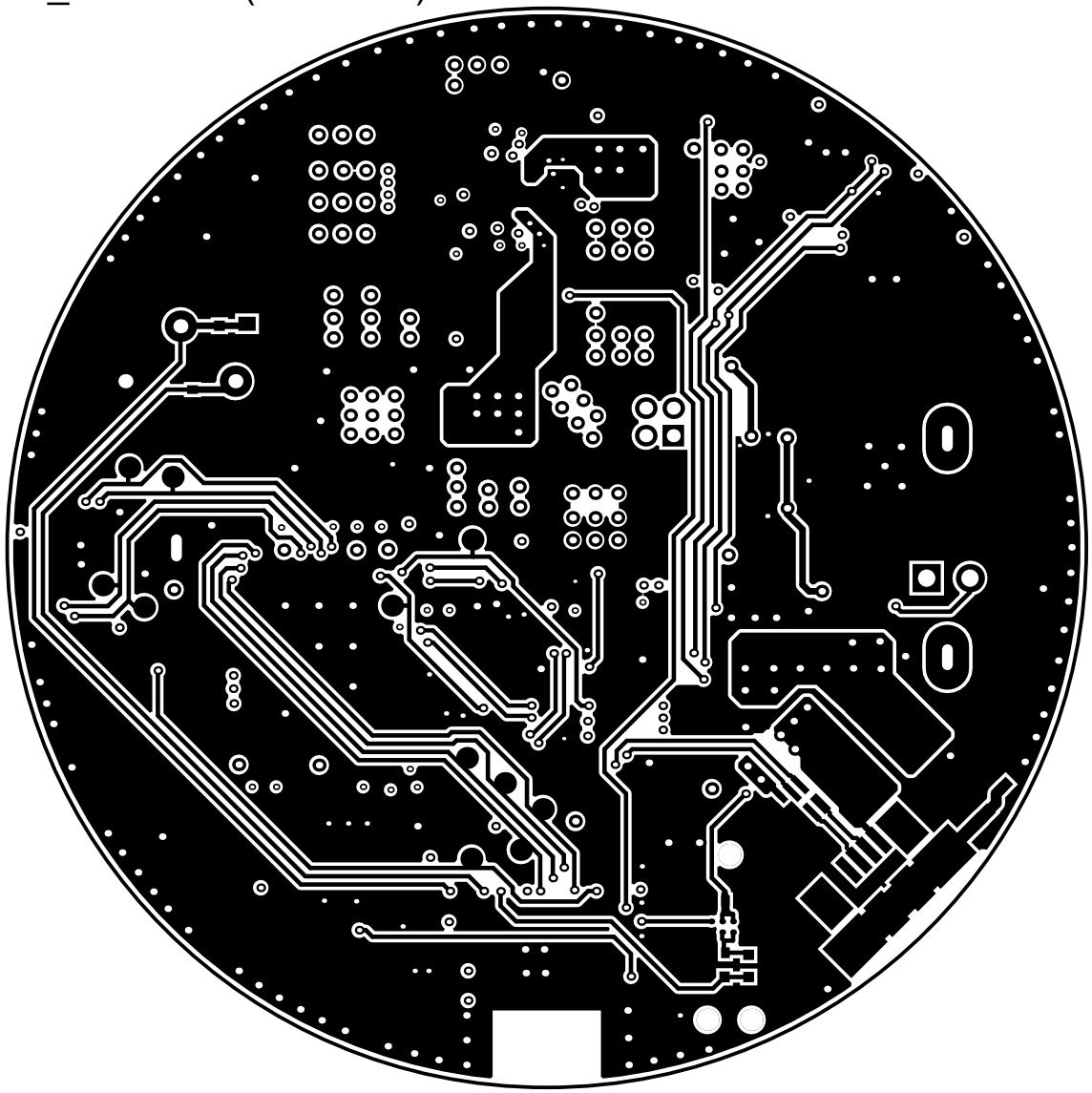
SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Internal signal layer/ground plane L2_GND		Fabrication document	Sheet 8 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
Repository revision: Not in repository control			

L3_PWR (Scale 3:1)



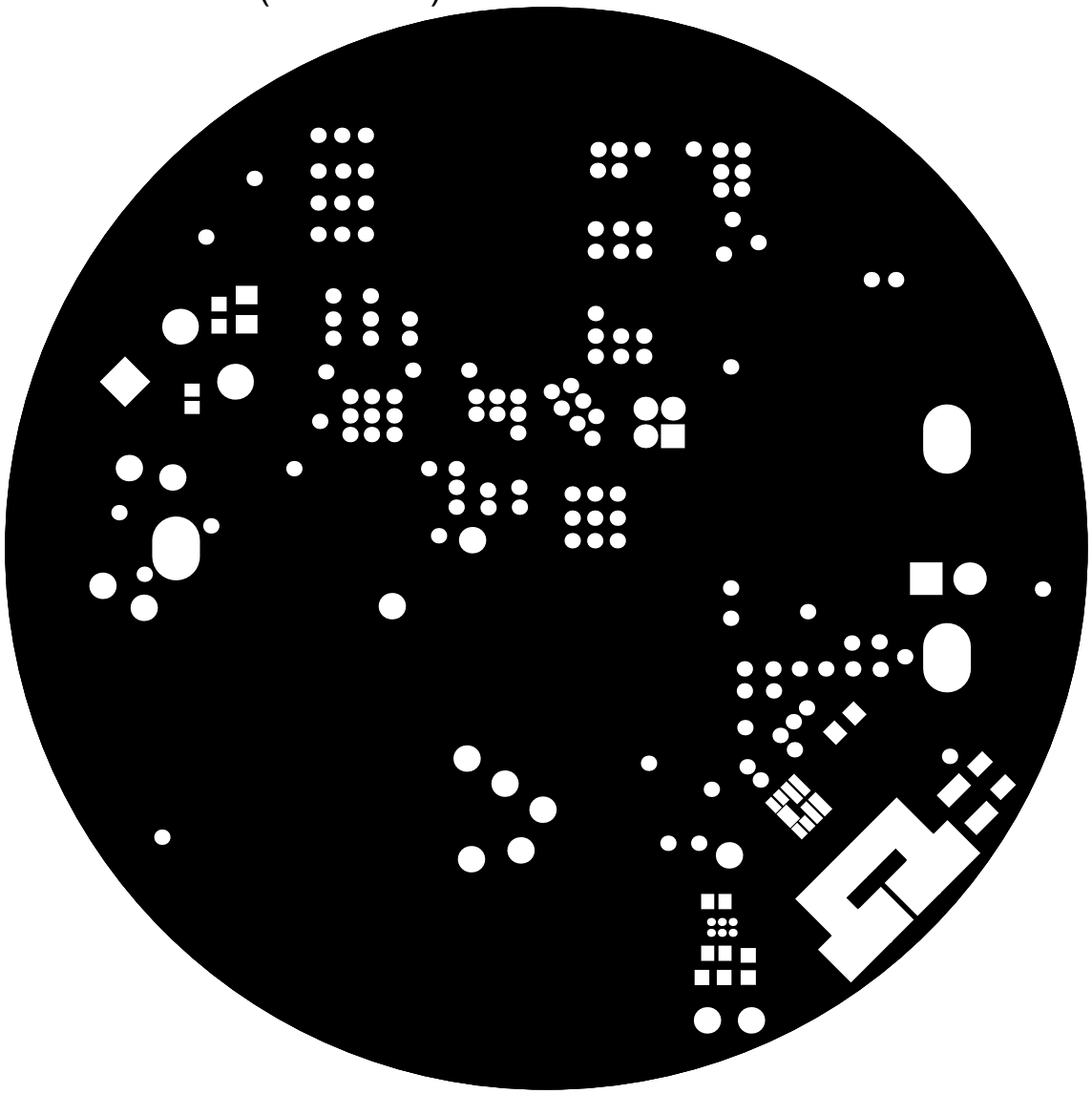
SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Internal power plane L3_PWR		Fabrication document	Sheet 9 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

L4_BOTTOM (Scale 3:1)



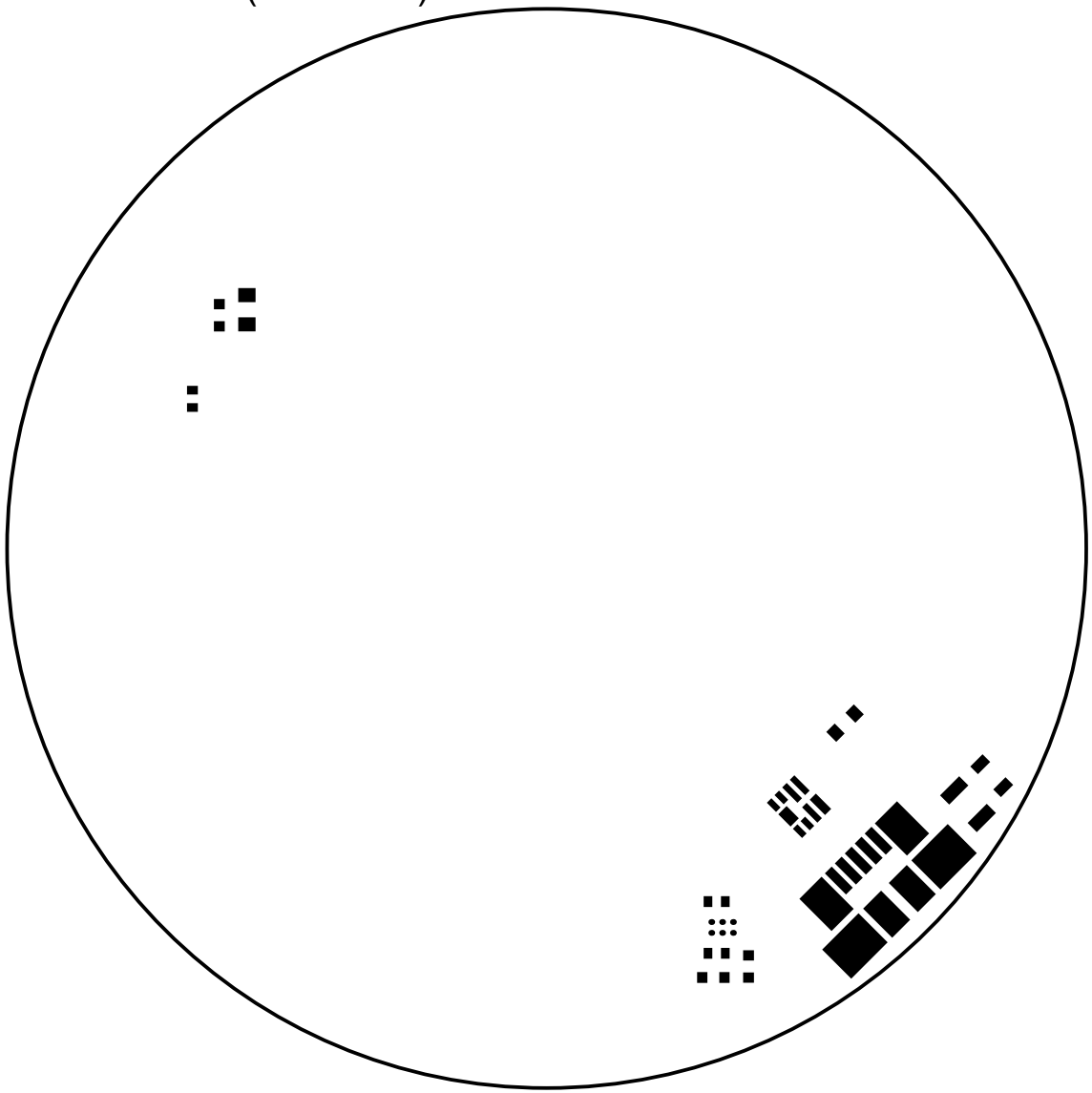
SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Layer L4_BOTTOM		Fabrication document	Sheet 10 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Bottom Solder (Scale 3:1)



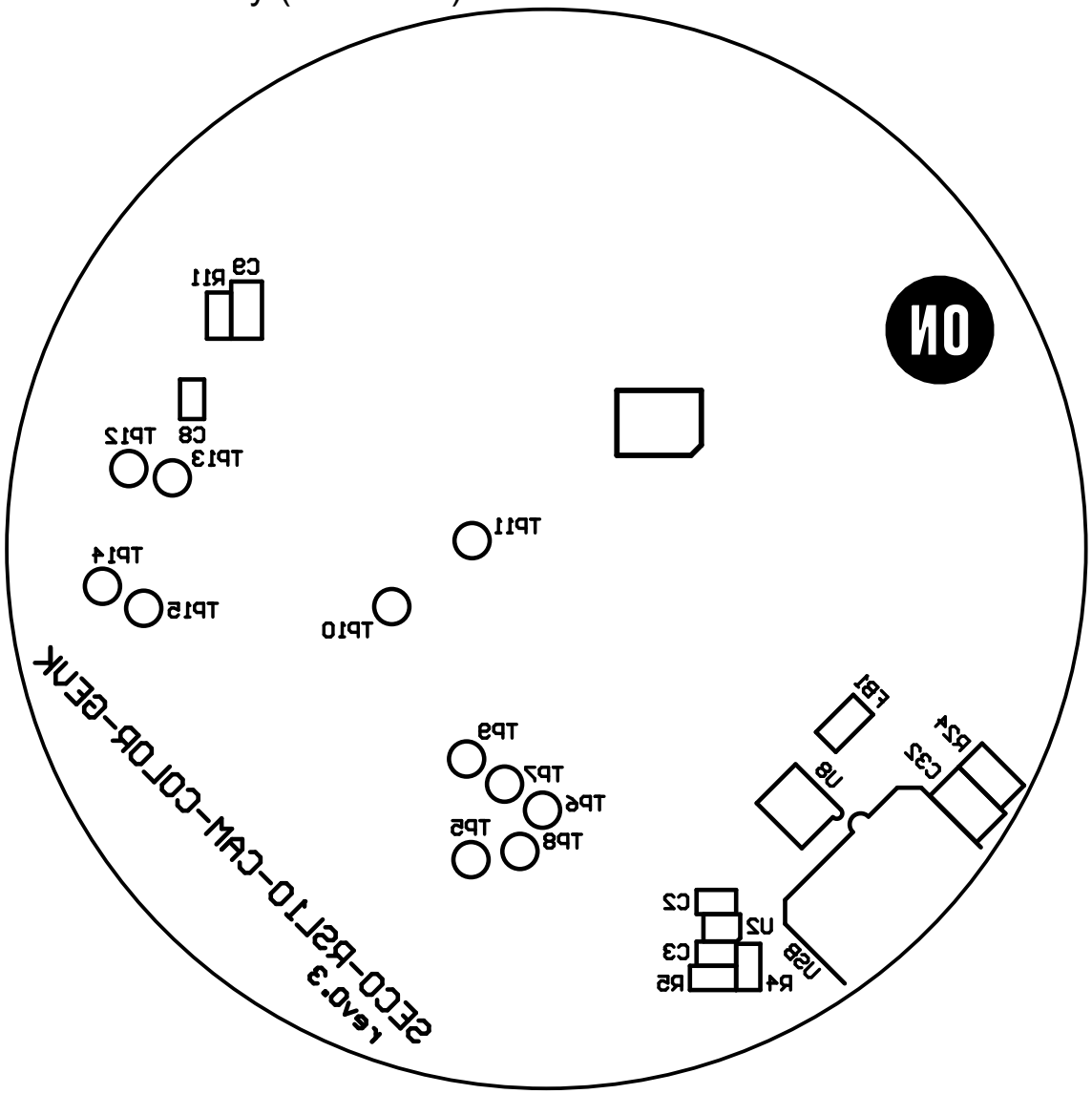
SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Bottom side solder mask		Fabrication document	Sheet 11 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Bottom Paste (Scale 3:1)



SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Bottom side solder paste		Fabrication document	Sheet 12 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Bottom Overlay (Scale 3:1)



SECO-RSL10-CAM-COLOR-GEVK		Revision: rev0.3	State: released
Bottom side silkscreen		Fabrication document	Sheet 13 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Drill Table - vias

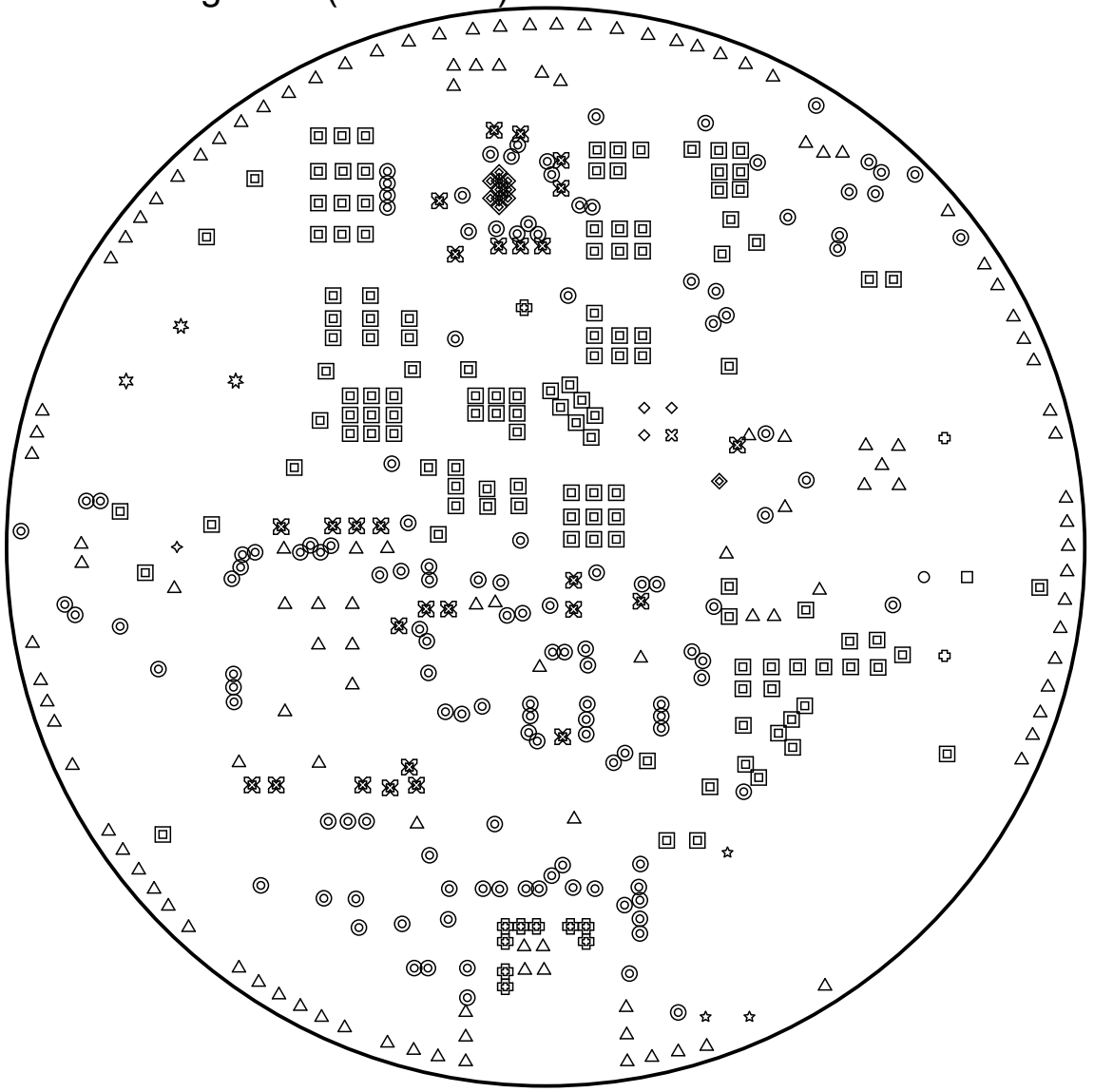
Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
	11	0.125mm(5mil)	Plated	L1_TOP - L2_GND	Via	v8h4_t
	27	0.152mm(6mil)	Plated	L1_TOP - L4_BOTTOM	Via	v12h6_t
	10	0.152mm(6mil)	Plated	L1_TOP - L2_GND	Via	v12h6_t
	132	0.203mm(8mil)	Plated	L1_TOP - L4_BOTTOM	Via	v16h8_t
	125	0.305mm(12mil)	Plated	L1_TOP - L4_BOTTOM	Via	v24h12_t
	130	0.305mm(12mil)	Plated	L1_TOP - L4_BOTTOM	Via	v24h12
	435 Total					

Drill Table - pads

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
	2	0.500mm(20mil)	Plated	L1_TOP - L4_BOTTOM	Pad	r300_200h50_120r100
	1	0.500mm(20mil)	Plated	L1_TOP - L4_BOTTOM	Pad	r275_200h50_125r100
	3	0.600mm(24mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c100h60
	1	0.600mm(24mil)	Plated	L1_TOP - L4_BOTTOM	Pad	s100h60
	1	0.650mm(26mil)	Plated	L1_TOP - L4_BOTTOM	Pad	s145h65
	2	0.650mm(26mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c145h65
	1	0.800mm(31mil)	Plated	L1_TOP - L4_BOTTOM	Pad	c130h80
	1	0.800mm(31mil)	Plated	L1_TOP - L4_BOTTOM	Pad	s130h80m140
	3	1.016mm(40mil)	Non-Plated	L1_TOP - L4_BOTTOM	Pad	c102hn102
	15 Total					

SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Drill tables		Fabrication document	Sheet 14 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			

Drill Drawing View (Scale 3:1)



SECO-RSL10-CAM-COLOR-GEVK		**Revision: rev0.3**	**State: released**
Drill drawing view		Fabrication document	Sheet 15 / 15
Engineer: T. Duris	Date: 18. March 2021		
PCB File: ULP_BLE_Camera.PcbDoc		**ON Semiconductor** Solution Engineering Center Piestany	
Repository revision: Not in repository control			