

- 1 Material: Isola IS400 or similar recommended
 - 2 Finish: ENIG (Electroless Nickel Immersion Gold), nickel layer $1 \div 4 \mu\text{m}$, gold layer $0.076 \div 0.2 \mu\text{m}$
 - 3 All gerber files generated as a top view
 - 4 Gerber files for internal power planes have to be inverted for manufacturing !
5. Fabricate according IPC-A-600
 6. Non-conductive epoxy ink recommended for silkscreen
 7. Silkscreen should not cover any exposed copper, silkscreen gerber data have to be trimmed eventually
 8. All holes diameter refer to final diameter after eventual plating

Gerber and drill file extensions table

Gerber files	Description
.GTO	Top side silkscreen
.GTP	Top side solder paste mask
.GTS	Top side solder mask
.GTL	L1_TOP - Top Layer
.GP1	L2_GND - Internal power plane - has to be inverted for manufacturing
.GP2	L3_PWR - Internal power plane - has to be inverted for manufacturing
.GBL	L4_BOTTOM - Bottom Layer
.GBS	Bottom side solder mask
.GBP	Bottom side solder paste mask
.GBO	Botom side silkscreen
.GM1	Board outline
Drill files	
.TXT	Layer pair L1_TOP to L4_BOTTOM Layer

IC_PAD		Revision: 0.1	State: in work
PCB fabrication notes and requirements		Fabrication document	Sheet 1 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
PCB File: ON_Semiconductor_2_sided_PCB.PcbDoc		<div>ON Semiconductor</div> <div>Solution Engineering Center Piestany</div> <div>ON</div>	
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Layer Stack

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.0356mm(1.400mil)		Signal	GTL
Core		1.6000mm(62.992mil)	FR-4	Dielectric	
Copper	Bottom Layer	0.0356mm(1.400mil)		Signal	GBL
Surface Material	Bottom Solder	0.0102mm(0.400mil)	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.6914mm(66.592mil)					

IC_PAD		Revision: 0.1	State: in work
Layer stack details		Fabrication document	Sheet 2 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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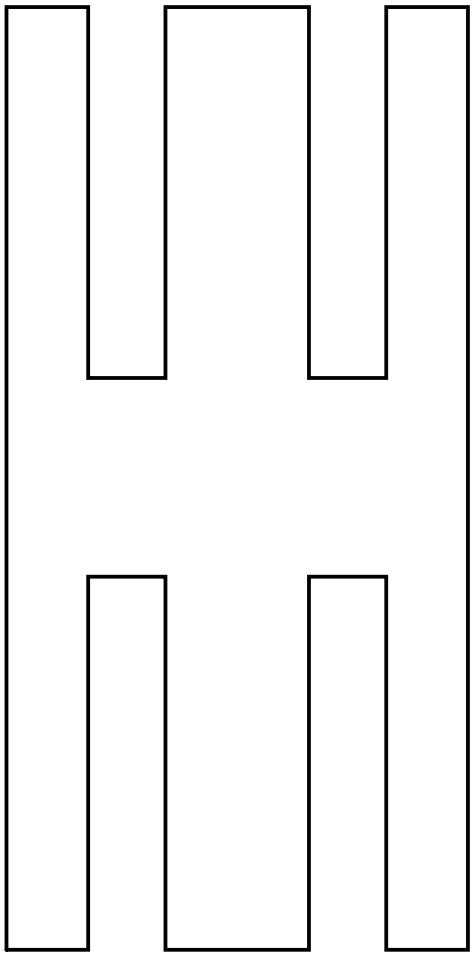
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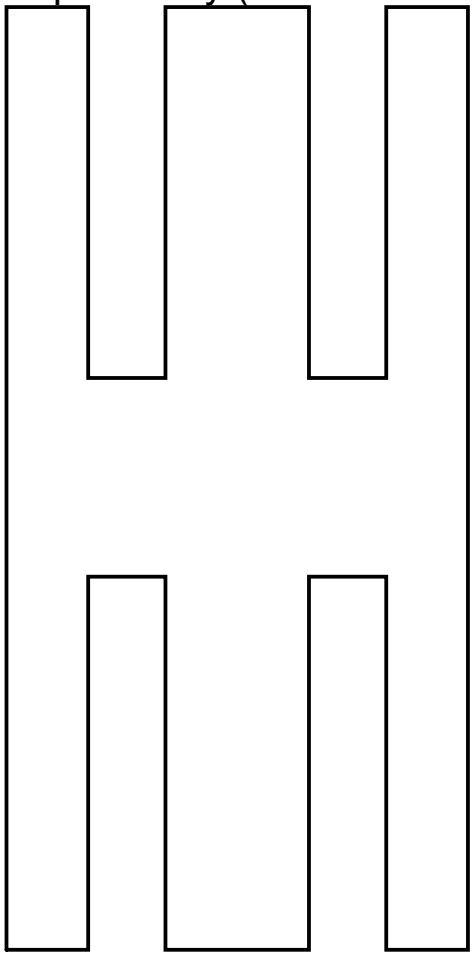
D



IC_PAD		Revision: 0.1	State: in work
Board outline definition - top view 2:3		Fabrication document	Sheet 3 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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Top Overlay (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Top side silkscreen - top view		Fabrication document	Sheet 4 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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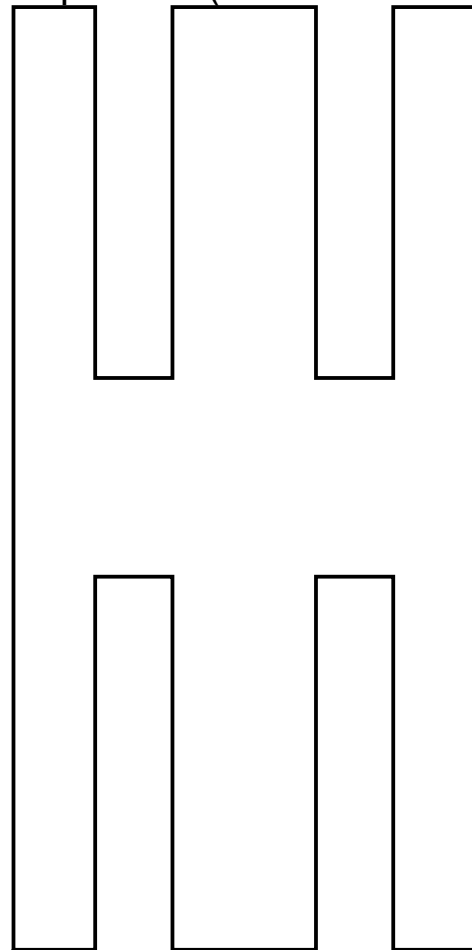
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Top Paste (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Top side solder paste - top view		Fabrication document	Sheet 5 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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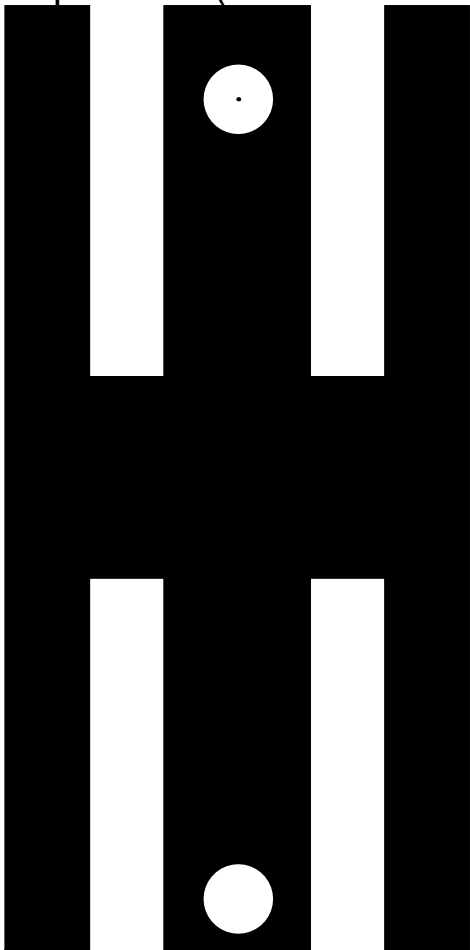
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Top Solder (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Top side solder mask - top view		Fabrication document	Sheet 6 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
PCB File: ON_Semiconductor_2_sided_PCB.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
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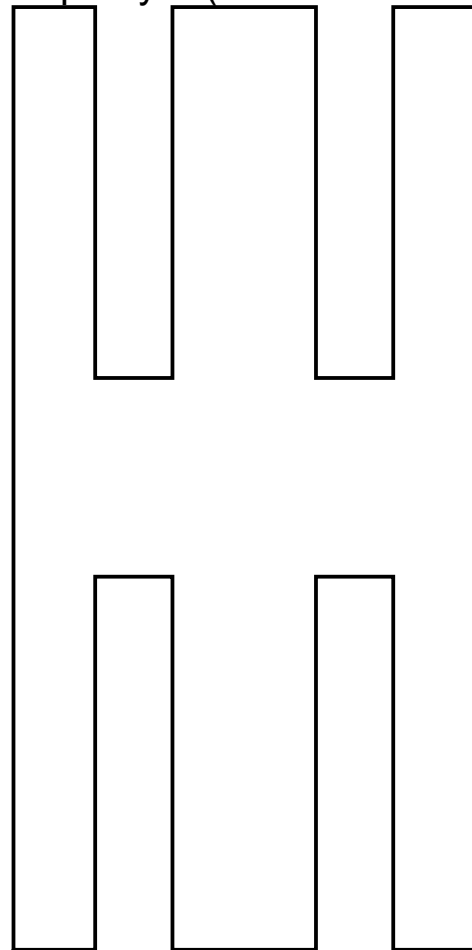
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Top Layer (Scale 2.29889298985168)



IC_PAD

Revision:
0.1

State:
in work

Top Layer - top view

Fabrication
document

Sheet
7 / 15

Engineer: zbjtdn

Date: ??.??? ???? ??:??

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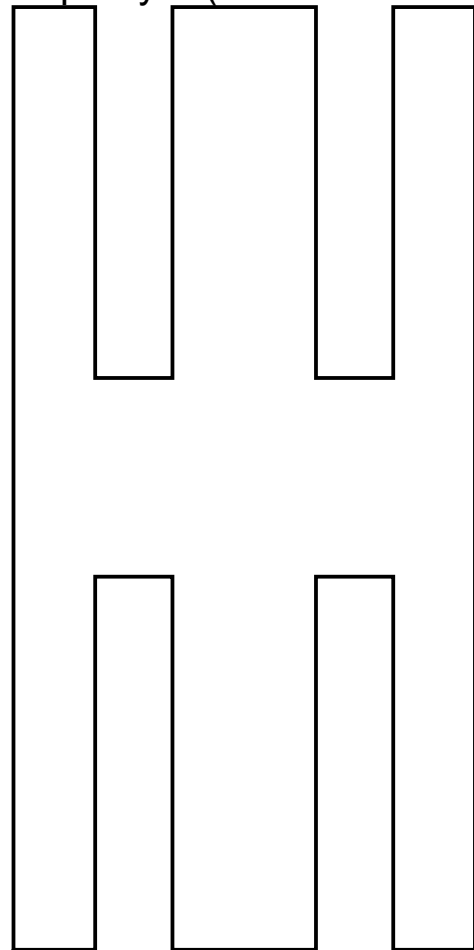
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Top Layer (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
L2_GND - internal power plane - top view		Fabrication document	Sheet 8 / 15
Engineer: zbjtdn	Date: ??:?? ???? ??:??		
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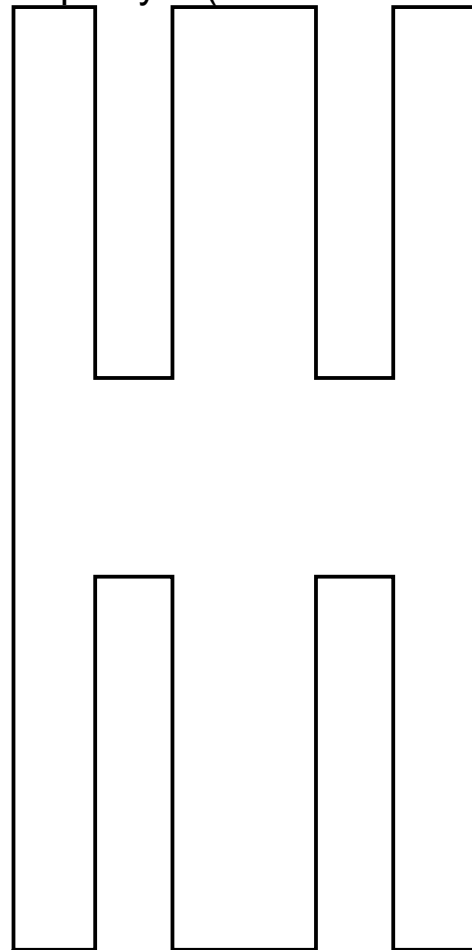
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Top Layer (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
L3_PWR - internal power plane - top view		Fabrication document	Sheet 9 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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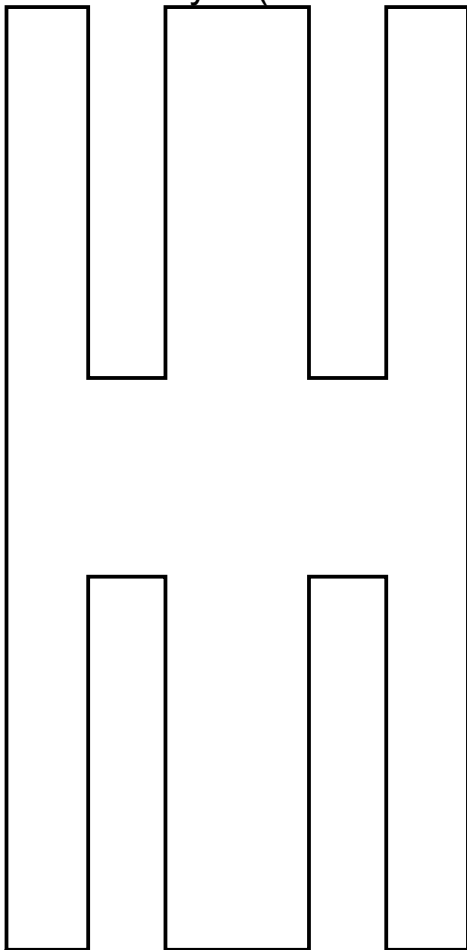
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Bottom Layer (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Bottom Layer - top view		Fabrication document	Sheet 10 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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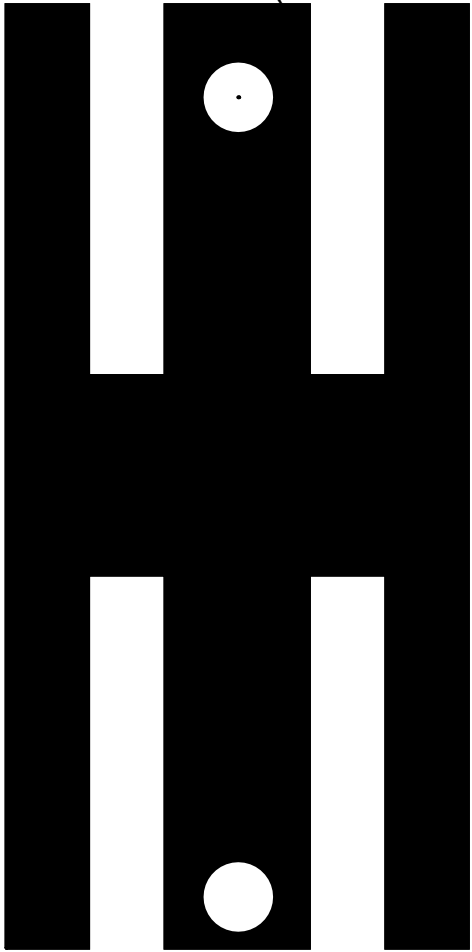
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Bottom Solder (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Bottom side solder mask - top view		Fabrication document	Sheet 11 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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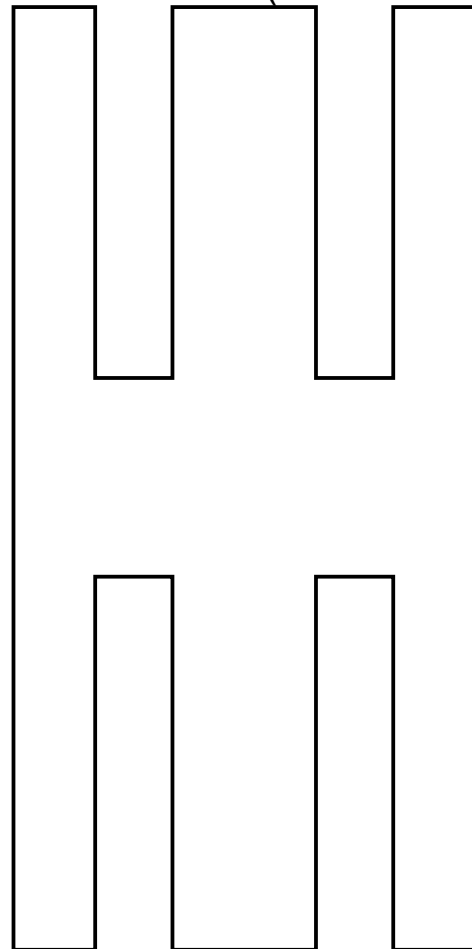
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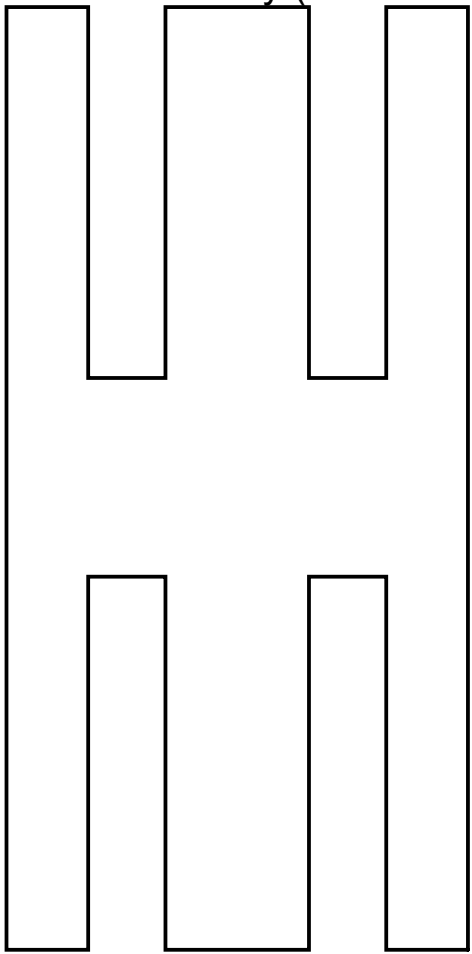
Bottom Paste (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Bottom side solder paste - top view		Fabrication document	Sheet 12 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
PCB File: ON_Semiconductor_2_sided_PCB.PcbDoc		ON Semiconductor Solution Engineering Center Piestany	
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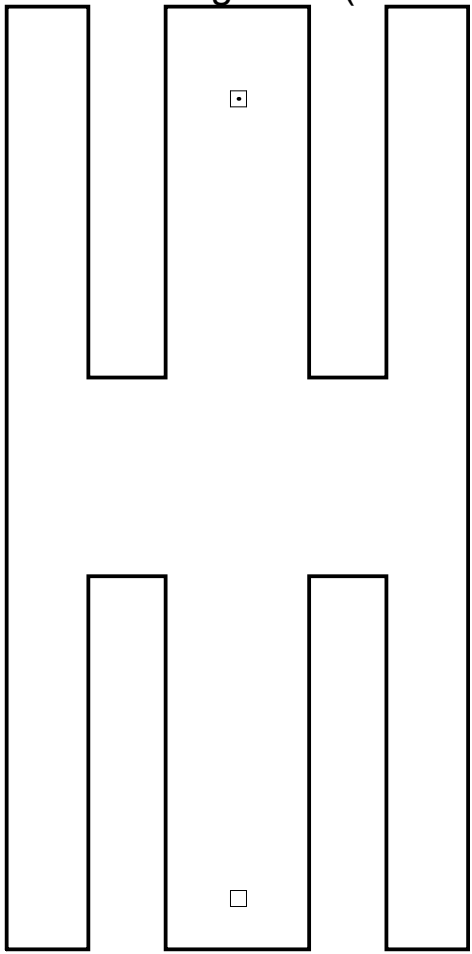
Bottom Overlay (Scale 2.29889298985168)



IC_PAD		Revision: 0.1	State: in work
Bottom side silkscreen - bottom view		Fabrication document	Sheet 13 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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Drill Drawing View (Scale 2.29889298985168)




9 Related drill table can be found on page 15


IC_PAD		Revision: 0.1	State: in work
Drill drawing		Fabrication document	Sheet 14 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad	Template
	2	4.000mm(157.5mil)	Non-Plated	Top Layer - Bottom Layer	Pad	(Mixed)
	2 Total					

⑩ Related drill drawing can be found on page 14

IC_PAD		Revision: 0.1	State: in work
Drill table		Fabrication document	Sheet 15 / 15
Engineer: zbjtdn	Date: ??.??? ???? ??:??		
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