MODELING CAPACITANCES OF A VERTICAL RF POWER TRANSISTOR

W. Cai[1], B. Gogoi[1], R.B. Davies[1], D. Lutz[1], G. Loechelt[2], G. Grivna[2]
[1]HVVi Semiconductors, Phoenix, AZ, [2]ON Semiconductor, Phoenix, AZ

***Abstract* — This paper addresses the device physics of a novel vertical power MOSFET through detailed TCAD simulation. The simulated I-V and C-V characteristics match well with the measured data. The bias dependence of electrical potential near the recess trench is identified as the cause of a sharp drop in output capacitance against drain voltage.**

***Index Terms* — power MOSFET, output capacitance, TCAD**

I. INTRODUCTION

A novel sidewall-gate, vertical power MOSFET with backside drain contact has been demonstrated which achieves minimal gate-to-drain capacitance [1]. In addition, a recess trench region is formed in the n-drift region, in which a silicided polysilicon layer residing on a thick oxide serves as a shield and is used to optimize the RDSon and breakdown voltage relationship. As a result, a lower gate-drain capacitance has been achieved than any competitive power MOSFETs with similar voltage ranking.

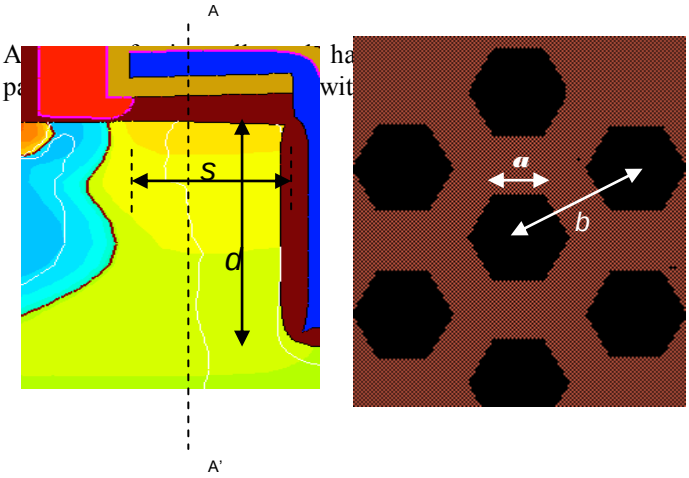


Fig. 1 Schematic cross-section and layout of power MOSFET with hexagonal symmetry. The poly-Si in the trench is also grounded and serves as a shield. The parameters *d* and *s* refer to the depth of the trench and separation between the trench and dielectric sidewall. The vertical cutline A-A' is used to monitor the extent of depletion as a function of drain bias.

II. EXPERIMENTAL DETAILS

The starting material consists of 10um-thick n-type epilayer on a heavily arsenic-doped Si (100) substrate. Ion implantation is used to introduce extra surface dopant to further reduce on-resistance. The source and gate electrodes are contacted from the top surface to achieve minimal source inductance and maximal heat transfer capability, and the drain is contacted from the backside after wafer thinning. Details of the fabrication process can be found in [1, 2].

As shown in Fig. 1, hexagonal-shaped holes (with a typical "porosity" factor in the range of 30-70%) were etched using Reactive Ion Etching within a sheet of dielectric layers. After the p-tub implantation that is self-aligned with respect to the edge of the hexagonal holes, a 200Å-thick gate oxide was formed at the exposed Si surface, followed by the deposition of an in-situ doped poly both on the flat surface as well as along the 90°-sidewall. The channel of the FET resides along the periphery of the hexagons with an estimated gate length of about 0.25 um.

III. RESULTS AND DISCUSSIONS

2D process and device simulations were performed on the device structure described in Section II. The Philips mobility model was used owing to its accuracy in modeling velocity saturation, and doping and temperature dependencies of mobility. The Lucent implementation of the Lombardi's formula was used to model mobility degradation due to surface roughness and acoustic phonon scattering.

A. Current-Voltage Characteristics

Fig. 2 (a) compares the measured (symbol) and simulated (line) I_d - V_{ds} curves for a constant gate biases (V_{gs}) that steps from 1.6 to 3.4V at T_{base}=300K. The negative differential resistance observed under high V_{gs} is due to device self-heating. Fig. 2 (b) shows a good agreement between the measured (symbol) and simulated (line) 300K transfer curves at V_{gs} =5V. Isothermal approximation can be justified here due to the negligible self-heating at low biases.

B. Capacitance-Voltage Characteristics

Fig. 3 plots the measured and simulated Coss and Ciss against bias voltages. With gate grounded, Coss for V_{ds} less than 4V is determined by the vertical doping profile in the n-drift region near the surface. Coss for V_{ds} >10V, on the other hand, is dominated by depletion of the n-epilayer. Furthermore, simulation correctly predicts the presence of a transition region (V_{tran} ~5V), though the simulated drop rate of Coss is much sharper than the measured data. The gradual slope of measured Coss in the transition region may be explained by the enhanced Debye length and excessive dopant diffusion.

To elucidate the cause for the steep drop in Coss at V_{tran}, we plot in Fig. 4 the evolution of equal-potential lines at V_{gs} =0 for different V_{ds}. Away from the junctions, the equal-potential lines are flat, supporting the fact these devices have an off-state breakdown voltage of greater than 120V. The white lines in these contour plots indicate the depletion boundary. Comparing the equal-potential lines for the two lowest biases shown here, we find that at 3.75V, the region sandwiched between the p-tub and trench is not fully depleted. It becomes fully depleted only at V_{ds} higher than 7.5V. For intermediate values of V_{ds}, the propagation of depletion boundary is strongly influenced by the large doping gradient in the region sandwiched between the p-tub and the trench, therefore causing the steep drop in Coss.

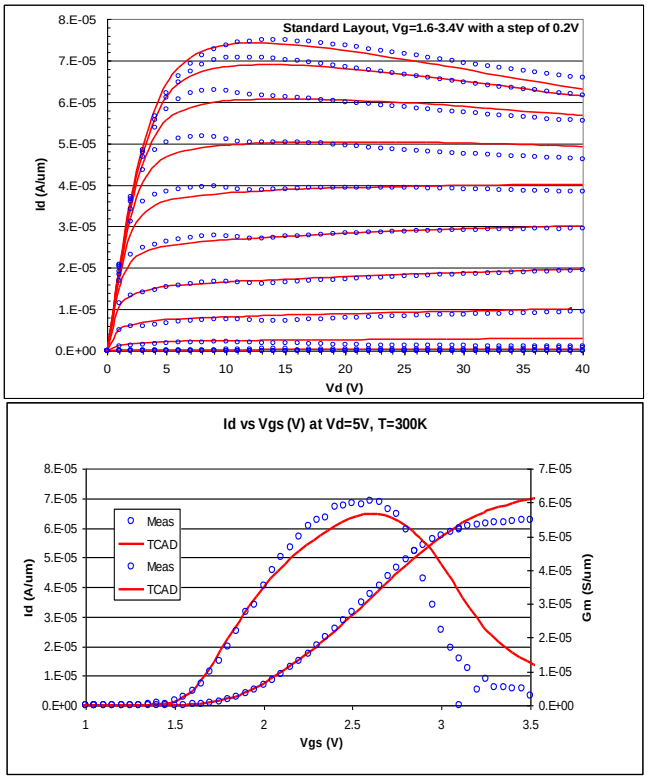


Fig. 2 Measured (symbol) and simulated (line) I-V characteristics at T_{base}=300K for the standard layout. (a) Id-Vd family curves) with Vgs=1.6 to 3.4V in 0.2V step. (b) Id-Vgs with Vds=5V.

To further confirm the mechanism responsible for the observed behavior of Coss, simulations were carried for two additional layouts. Fig. 5 plots Coss for these three devices. We find that the transition shifts to higher voltage as *s* increases. As expected, the three curves approach the same asymptotic limit for very large or very small V_{ds}.

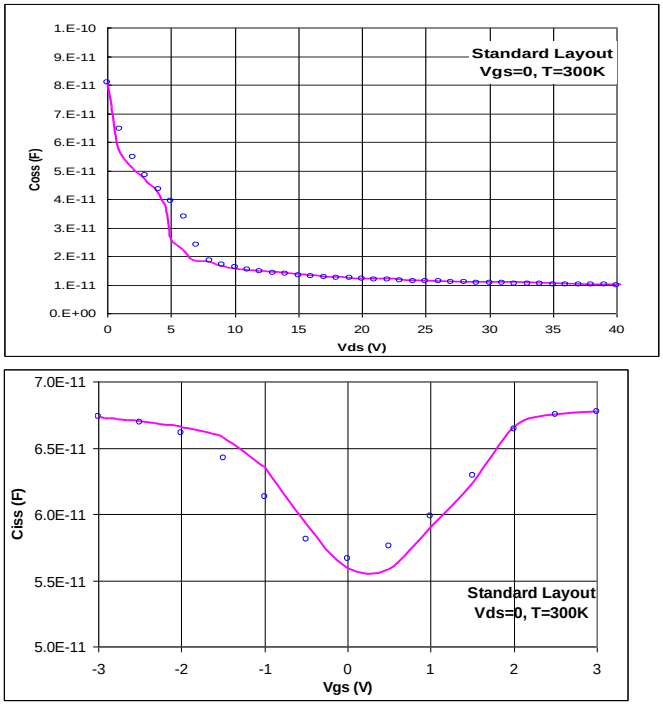


Fig. 3 Measured (symbol) and simulated (line) C-V characteristics for the standard layout (case A) (a) Coss vs. Vds with Vgs=0, and

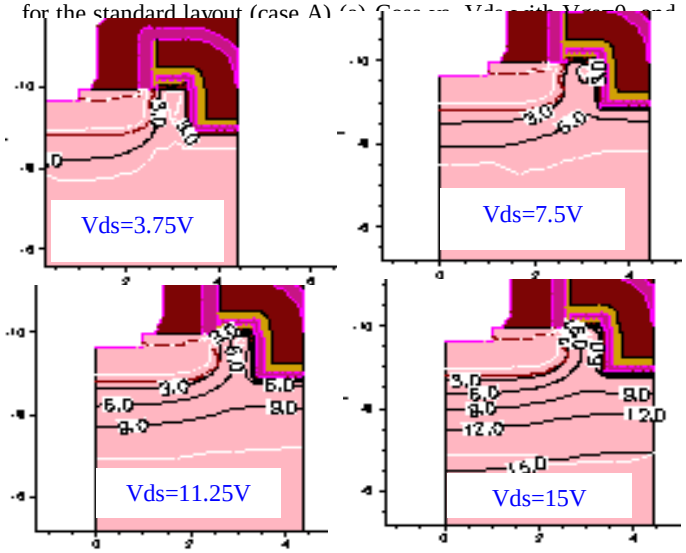


Fig. 4 Simulated electrostatic potential for the standard layout (case A) at Vgs=0 and Vds=3.75, 7.5, 11.25, 15V. The labels (from 0 to 15V in 3V step) on the lines refer to the values of the electrostatic potential. The white lines indicate the depletion boundaries.

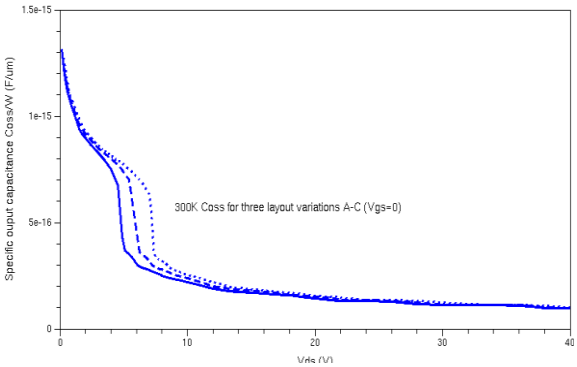
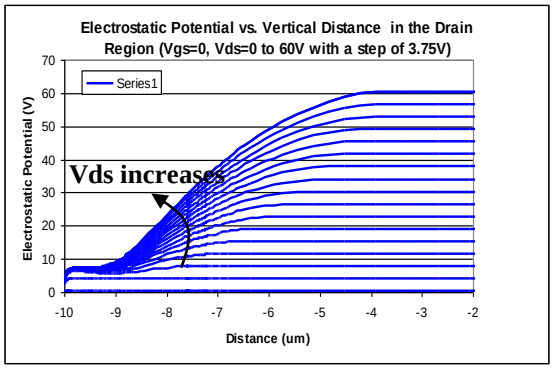
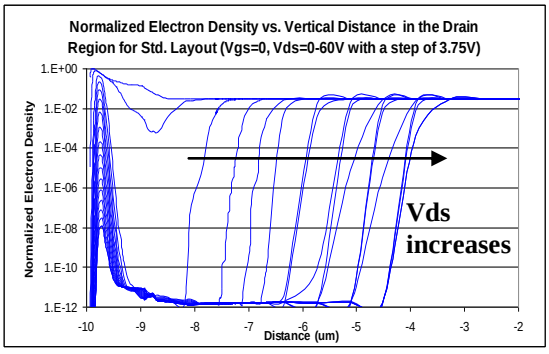


Fig. 5 Simulated Coss-V_{ds} characteristics for devices with varying dimension *s*, as defined in Fig. 1. Cases A-C correspond to *s* with values as Standard (solid), Standard+0.1um (dashed), and Standard+0.2um (dotted), where V_{tran} occurs at 5, 6, 7V, respectively. V_{gs} is set at 0V for the simulation.





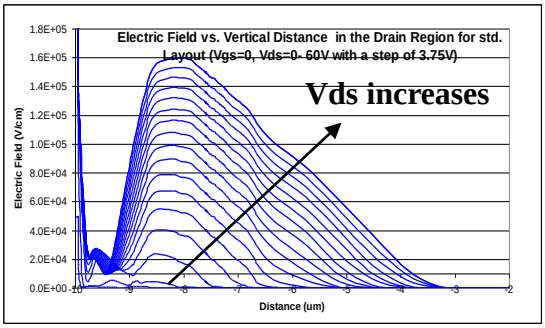


Fig. 6 (a) Electrostatic potential, (b) electron density, (c) electrical field along the vertical cutline A-A' in the n-drift region for the standard layout.

Fig. 6 plots the coordinate-dependence of the electrostatic potential, electron density, and electrical field along the 1D cutline A-A' as depicted in Fig. 1. V_{ds} is stepped from 0 to 60V in 4V step. We find that between the gate oxide/Si interface, which is situated at y= -9.97um, and y= -9 um, the electrostatic potential is essentially pinned at ~8V. The pinning potential is attributed to the field shaping capability of the L-shaped shield. Also, 60V drain bias does not fully deplete the n-epilayer, leaving potentials for operation at even higher V_{ds}.

V. Conclusions

We have demonstrated a novel vertical power MOSFET that has extremely low feedback capacitance due to implementation of an intrinsic shield and self aligned body junction. Very good matching of I-V and C-V curves is achieved between measurement and TCAD simulation. We have shown using simulation that the steep change of rate of decrease in Coss near V_{ds} =5V is due to propagation of depletion boundary into the n-drift region. The steep drop in Coss is attributed to the large doping gradient.

References

[1] Brian Battaglia, Walt Wright, Robert Neeley, and Bishnu Gogoi, "High performance vertical MOSFET technology enables phased array radar applications," *Proceedings of the 2008 European Microwave Conference*, Amsterdam, Netherlands, Nov. 2008.

[2] B. Gogoi, et al. accepted by IMS 2009

[3] Annemarie Aarts, Nele D'Halleweyn, and Ronald van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Trans. Electron Devices*, Vol. 52, No. 5, pp. 999-May 2005.

[4] A. Aarts, R. van Langevelde, J. C. J. Paasschens, A. J. Scholten, M. B. Willemsen, and D. B. M. Klaassen, "New fundamental insights onto capacitance modeling of laterally nonuniform MOS devices," *IEEE Trans. Electron Devices*, Vol. 53, No. 2, pp. 270-278, Feb. 2006.

[4] M. Y. Hong and D. A. Antoniadis, Theoretical analysis and modeling of submicron channel length DMOS transistors, *IEEE Trans. Electron Devices*, Vol. 42, No. 9, , Sep. 1995, pp. 1614–1622.

[5] Hsin-Hui Hu, Kun-Ming Chen, Guo-Wei Huang, Ming-Yi Chen, E. Cheng, Yu-Chi Yang, Chun-Yen Chang, Temperature-Dependent Capacitance Characteristics of RF LDMOS Transistors With Different Layout Structures, *IEEE Electron Device Letters*, Vol. 29, Issue 7, July 2008 pp. 784 – 787.

[6] M. D. Dawish, et al. *IEEE Trans. Electron Devices*, Vol. 44, No. 9, Sept. 1997, p1529-1538.