

## Description

AIP301 is a Total Ionizing Dose (TID) tolerant and Single Event Latch-Up (SEL) immune Digital Gate Library implemented in ON Semiconductor ONC18 process technology. ONC18 provides 180nm 1.8V CMOS with a number of variants to support analog, mixed-signal and dual gate oxide. The library is usable in most ON Semiconductor ONC18 process variants extending the library's use to a large number of applications.

The library utilizes radiation hardened by design (RHBD) layout techniques to improve TID performance well beyond ONC18 inherent performance and ensure latch-up immunity. Dual active contacts and interconnect vias are used to ensure high reliability.

For the best density possible, the library utilizes an enclosed drain RHBD technique for the NMOS poly gate. Anatrix offers a digital cell library, AIP302s, with higher cell density but lower TID performance.

The library contains the following views: schematic, symbol, layout, verilog, .lib, .lef and netlist.

## Applications

- Programs with greater than 300KRad TID
- SEL immunity requirements
- HiRel Products requiring redundant contacts
- Verilog and Behavioral Designs
- Custom Digital Functional Blocks
- Analog/Mixed-Signal/RF Control Logic
- Place and Route Digital Blocks

## Features

- Total Ionizing Dose Tolerant over 300KRad
- Single Event Latch-Up Immune
- 2.5X area penalty vs standard gates
- High reliability design rules
- Place and Route Capable
- 300pS Clock to Q DFF

## Logic Gates Included

1X and 2X drive:

AND2, AND3, AND4  
NAND2, NAND3, NAND4  
OR2, OR3, OR4,  
NOR2, NOR3, NOR4  
XOR2, XNOR2  
MUX2  
AOI22  
OAI22  
ADDH, ADDF  
DFF, DFFR, DFFSB, DFFE

1X, 2X, 3X, 4X, 6X, 8X, 12X, 16X, 20X drive:

INV  
BUF

Support Cells:

Antenna diode  
TieHigh, TieLow  
FILLER (1, 2, 4, 8, 16, 32, 64 track widths)  
CAP\_FILLER (2, 3, 4, 8, 16, 32, 64 track widths)

## Contact Us

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