Eliminating a Polysilicon Hole Defect Created During Oxide Removal

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***Abstract*— Gate Oxide failure analysis during technology qualification led to discovery of the polysilicon hole defects in large (>200K μm^2) PMOS capacitors. In-line KLA inspections confirmed that polysilicon holes were formed during the salicide block process module. It is hypothesized that a three way interaction between the P+ source/drain implanted boron, heat added during salicide block mask deposition, and NH_4+ in the BOE causes the polysilicon hole. By replacing the BOE (Buffered Oxide Etchant) with a 100:1 HF solution, the creation of polysilicon holes was eliminated as confirmed by KLA and VBD testing.**

Keywords-: polysilicon void defects, GOI, Boron implant, Salicide block module, BOE

I. INTRODUCTION

Gate oxide failures are one of the major contributors to the reliability and yield loss of semiconductor devices. While most gate oxide issues are created within the gate oxide module, this paper will demonstrate that post gate processing can contribute to gate oxide defects. Specifically, defects formed during the salicide block module on polysilicon; a module that serves as a hard mask for selective salicide formation.

An in depth investigation revealed that failing gate oxide test results were due to polysilicon holes that formed in the salicide block module, during the pre-metal-deposition cleans. Subsequent silicide formation in the polysilicon hole caused electrical shorts. While not directly related to inherent oxide quality, the failures appeared as extrinsic gate oxide defectivity.

II. ISSUES AND IDENTIFICATION

As part of a high voltage 0.35um technology qualification, gate oxide integrity tests including TDDB and VBD were performed. TDDB and VBD tests showed that PMOS GOI capacitors exhibited high failure rates on PCSQ1 (large square active area), PCPE1 (poly edge) and PCBB1 (Birds Beak) structures, while all complimentary NMOS structures were relatively defect free. Data analysis indicated that the failures were Type-A extrinsic defects in nature. Excluding these failures otherwise indicated that the intrinsic lifetime for the gate oxide met the 10 year requirements. Table 1 outlines the test structure types, its dimensions, and it failure rate.

Table 1: Oxide qualification module

Structure Name and Size	PCSQ1	PCPE1	PCBB1
Active Area (um^2)	243,000	243,000	243,000
Edge length (um)	PE: 0 FE: 2,070	PE: 194,400 FE: 720	PE: 0 FE: 195,120
# of Defect (out of 116 caps)	15	28	41

FA (Failure analysis) by photo emission, SEM review, and SEM cross sections showed a round hole in the polysilicon top plate. These polysilicon holes were completely void of polysilicon and typically showed titanium silicide on the sidewalls and hole bottom. Figure 1 and 2 shows a typical appearance of these defects.

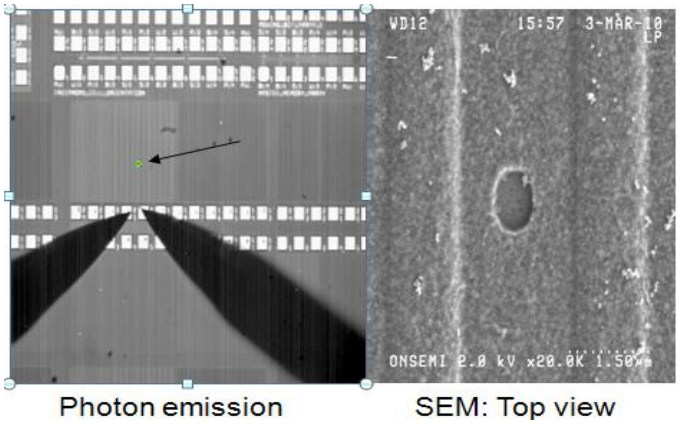

Figure 1: Failure analysis work by ONSEMI

Figure 2: Polysilicon hole with Ti-silicide formation at the bottom of the hole.

Based upon the FA results, in-line product scans were intensified in the manufacturing line using a KLA2132 Brightfield wafer scan tool. The focus of these scans was in the salicide block module, as listed in Table 2.

Table 2: Salicide block processing module

Process Steps	Comments
SiO2 depsotion	LPCVD TEOS
Si3N4 deposition	LPCVD
Patterning / etch / ash / clean	
Pre-metal clean	BOE wet clean
Ti deposition	Endura deposition
TiSi formation	RTP
Ti Strip	SC1 strip

Stepwise scan recipes were developed to determine where in the salicide block processing module that the defect type was first formed. For these inline scans, a relative visual Defect Density (D_0) was determine through review of the defects found with KLA scans. D_0 is defined as number defects per square centimeter of area scanned. Through the in-line scans, the polysilicon defect was determined to be first detected after pre-metal clean. This clean is used to remove any native oxide prior to Ti deposition and can be considered as primary process step in the creation of polysilicon hole defects. With this discovery, additional experiments were performed to identify contributing factors to the defect formation and to understand the mechanism of polysilicon hole formation.

III. Contributing Factors Experiments

A short-loop flow was created based on salicide block module utilizing patterned implanted wafers. With the short-loop flow wafers, many experiments were designed to find the root cause for the defect of interest. Below are summaries of the important experiments that lead to determining a root cause for the polysilicon holes defects. All experiment results are based on visual defect counts.

A. Implant damage

One theory to the defect formation was that the P+ implant is physically damaging the poly-silicon and allowing the pre-metal clean to remove the damaged poly-silicon. An experiment designed to test this theory used B, BF2, and Ar as implant species with same dose and energy condition as the standard P+ source/drain implant used by the technology. The inert Argon gas was chosen to only study the physical damage effect of an implant on the polysilicon. Table 2 summarizes of the visual D_0 for the implant damage theory experiment.

Table 2: Effect of implant on polysilicon holes

	POE (BF2)	B	Ar only	B+Ar
Overall KLA visual defect counts	88	271	2.2	561
Polysilicon visual defect counts	70	211	0	505

The DOE results showed that any Boron base implant produced polysilicon holes, while Ar did not produced any holes.

B. Plasma charge damage

The second theory investigated was whether the P+ source/drain implant conditions were the initiator of the problem. Specifically, it was hypothesized that implant recipe arc current was too high and thus caused some type of ESD damage to the polysilicon which was later enlarged via the pre-metal clean. For this experiment, the arc current was varied to produce poor electron neutralization conditions with results are shown in Figure 3.

Scans showed that a polysilicon hole like defect was created, but differed in characteristic from the defect under study. The defect not only formed in the polysilicon but also in the Si substrate in the case of high arc current. Also the created defect had the appearance of a typical electrical discharge, and thus was not circular in nature. From these observations, it was thus concluded that the polysilicon hole defects were not due to wafer charging during ion implantation.

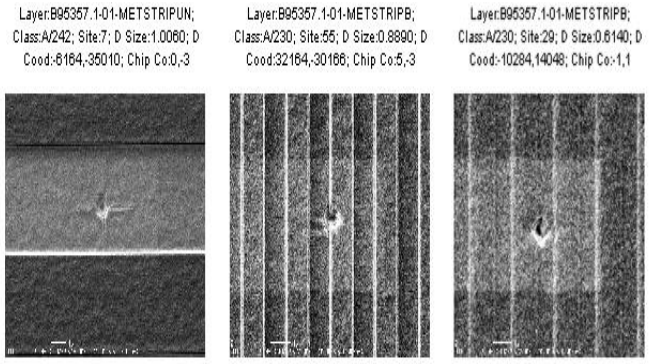

Figure 3: Implant charging damage defects at high arc current.

C. Pre-metal clean chemical

As KLA scans indicated that the polysilicon hole defects first appeared following the pre-metal clean, an experiment was centered around the clean conditions. The process of record pre-metal clean used a BOE based clean in order to remove native oxide prior to titanium deposition. An alternative of a 100:1 HF solution was proposed. A split was performed between these two chemicals and the resultant D_0 is shown in table 3. A significant reduction of polysilicon hole with HF was observed.

Table 3 Pre-metal Cleans

	HF	BOE
Overall KLA visual defect counts	6.5	105
Polysilicon visual defect counts	0	105

D. *LPCVD vs PECVD vs HDP films*

Summer F.C from SMIC claimed that silicon rich oxide with RI (refractive index) of 1.56 when used as hard mask for selective salicidation, also prevents polysilicon hole generation.[1] To determine if this was the case, a short-loop experiment was designed to test SiO_2 deposition method. In current process, both a SiO_2 (TEOS generated) and Si_3N_4 are used to form the salicide blocking mask. For this test, both LPCVD, PECVD and HDP oxide films and LPCVD, and PECVD nitride films were studied. The PECVD films employed standard operation condition as other intra-metal dielectric films used in the FAB, while the HDP wafer received a SiO_2 film having a Refractive index of 1.56. Table 4 shows defect density for this DOE. From the results it can be concluded that the HDP silicon rich film is capable of controlling the generation of the polysilicon hole defects but not to the same level as seen by changing the pre-metal cleans chemistry.

Table 4: Thermal budget and HDP experiment result.

	POE	HDP (Si Rich- RI of 1.56)	HDP + RTA	PECVD TEOS	PECVD TEOS + RTA	PECVD SiN	SiN removed via Hot Phos
Overall KLA visual defect counts	88	4.47	2.5	184	23.4	26	139
Polysilicon visual defect counts	70	3.6	2.1	184	23	26	125

E. *Different salicide block module*

The fact that there are salicide block module integration differences between 0.35µm processes in our FAB was noted. In-line and electrical testing that one integration scheme did not have the polysilicon hole defects while the other did. The major difference was that salicide block module included a Si_3N_4 layer on the process that had the polysilicon hole defects. A short-loop experiment was again used to determine if the factor was Si_3N_4 or other previous processing differences between the two flows. Splits were done around the salicide block module steps. Table 5 shows no defect creation when the Si_3N_4 layer is omitted from the flow.

Table 5: Salicide block module integration difference.

	POE	Thicker TEOS	Extened TEOS dep	No SiN layer	No SiN with BOE	STD with HF
Overall KLA visual defect counts	146	73	143	14	24	6.7
Polysilicon visual defect counts	146	43	143	0	0	0

IV. DISSCUSION AND RESULTS

Several hypothesis tests were developed based upon known failure mechanisms in an effort to resolve and understand the polysilicon hole defect issue. These hypotheses ranged from metal enhanced pitting of Si in HF solutions[2] to grain boundary enhanced HF etching. However, no known failure mechanisms completely explained the observed polysilicon hole defects. As a results, additional hypothesis test were performed internally. Many tests resulted in more questions, but several provided insight into the polysilicon hole formation mechanism.

From the observation that only the PMOS capacitor structures were impacted by this defect and later confirmation with ion implantation splits, it was determined that boron is a key component in this defect formation. From splits performed at the pre-metal clean, it was shown that BOE solution was a major factor. Additionally, by changing the salicide block integration and film stochiometry, the defects were modulated. This last result can be explained by a polysilicon grain boundary stuffing as hypothesized by Summer F.C, changes to film stress, or changes to the wafer thermal budget.

With these results, the authors hypothesize that the polysilicon hole defects arise from three way interaction between boron implant in polysilicon, subsequent thermal processing, and the BOE chemistry. During the salicide block depositions, the boron agglomerated in the implanted polysilicon due to the thermal energy in the LPVD deposition steps. This aggregated boron-rich-silicon is then etched by the BOE etch chemistry yielding a polysilicon hole defect. It remains unknown what property of BOE (vs HF) allows for this phenomenon: the difference in pH or the NH_4F in BOE solution. Further characterization is required to confirm this hypothesis and to understand the mechanism.

While the mechanism remains unknown, the solution of replacing the BOE based pre-metal clean with a 100:1 HF based pre-clean was implemented. Following implementation of this new pre-metal clean, no polysilicon hole defects have been detected with in-line inspections. Additionally, Vramp testing confirmed the D_0 results; HF based pre-metal clean shows improved Vramp performance (Figure 4).

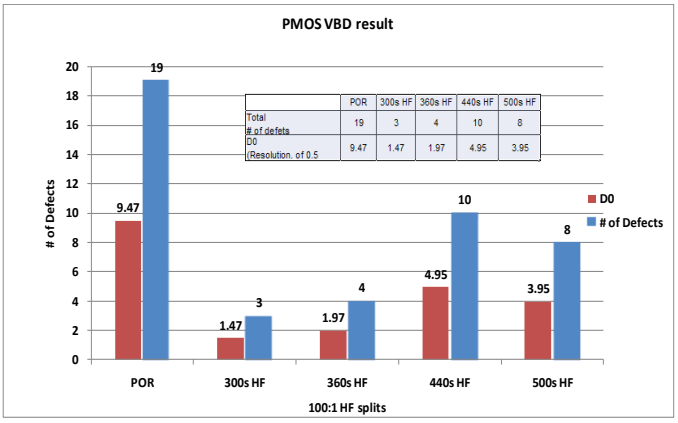

Figure4: VBD result on 100:1 HF

V. Conclusion

Reliability testing on a new process introduction identified a post-gate module defect issue impacting gate oxide integrity results. Stepwise product scan first identified the appearance of a polysilicon hole defects post the pre-metal clean. With the source identified as the pre-metal clean, short flow demonstrated that additional factors were necessary to the creation of these defects. These secondary factors include a boron doped polysilicon, and an oxide/nitride based silicide block module. It is theorized that aggregated boron in the polysilicon is etched in a BOE based solution; the final solution to the polysilicon hole defect was the replacement of a BOE clean with a HF based clean.

Acknowledgment

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