C3/D3

Process Technology

C3/D3: 0.35 μm Process Technology

ON Semiconductor®

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Overview

The C3/D3 process family from ON Semiconductor is an ideal 0.35 μm low cost solution to mixed−signal designs requiring a moderate amount of digital logic (up to 250 k gates). Optimized for 3.3 V operation with added devices for 5 V capability, high−performance, low−power, and mixed−signal digital libraries, and mixed−signal features such as poly−poly capacitors, Schottky diodes, and high resistivity poly. C3/D3 provides the flexibility to implement a variety of mixed−signal applications.

Features

- 3 to 5 Metal Layers
- Poly to Poly Capacitors
- Schottky Diodes
- High−resistance Poly
- Salicide Process with Optional Blocking
- 5 V Devices (Thick Gate Oxide)
- 5 V Tolerant I/O in Normal Process

PROCESS CHARACTERISTICS

Operating Voltage	3.3 V, 5 V
Substrate Material	P−Type, EPI
Drawn Transistor Length	0.35 μm
Gate Oxide Thickness	7.0 nm / 11.0 nm
Contact/Via Size	0.4 μm / 0.5 μm
Top Metal Thickness	675 nm
Contacted Metal Pitch	
Metal 1	1.1 μm
Metal 2−5	1.2 μm
Metal Composition	Al/TiN

SAMPLE PROCESS OPTIONS

	Mask Layers
1 Poly, 3 Metal	16
1 Poly, 5 Metal	20
2 Poly, 3 Metal. Hi−R Poly	20
2 Poly, 5 Metal. Hi−R Poly	24

DEVICE CHARACTERISTICS

All Values Typical at 25°C

TRANSISTORS

N−Channel	Typical Value	Units
V_t	0.5	V
I_{dsat}	510	μA/μm
P−Channel	**Typical Value**	**Units**
V_t	−0.554	V
I_{dsat}	−259	μA/μm

THICK GATE TRANSISTORS

N−Channel	Typical Value	Units
V_t	0.76	V
I_{dsat}	470	μA/μm
P−Channel	**Typical Value**	**Units**
V_t	−0.95	V
I_{dsat}	−240	μA/μm

RESISTORS

	Typical Value	Units
Poly	10	Ω/square
Hi−R Poly	1000	Ω/square
N−Diffusion	10	Ω/square
P−Diffusion	10	Ω/square
N−Well	1250	Ω/square

CAPACITORS

	Typical Value	Units
Poly−Poly	0.9	fF/μm^2

DIODES

Schottky Diode	Typical Value	Units
Area	5.1	μm^2
Id (Vf = 0.1 V)	0.05	μA
Id (Vf = 0.3 V)	2	μA
Id (Vf = 0.6 V)	175	μA

LIBRARIES

Standard Cell	
Ultra High Density Core Cell	pn sum: 2.0
	Area of 2−input nand (na21): 38.88 μm
	Gate density (na21 @ 100% utilization): 25.72 k gates/mm^2
	Scan Flop density (scan flops @ 100% utilization): 3.215 k ff/mm^2
	Average power (@ 3.3 V): 0.604852 μW/MHz/gate
Mixed−Signal Core Cell − Separate substrate for reduced noise	pn sum: 4.5
	Area of 2−input nand (na21): 74.88 μm
	Gate density (na21 @ 100% utilization): 13.35 k gates/mm^2
	Scan Flop density (scan flops @ 100% utilization): 1.842 k ff/mm^2
	Average power (@ 3.3 V): 0.6074 μW/MHz/gate
5 V Capable Core Cell − Thick gate logic design	pn sum: 5.0
	Area of 2−input nand (na21): 108 μm^2
	Gate density (na21 @ 100% utilization): 9.259 k gates/mm^2
	Scan Flop density (scan flops @ 100% utilization): 1.187 k ff/mm^2
	Average power (@ 5.0 V): 3.0553 μW/MHz/gate
Core Cell Level Shifters	Bidirectional: 2 cells, pad high to core low, or pad low to core high
	Unidirectional: 1 cell optimized for speed, pad high to core low
Standard I/O	
Fat Pad I/O Library (for core limited designs)	135 μm max in−line pad pitch
	459.15 μm pad height
Tall Pad I/O Library (for pad limited designs)	86 μm max in−line pad pitch
	730 μm pad height
5 V Capable I/O Library − Thick gate logic design	140.40 μm max in−line pad pitch
	274.05 μm pad height

MEMORY OPTIONS

RAM	
Asynchronous Single Port SRAM*	35 μm^2/bit (64 k bit memory)
Asynchronous Dual Port SRAM*	64 μm^2/bit (64 k bit memory)
ROM	
Asynchronous Diffusion ROM*	5.4 μm^2/bit (64 k bit memory)
Non−Volatile Memory	
EEPROM	Differential Bit Cell (Redundancy for High Reliability)
	2 ms Write
	Array: up to 1 k Bits (32x32), Vector: up to 32 bits (1x32)
	Internal Charge Pump provided

*Compiled

CAD TOOL COMPATIBILITY

Digital Design	Synopsys Design Compiler
	Cadence Verilog
Analog Design	Cadence DFII (4.4.6)
	Spectre
Place and Route	Synopsys Apollo, Astro
	Cadence Silicon Ensemble
Physical Verification	Mentor Calibre

PUBLICATION ORDERING INFORMATION

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