Development of a Trench isolated 50V technology on an SOI substrate

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High voltage BCD technologies developed at ON Semiconductor entail vertical DMOS requiring an n-buried layer (BLN) to collect the drain current and a highly doped n-path from the BLN to the top silicon, called n-sinker to bring back the current to the surface. The n-sinker is integrated to the Deep Trench Isolation module (DTI) required to isolate high voltage devices.

The DTI module has been the object of careful process optimization on bulk substrate to minimize leakage and reduce the amount of silicon defects [1, 2, and 3]. To further improve isolation and latch-up performances, the DTI module has been transferred to SOI (Fig. 1).

Feasibility of DTI without n-sinker on SOI has already been demonstrated with a filling made only of deposited oxide [4, 5] or of a bi-layer thermal oxide / polysilicon [6]. Adding an n-sinker to the sidewall of the DTI module is source of silicon defects, which can be reduced by filling the trench with a bi-layer deposited TEOS / polysilicon[7]. We demonstrated that defect free processing of DTI with n-sinker on SOI was possible using a bi-layer of thermal oxide and polysilicon or a tri-layer of thermal oxide, TEOS and polysilicon as filling.

For the purpose of the experiment a test vehicle has been processed on SOI and its quality was assessed by electrical measurements and physical characterization. On SOI, since the isolation is being ensured by the Buried Oxide (BOX) and not by a diode, the DTI processing can be limited to its upper part above the BLN. The etching down to the substrate is therefore avoided, as well as the hard mask it requires. Although processing is simpler and electrical performances are better, the module is very sensitive to liner oxide and sinker doping processing conditions with respect to defect generation.

First of this critical processing steps, the N-sinker, is formed by liquid source diffusion using $POCl_3$ as the Phosphorous source. The doping sequence starts with the conformal deposition of a phosphorus doped oxide, followed by a diffusion step where the phosphorous penetrates into the silicon. As seen in Fig. 2, long phosphorous deposition steps result in higher silicon defect. Next to destructive selective wet etching, drain quiescent current frames (IDDQ) can also be used to quantify accurately silicon defects. Fig 4 shows the response leakage of the IDDQ array for various $POCl_3$ splits. No sinker or lowly doped sinker yields no leakage while highly doped sinker results in high IDDQ leakage level, which is in line with the defect signature revealed by selective wet etching.

As depicted in Fig. 3, a thick liner oxide guarantees a high breakdown voltage of the DTI. For too thin liner oxide, the breakdown voltage decreases drastically due to oxide thinning at trench bottom (Fig.5). Unfortunately, increasing liner oxide thickness yields too many silicon defects if oxide is grown at reference temperature (Fig. 6). A way to overcome the appearance of silicon defects is to grow the liner oxide at higher temperature. Fig. 7 and 8 shows that defects can be avoided even for a 3 kÅ liner oxide when grown at higher temperature. This beneficial effect of high temperature can be attributed to the oxide viscosity and generated stress which decreases with increasing temperature [8, 9]. However, a trade-off has to be found between increased thermal budget necessary to avoid silicon defects and excessive sinker diffusion induced by this thermal budget. Indeed, as seen in Fig. 9, if sinker diffuses too much towards the active area, the breakdown voltage of VDMOS drops due to interaction with the lateral termination of the device. A way to overcome the too high thermal budget while enhancing the breakdown voltage of the DTI module and avoiding generation of silicon defects is to deposit a TEOS layer on a thin liner oxide grown at reference temperature. As seen in Fig. 10, the deposited TEOS is very conformal and compensate the liner oxide thinning at trench bottom.

We demonstrated so far that fabrication of defect free DTI trenches with high breakdown voltage was possible. Final paper will present an optimized DTI module, combining high DTI isolation capability, low diffusion of sinker and defects free silicon. Two processing options are being investigated; reducing the initial sinker doping to keep sinker diffusion under control despite a high thermal budget required to grow a thick liner oxide at high temperature or combining a thin thermal oxide grown at low temperature with a TEOS deposition to enhance dielectric thickness.

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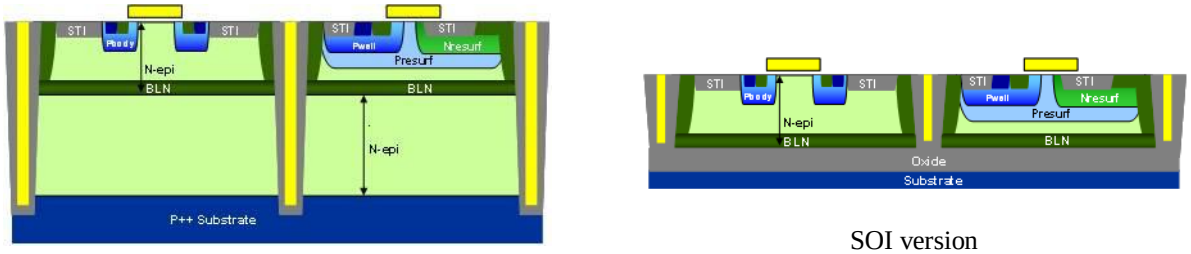
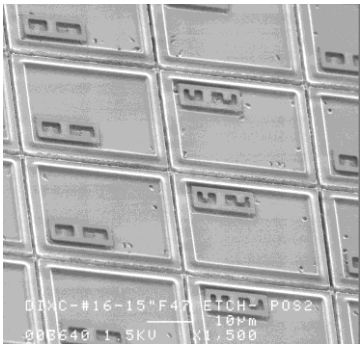


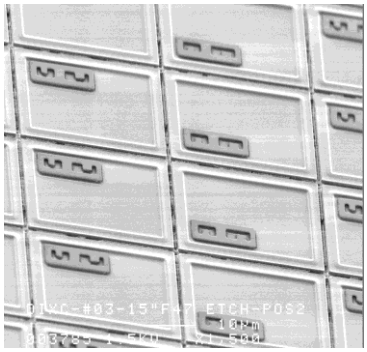
Bulk version

SOI version

Figure 1: Schematic of the high voltage technology on bukl and SOI substrates



(a) Long $POCl_3$ deposition step + standard diffusion



(b) Reduced $POCl_3$ deposition step + standard diffusion

Figure 2: Silicon defect generation in function of $POCl_3$ processing. Long deposition step (a) yields silicon defects while reduced deposition step (b) avoid defect formation

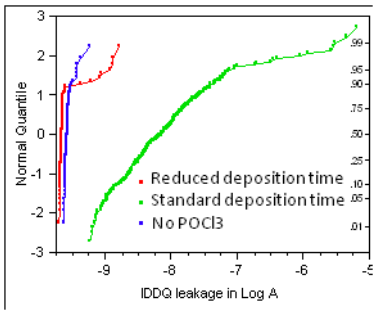


Figure 3: Leakage of IDDQ frame in function of $POCl_3$ deposition time

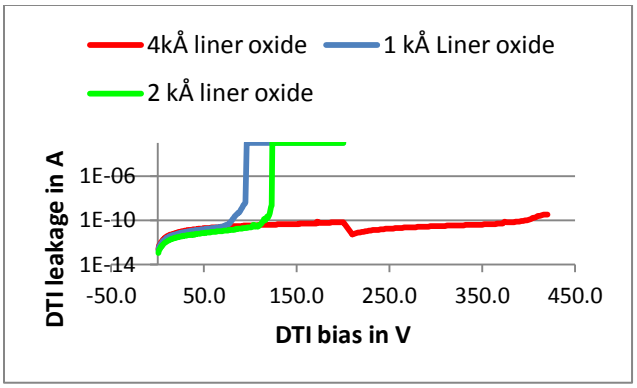


Figure 4: DTI breakdown voltage in function of liner oxide thickness

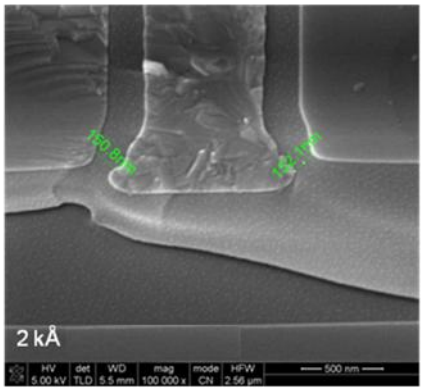


Figure 5: Oxide thinning at trench bottom

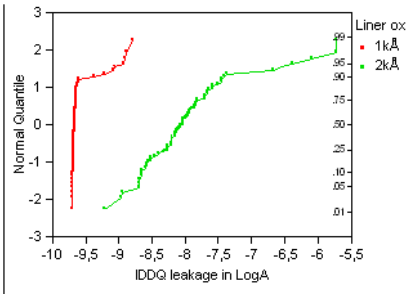


Figure 6: IDDQ leakage in function of liner oxide thickness (reference temperature)

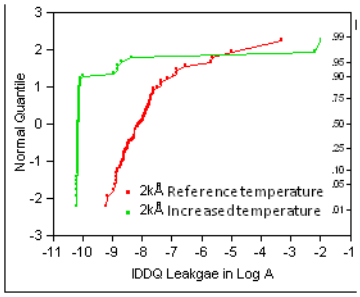
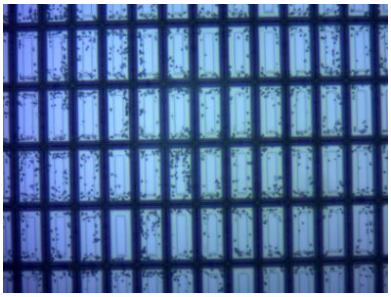
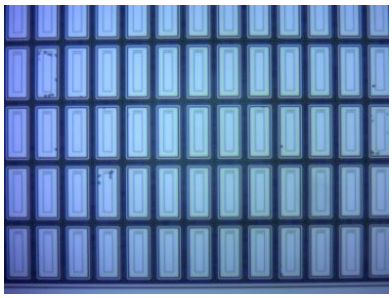


Figure 7 : IDDQ Leakage in function of liner oxide temperature



3 kÅ liner oxide at reference temperature



3 kÅ liner oxide at higher temperature

Figure 8: Defect generation in function of liner oxide temperature growth. Low oxidation temperature (a) yields silicon defects, while high oxidation temperature (b) results in defects free structures

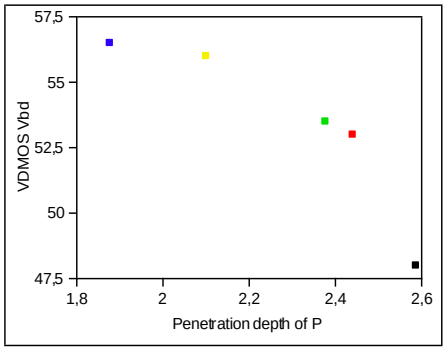


Figure 9: N-sinker diffusion depth versus VDMOS breakdown voltage

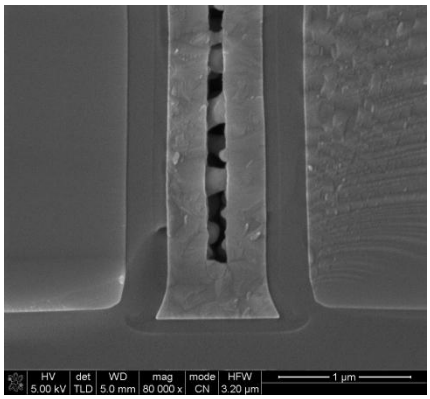


Figure 10: Reduction of dielectric thinning by depostion of a TEOS layer