New VDMOS Structure with Discontinuous Thick Inter-Body Oxide to Reduce Gate-to-Drain Charge

J. Roig, S. Mouhoubi, P. Gassot, R. Charavel, A. Suvkhanov*, P. Moens, F. Bauwens, M. Tack
Power Technology Centre - Corporate R&D, ON Semiconductor, Oudenaarde (Belgium)
*Process Development & Integration - Corporate R&D, ON Semiconductor. Gresham (USA)
jaume_roigguitart@onsemi.com

***Abstract*— A new vertical power MOSFET (VDMOS) structure with a Discontinuous Thick Inter-Body Oxide (DTIBO) is presented and experimentally analyzed in this paper. The new structure substantially reduces the Qgd*sRon figure-of-merit without excessive BVds penalization with respect to the conventional VDMOS. Moreover, the undesired hot-carried injection (HCI) effects are also assessed.**

I. INTRODUCTION

High-frequency systems including power switches require low transient losses to increase their efficiency. Among other power switches, the planar vertical power MOSFET (VDMOS) is still a feasible option due to its robustness and fabrication simplicity. Consequently, many efforts have been made during the last years to minimize Qgd, which is crucial to alleviate the transient losses in these devices. In the conventional VDMOS structure, the shrinkage of the inter-body region is a common solution to diminish Qgd. However, this solution increases sRon even when considerable improvement is achieved by shallow p-body implants [1]. Aside from the conventional structure, two main variants are reported to optimize Qgd in planar vertical power MOSFETS: the Split-Gate [2-7] and the Continuous Thick Inter-Body Oxide (CTIBO) structures [8-10]. On top of the increment of the process complexity and cost, these structures sometimes degrade sRon or/and BVds. In this work a new VDMOS device with low Qgd is created by means of a Discontinuous Thick Inter-Body Oxide (DTIBO). The electrical performance and Hot Carrier Injection (HCI) degradation of the DTIBO is critically evaluated and compared to VDMOS and CTIBO. Even though the DTIBO structure is experimentally proved for a 100V power switch, the extension of DTIBO for a 30V range is eventually demonstrated by three-dimensional TCAD simulation.

II. DEVICE STRUCTURE AND TECHNOLOGY

A comparison between the conventional n-channel VDMOS, CTIBO and DTIBO structures is displayed in Fig. 1. In order to integrate the DTIBO device, a new Shallow Trench Isolation (STI) pattern has been defined for an existent 100V-rated VDMOS. The later is integrated in a 0.18µm Smart Power technology resembling the quasi-vertical n-channel VDMOS in our former technologies [11]. The critical parameters defined in the new STI pattern are: the polygate edge to STI distance (Lb), the STI width (Wsti) and the STI spacing (Wfin). Moreover, the p-body implant is aligned to the poly-gate thus giving for a constant channel length (Lch) and junction depth (Xj). Note that Xj is similar than the STI depth (Tsti), being both of them in the submicron range.

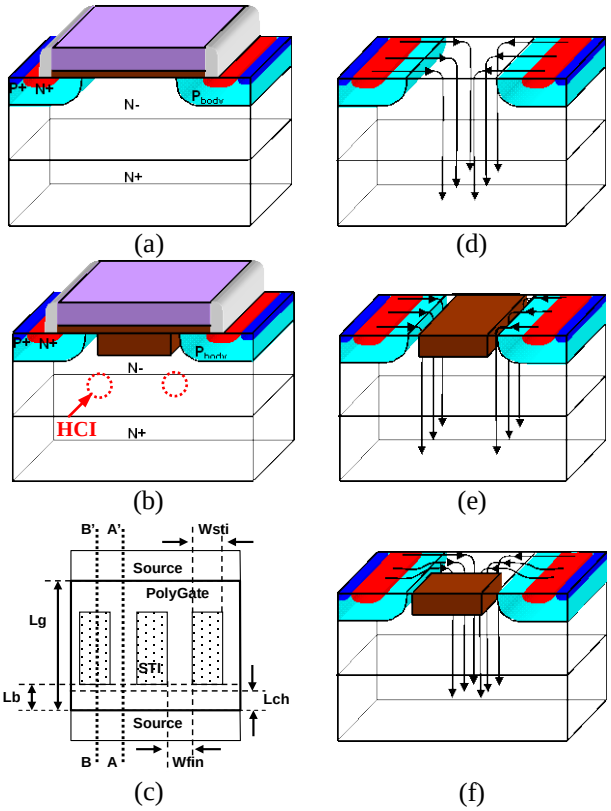

Figure 1. Schematic 3D structure of (a) VDMOS and (b) DTIBO/CTIBO. The main geometrical parameters for DTIBO (Lb, Wsti, Wfin) are indicated in (c).Current flowlines in on-state for (d) VDMOS, (e) CTIBO and (f) DTIBO. In the fabricated devices Tox=7nm, Tsti~Xj<1µm and Lg is fixed to the VDMOS optimum value.

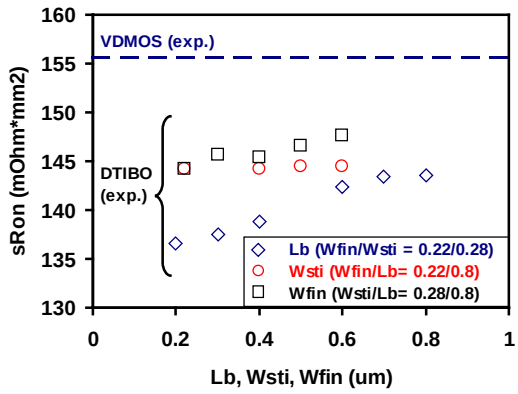

Figure 2. sRon (Vgs=3.3V, Vds=0.1V) vs. Lb, Wsti and Wfin for DTIBO (exp.). The sRon for conv. VDMOS (exp.) is indicated.

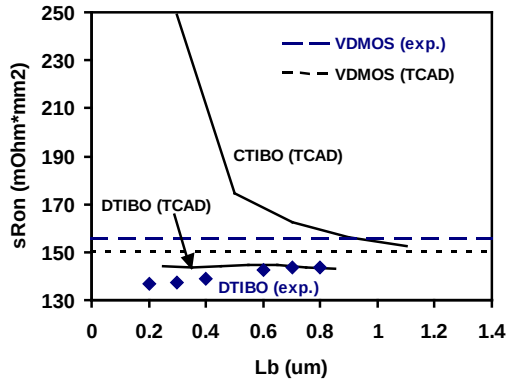

Figure 3. sRon (Vgs=3.3V, Vds=0.1V) vs. Lb for DTIBO (exp./TCAD) and CTIBO (TCAD). Wfin/Wsti=0.22/0.28 in DTIBO.

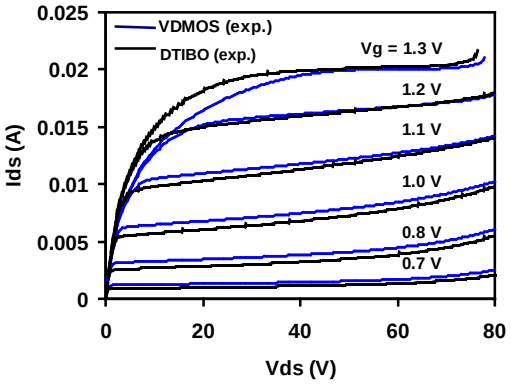

Figure 4. Comparison between output characteristics for DTIBO (Wfin/Wsti=0.22/0.28, Lb=0.4μm) and conventional VDMOS.

The process to create the STI islands in DTIBO corresponds to the standard 0.18μm CMOS process to create STI isolation regions. As a consequence, the DTIBO devices do not require additional mask/process. Despite that the real structure of the VDMOS is quasi-vertical, the additional parasitic elements corresponding to the N^+ buried layer and N^+ sinker wells are negligible. In accordance to all this, the beneficial effects of the DTIBO structure on the Qgd*sRon trade-off are established by the combined action of device areas with AA' and BB' cross sections:

(i) The areas with BB' cross section, defined by Wsti, reduce Qgd by partially replacing thin gate oxide by thick STI oxide in between two consecutive p-body regions (Tsti>>Tox). The STI region should not penetrate into the p-body (Lb>Lch) in order to avoid pile-up of dopants close to the STI (causing a double Vth) and a possible channel resistance degradation. In the CTIBO approach the BB' cross section is everywhere.

(ii) The areas with AA' cross section, defined by Wfin, enable low sRon by enlarging the conduction area at the accumulation region (see current flowlines in Fig. 1). It can be noticed that the AA' cross section is identical to the conventional VDMOS one. Hence, Lg is optimized in the same way as than in VDMOS by searching the best compromise between the area and the parasitic JFET resistance.

III. Electrical Characteristics

A. *Specific On-State Resistance*

The measured sRon in VDMOS and DTIBO are compared in Fig. 2, including variations on Lb, Wsti and Wfin. While Wsti and Wfin do not have a relevant effect on sRon, influence of Lb is interestingly important. For short Lb, the BB' regions are expected to show a highly resistive path for the current due to the current crowding between STI and p-body/n-drift junction. This effect is clear in CTIBO from the TCAD results in Fig. 3. Contrarily, sRon in DTIBO and VDMOS are similar thanks to the existence of AA' regions. The slight sRon decrement with Lb in DTIBO, as well as the low sRon values (below the 156mOhm.mm^2 measured in VDMOS), can be explained by the existence of an accumulation region in the lateral STI walls. A prove of this is that DTIBO shows larger Id than VDMOS at high Vg but not at low Vg as observed from the Ids-Vds curves of Fig. 4. Other important parameters such as Vth remain nearly unchanged in all cases (Vth~0.6V).

B. *Reverse Breakdown Voltage*

A comparison between measured BVds in VDMOS and DTIBO is shown in Fig. 5 for different Lb, Wsti and Wfin. In VDMOS, a short enough Lg provides the known shield effect between two adjacent p-body wells. Subsequently, the BVds is close to the parallel plane p-body/n-drift junction one (with BVds=115.5V). Differently, BVds is reduced in DTIBO, being lower at short Lb (STI region approaches the p-body). The BVds decay with Lb is even more pronounced in CTIBO as it is observed from the TCAD results in Fig. 6. This means that the STI next to the cylindrical p-body/n-drift junction certainly have an influence on the BVds. Indeed, the presence of STI enhances the electric field and the impact ionization in the corner of the p-body as it can be inferred from TCAD results in Fig. 7. The increment of Lb as well as the DTIBO structure relaxes such effect. It can be noticed from Fig. 5 that a DTIBO with larger Wsti or shorter Wfin is approaching the

CTIBO and, consequently, a lower BVds appears. The leakage current before BVds is always low (Ileak~1x10^{-11}A/µm).

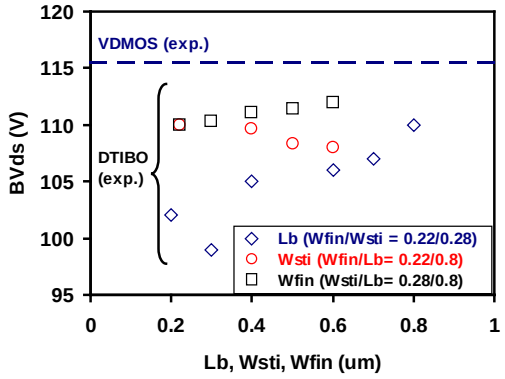

Figure 5. BVds vs. Lb, Wsti and Wfin for DTIBO (exp.). The BVds for conventional VDMOS (exp.) is indicated.

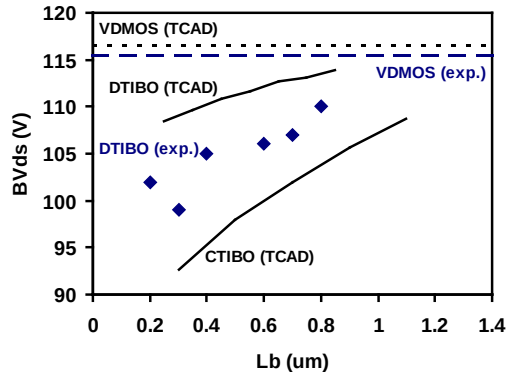

Figure 6. BVds vs. Lb for DTIBO (exp./TCAD) and CTIBO (TCAD). Wfin/Wsti=0.22/0.28 in DTIBO.

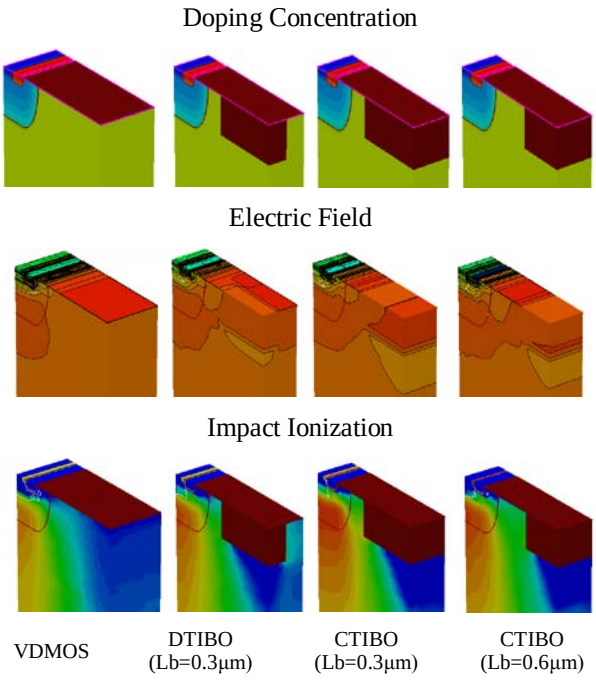

Figure 7. TCAD results for electric field and impact ionization isolines in VDMOS, CTIBO (Lb=0.3µm) and DTIBO (Lb=0.3 and 0.6µm) when the drain is biased to BVds and the gate/source are grounded .

C. Gate-to-Drain Charge

In order to obtain a low Qgd, two main parameters are minimized in the DTIBO layout: Lb and Wfin/Wsti. The Qgd per unit of area (Qgd/A) is linearly reduced with Lb in CTIBO and DTIBO as it is demonstrated by TCAD simulations in Fig. 8. The Qgd values in the TCAD simulations are directly extracted from the plateau region in the typical Vg-Qg curve. As it is understood, the Qgd/A reduction in CTIBO is more important than in DTIBO. In fact, Qgd/A is proportional to the accumulation area without STI. In spite of the fast Qgd/A drop, the CTIBO with short Lb suffers from a critical sRon increment (see TCAD data in Fig. 3) which becomes predominant in Qgd*sRon. As a consequence, DTIBO shows the best Qgd*sRon. Nevertheless, the excessive shrinkage of Lb is a possible inconvenience in DTIBO. In addition to the observed diminishment of the BVds (Fig. 5), the HCI is a limiting factor as it will be elucidated in the following section.

An alternative way to reduce Qgd/A is the Wfin/Wsti minimization. Such a minimization has some limits. For instance, the smaller Wfin distance is fixed by the technology rules and the largest Wsti should not imply a degradation of the channel resistance when Wsti>>Lch. In our fabricated devices Wfin cannot be further reduced. However, Wsti can be enlarged until 0.6µm (with Lb fixed to 0.8µm) without suffering drastic changes in sRon and BVds as it is noticed from Figs. 2 and 5.

Once the optimum geometrical parameters for a 100V DTIBO are defined as Lb=0.6-0.8µm and Wsti=0.6µm, the combination of simulated Qgd and measured sRon concludes an important Qgd*sRon improvement with respect to VDMOS and CTIBO. A summary of the main electrical characteristics for DTIBO, CTIBO and VDMOS is found in Table 1. For a 100V-rated power switch, Qgd*sRon is reduced by a 50% and 20% compared to VDMOS and CTIBO, respectively. A complete TCAD study of Qgd*sRon is also performed in 30V-rated power switch. In this case the drift region thickness and doping concentration have been re-optimized, as well as Lg and Lb values. It is inferred from Table 1 a 40% and 10% Qgd*sRon reduction when comparing to VDMOS and CTIBO, respectively.

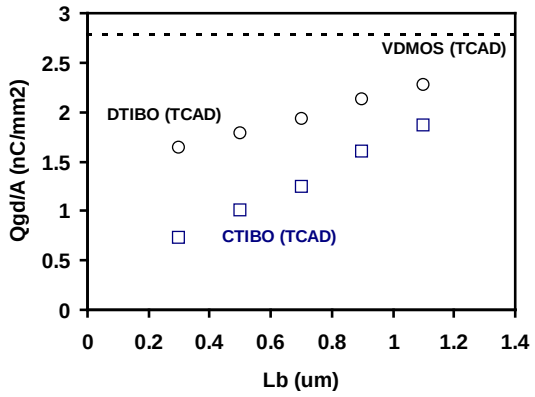

Figure 8. Qgd/A (Vds=10V) vs. Lb for DTIBO (TCAD), CTIBO (TCAD) and conventional VDMOS (TCAD). Wfin/Wsti=0.22/0.28 in DTIBO.

TABLE I. ELECTRICAL CHRARACTERISTICS FOR 30 AND 100V VDMOS, CTIBO AND DTIBO

100V	**VDMOS**	**CTIBO Lb=1um**	**DTIBO**	
			Lb=0.8µm Wsti=0.6µm Wfin=0.22µm	**Lb=0.6µm Wsti=0.6µm Wfin=0.22µm**
BVds (V)	**115.5**	108.0	**108.0**	**107.5**
sRon (mOhm*mm2) Vds,Vgs=0.1V, 3.3V	**155.5**	155.0	**143.5**	**146.6**
Qgd/A (nC/mm2) (Vds=10V)	2.8	1.8	1.7	1.5
Ron*Qgd (mOhm*nC)	435	279	244	213

30V	**VDMOS**	**CTIBO Lb=0.7um**	**DTIBO**	
			Lb=0.5µm Wsti=0.6µm Wfin=0.22µm	**Lb=0.5µm Wsti=0.6µm Wfin=0.22µm**
BVds (V)	34.8	34.4	34.5	34.5
sRon (mOhm*mm2) Vds,Vgs=0.1V, 3.3V	14.6	20.5	17.5	17.5
Qgd/A (nC/mm2) (Vds=10V)	2.0	0.9	1.0	1.0
Ron*Qgd (mOhm*nC)	29.3	18.8	17.5	17.5

a. Experimental (bold) and TCAD (normal) are combined to extract Ron*Qgd.

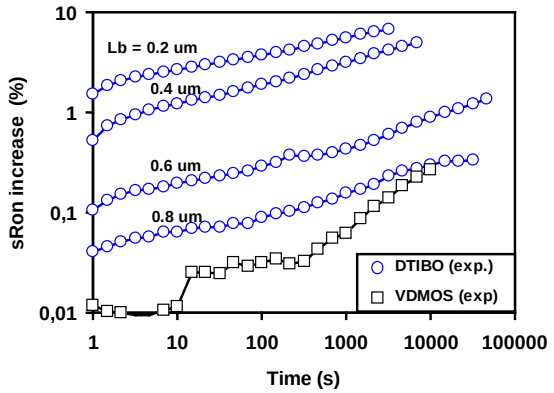

Figure 9. Measured sRon degradation vs. time for conventional VDMOS and DTIBO (Wfin/Wsti=0.22/0.28, Lb=0.2, 0.4, 0.6 and 0.8µm). Vds=80V and Vgs=1V.

IV. HOT CARRIER INJECTION DEGRADATION

It is noticed from Fig. 8 that the DTIBO devices with Lb<0.6µm can further ameliorate Qgd*sRon. However, these devices have been disregarded in Table 1 due to the experimented severe HCI degradation. As it is observed from Fig. 9, the initial sRon degradation (for less than 1s) rises when reducing Lb, thus being high above 0.1% for Lb<0.6µm. In a comparable way to lateral power MOSFETs with STI [12], the initial degradation is probably due to the injection of holes in the deep STI corner next to the p-body (dotted line circles in Fig. 1b). In this region, the current density is larger for shorter Lb thus producing more prominent impact ionization. After the initial degradation the parameter n, corresponding to a t^n degradation model, is similar for all Lb (n~0.2). Another remarkable observation is that n~0.3 in VDMOS but the initial degradation is very small.

V. CONCLUSION

A new DTIBO power switch is presented, analyzed and experimentally proved in this paper. The DTIBO significantly improves Qgd*sRon with respect to the conventional VDMOS and CTIBO for applications ranging from 30 to 100V. This advantage does not imply a relevant penalization of BVds or a more severe HCI degradation. Moreover, the integration of DTIBO in our 0.18µm Smart Power technology does not require additional cost.

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