

# Shielded from the blight

Switched-Mode Power Supplies (SMPS) are increasingly popular in automotive electronic systems but can present EMC problems. Frequency modulation could provide the answer. By Kieran McDonald

As energy efficiency becomes a key concern throughout vehicle infrastructure, Switched-Mode Power Supplies (SMPSs) are becoming the preferred solution thanks to their high efficiency compared to linear regulators. But switched-mode converters generate electromagnetic interference (EMI) that may call for expensive countermeasures such as shielding and could demand extra engineering time to pass vehicle Electromagnetic Compatibility (EMC) tests.

Among various power-supply design techniques used to minimise EMI, spread-spectrum techniques that automatically vary the switching frequency are effective in reducing the noise energy at any given frequency. Complex spread-spectrum techniques such as pseudo-random modulation can yield the greatest improvements.

While some SMPS controllers have an integrated spread-spectrum function, many do not. In such cases, an alternative means of achieving spread-spectrum behaviour can help improve the vehicle's EMC performance: knowing that other in-vehicle electronics often contain an FPGA to provide basic

functions it is feasible to use some of the FPGA circuitry to implement a pseudo-random modulator. Only a small amount of FPGA circuitry and a single I/O pin, and an SMPS IC with a synchronisation (SYNC) pin, are needed.

## Spread-spectrum modulation

Typically, the SMPS output is regulated by switching the main power MOSFET at a fixed frequency, using a voltage signal fed back from the output to modulate the pulse width and so regulate the output voltage. When using SMPS ICs such as the NCV8851-1 or NCV890231, the switching frequency is determined by connecting a resistor between the internal oscillator and ground via the IC's  $R_{OSC}$  pin, as the simplified SMPS block diagram of Figure 1 shows. Alternatively the device can be synchronised to an external clock by connecting a frequency source of higher frequency than the integrated oscillator to the IC's SYNC pin, also shown in Figure 1.

When analysed in the frequency domain, the switching pulses can be seen to comprise a fundamental sinusoidal component at a frequency related to the pulse period and a theoretically infinite number of harmonics at higher frequencies. Lower-order harmonics contain the highest proportion of the total signal energy, reducing in higher-order harmonics towards a practically negligible level.

The energy contained in the fundamental and harmonics is responsible for EMI emitted by the power supply, and must be attenuated. In general-purpose applications, best design practice applied to aspects such as

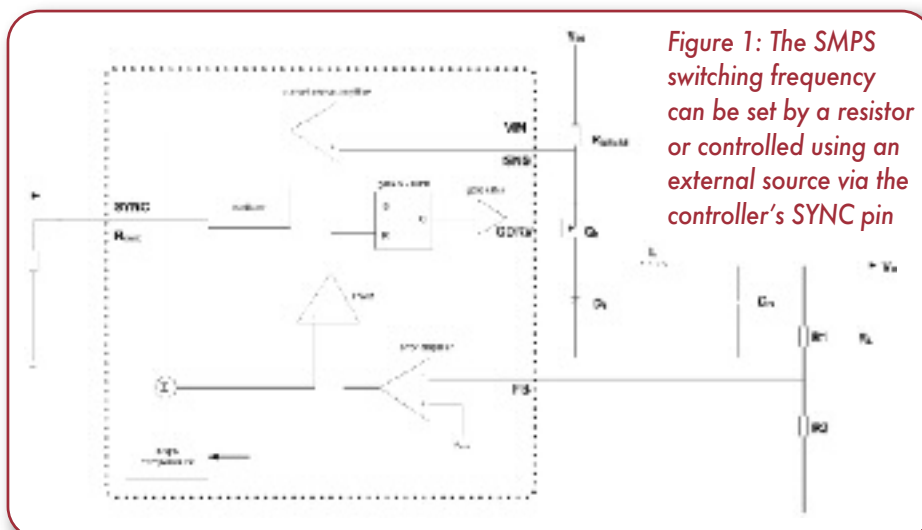


Figure 1: The SMPS switching frequency can be set by a resistor or controlled using an external source via the controller's SYNC pin

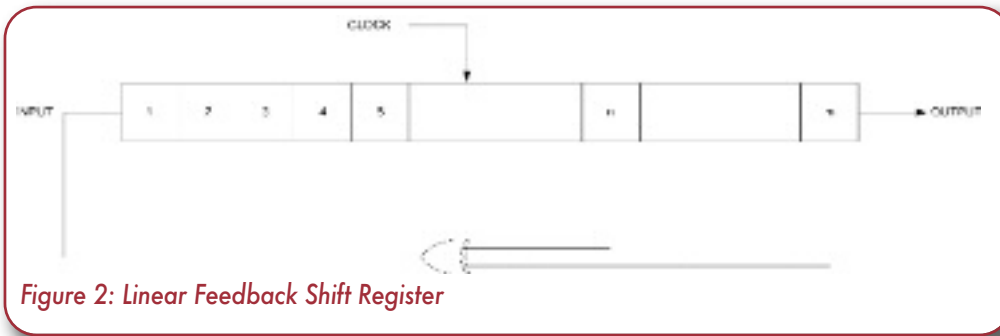


Figure 2: Linear Feedback Shift Register

Various randomisation schemes could be considered; a Linear Feedback Shift Register (LFSR), shown in Figure 2, is considered the most appropriate for digital implementation.

The LFSR is a synchronous circuit making use of D-type

Flip-Flops, connected in series, as a shift register. The shift register is of 'm' bits in length, clocked by a periodic clock which will produce a pseudo-random bit sequence. Feedback is provided by XORing the output at one or more 'tap' points, the mth and nth bits respectively, to the input of the register. The register will cycle through a set of deterministic states, repeating the sequence every 'K' cycles. The maximum number of cycles is termed maximal-length:

$$K = 2^m - 1$$

The "-1" term is introduced as an all zero register state would result in a zero being fed back to the input, which ultimately results in register lock-up by allowing a perpetual all-zero state. The aim then is to determine, for a register of a given length, the maximal state; that is the tap point for the XOR feedback that ensures the all zero state will not occur. The tap sequence to achieve maximal length is a polynomial mod2:

$$1 + X^n + X^m$$

The LFSR therefore does not produce a random

sequence but a pseudo-random sequence, as it is a sequence that will repeat itself at the end of the cycle. However, the sequence length can be made to be such a length that its repeat rate or frequency is low and can therefore, for

component selection, PCB layout, shielding and filtering may be adequate. When very low emitted noise is required, such as in an automotive SMPS, spread-spectrum techniques can achieve further noise attenuation by modulating the frequency of the switching pulses to spread the energy contained over a broader frequency range. Although spread-spectrum does not reduce the total noise energy in the switching waveform, the peak energy at any given frequency is reduced.

Pseudo-Random Frequency Modulation with Fixed Duty cycle (PRFMFD) has been found to yield optimal results, by not only distributing the noise power over a continuous spectrum but also minimising output-voltage ripple by virtue of the fixed duty cycle. This results in superior output regulation and reduced low-frequency noise, and also helps to simplify design of the feedback circuit while ensuring loop stability.

### Circuit implementation

Implementation of a PRFMFD function in an FPGA requires two key design blocks: a randomisation block and a modulation block. A decoder is required to interface the two.

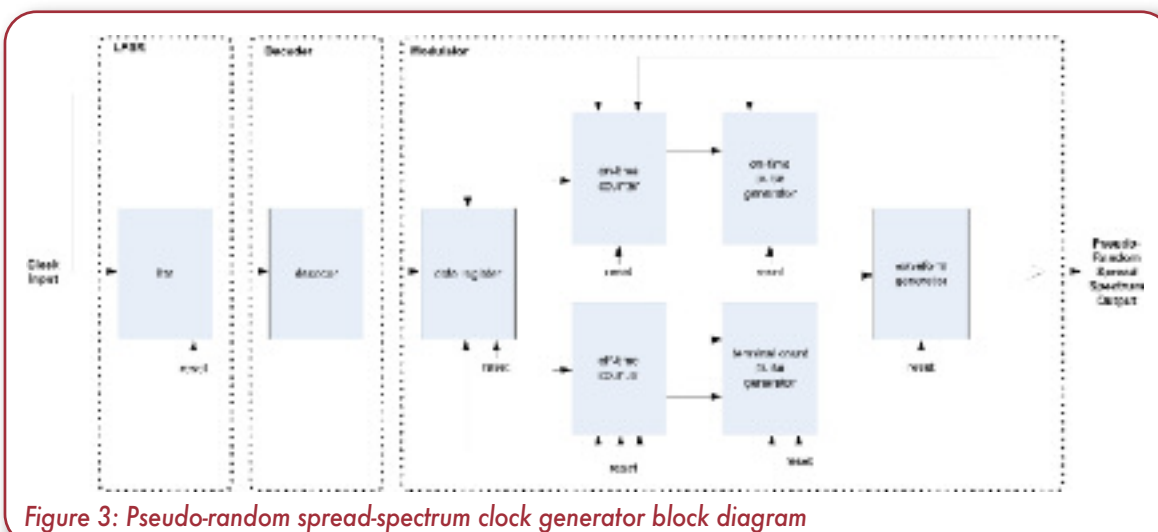
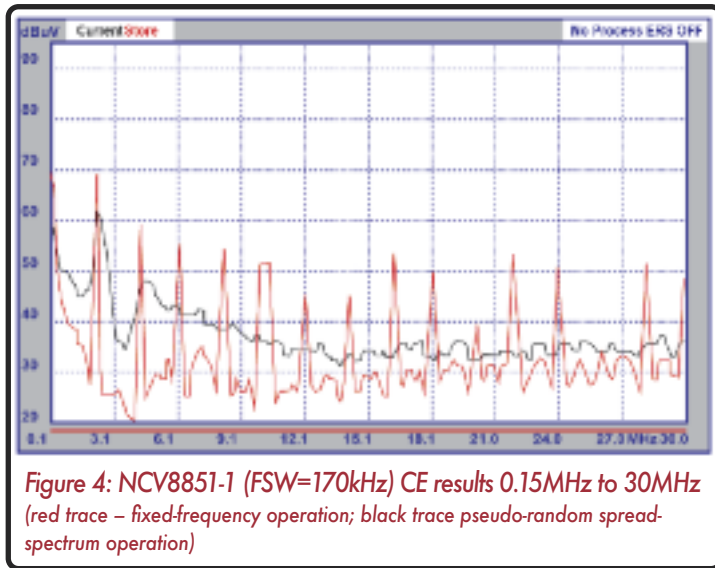


Figure 3: Pseudo-random spread-spectrum clock generator block diagram



most practical purposes, be considered statistically random.

The length of the LFSR,  $m$ , is a key parameter enabling control of the modulating frequency and other key control parameters. The modulating frequency, or the register frequency, has to be set so as to avoid audible frequencies. The human audible range is between approximately 20Hz and 20kHz.

Different register lengths require different tap points; the  $m$ th and the  $n$ th terms XORd together. For most values of 'm' a single tap point, 'n', is required, however for some values of 'm' multiple tap points are required. While additional XOR operators can be included in the design, the circuit can be simplified somewhat by avoiding values of 'm' that require more than a single tap point.

The LFSR cycle sequence is deterministic. The registers as a result should be started in a known state for validation of correct operation. For this

reason a reset is used so that the registers are 'seeded' at reset both to ensure a known state is initialised and to ensure that register lock-up does not occur.

The decoder interfaces the LFSR word to the modulator word, interpreting the LFSR outcome to a specific period. It can be designed as an asynchronous block, with the intent that the decoding process should occur in a time period of less than the LFSR clock period, so as not to compromise statistical randomness.

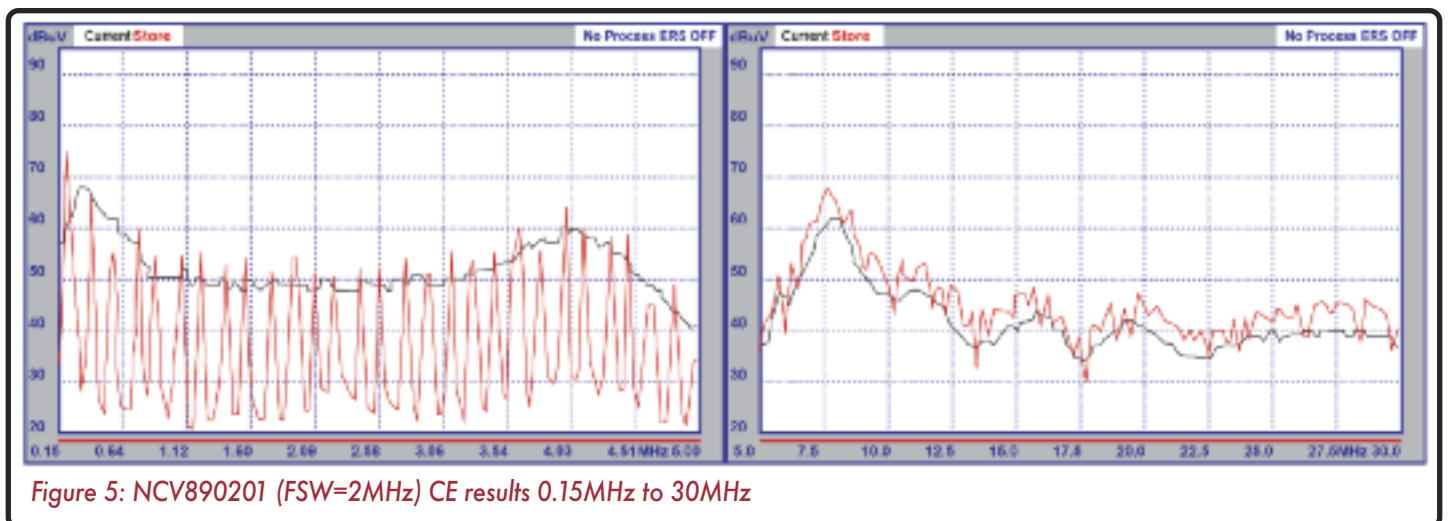
The implemented design samples the first four bits of the LFSR. These are then decoded to a maximum of 16 possible frequency outcomes.

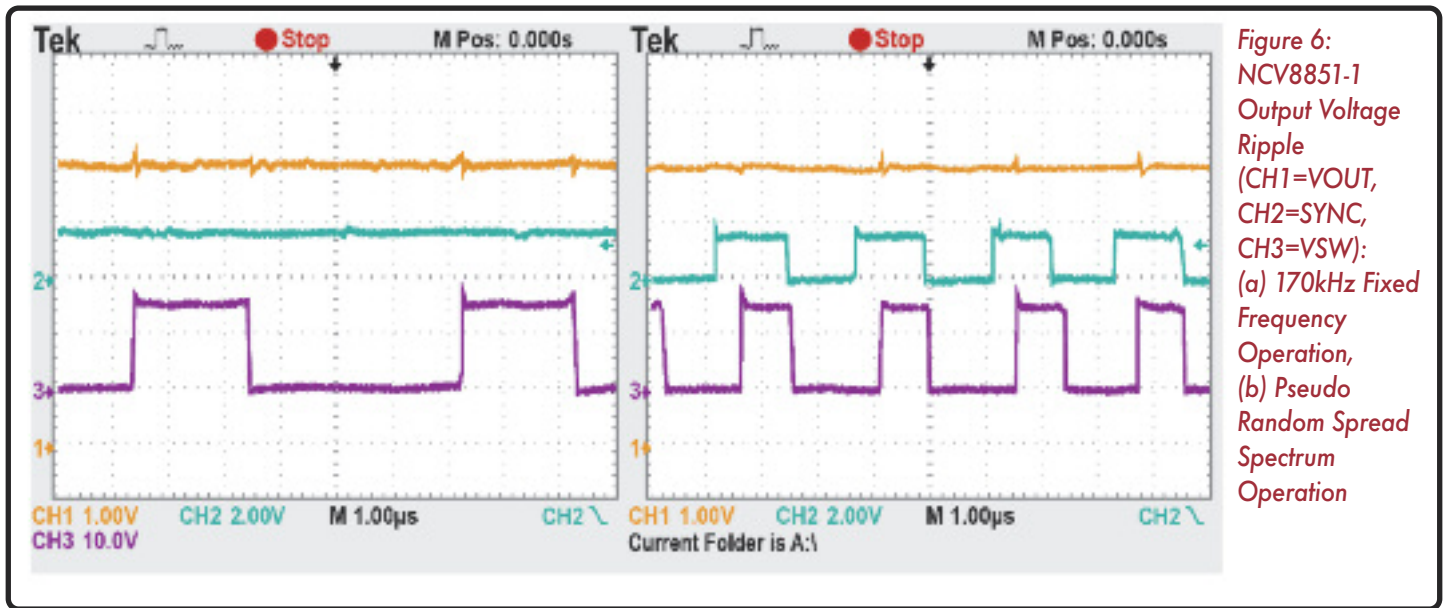
The FPGA is able to implement an entirely digital interface capable of producing a rectangular waveform. In practice this limits the interface to driving the SMPS SYNC pin only.

The LFSR provides a parallel output signal to the decoder which decodes the LFSR number to a number that corresponds to a period that the modulator can interpret and reproduce at the output.

The modulator is a synchronous circuit receiving data from the decoder and interpreting this as a fixed period, driving its output signal appropriately. The output transmits a rectangular wave with a fixed 50% duty.

A key consideration is to create a design that controls an SMPS IC suitable for automotive cockpit applications. However, implicit within this is the need to minimise any EMC impact that the design may have on other nearby systems and specifically with the highly susceptible radio receiver. As a result the frequency of operation of the design, and consequently the switching





frequency of the SMPS IC it is controlling, is an important consideration.

While most consumer listening of analogue audio frequencies is of stations broadcasting in the FM band, FM's higher signal-to-noise ratio means that FM interference is less problematic than AM interference. Hence avoiding a fundamental frequency, or one of its harmonics, that conflicts with a tuned radio band is important if the design is to minimise interference with the radio receiver. While it is difficult to avoid harmonics in the broadcast bands a nominal frequency can be selected that minimises conflicts. A higher switching frequency has a lower probability of harmonic conflict within a broadcast band.

### Evaluating performance

The PRFMFD circuit was implemented using 63 logic elements of an Altera Cyclone 2 2C20 FPGA, representing just 0.3% of available resources. A single pin provides the spread-spectrum output. For test purposes a hard-wired toggle switch is used to enable/disable the output.

The spread-spectrum output of the FPGA was applied to two different ON Semiconductor automotive 'buck' SMPS ICs: NCV8851-1, a 0.5MHz NMOS synchronous controller and NCV890201, a 2MHz NMOS non-synchronous converter. Two different nominal frequency settings and bandwidths were used, depending upon the

SYNC frequency range of the SMPS IC: 32 frequencies between 219kHz to 481kHz, or four different frequencies between 1.92MHz to 2.5MHz.

As Figures 4 and 5 show, performance varies across the spectrum. However, the results can be summarised. Pseudo-random modulation of the NCV8851-1 yielded a 10dB/µV improvement of the 170kHz fundamental and approximately 5dB/µV across the spectrum. Pseudo random modulation of the NCV890201 yielded an 8dB/µV improvement of the 2MHz fundamental and approximately 10dB/µV to 18dB/µV across the spectrum.

The difference between the lower and upper limits of peak-to-peak output voltage measured in different experiments was only 240mV. The worst case ripple was 800mV. This compared to a worst case peak-to-peak output voltage for fixed-frequency operation of 720mV, as shown in Figure 6. This indicates there is no significant increase in ripple due to pseudo-random spread-spectrum operation.

Pseudo-random spread-spectrum modulation, in automotive cockpit applications, can be implemented with spare FPGA system resource and SMPS ICs such as the ON Semiconductor NCV8851-1 and NCV890201. The solution utilises minimal FPGA system resources and I/O, and can substantially reduce spectral emissions, without sacrificing output voltage ripple.

Author profile: Kieran McDonald is a Field Applications Systems Engineer for ON Semiconductor

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