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A LOW SERIES RESISTANCE, HIGH DENSITY, TRENCH CAPACITOR FOR HIGH-FREQUENCY APPLICATIONS

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Presentation Outline

- **1. Introduction / purpose**
- **2. High frequency trench capacitors**
  - **a) MIS trench capacitors**
  - **b) High frequency “wrap-around” PIP cap.**
- **3. High frequency PIP capacitor characterization**
  - **a) Electrical characterization and modeling**
  - **b) Reliability evaluation**
- **4. Potential enhancements / applications**
- **5. Summary**
- **6. Acknowledgments**

1. Introduction/Purpose

- A novel, modular, high speed, VLSI MOS-compatible decoupling trench capacitor with tunable frequency response has been modeled and electrically characterized.

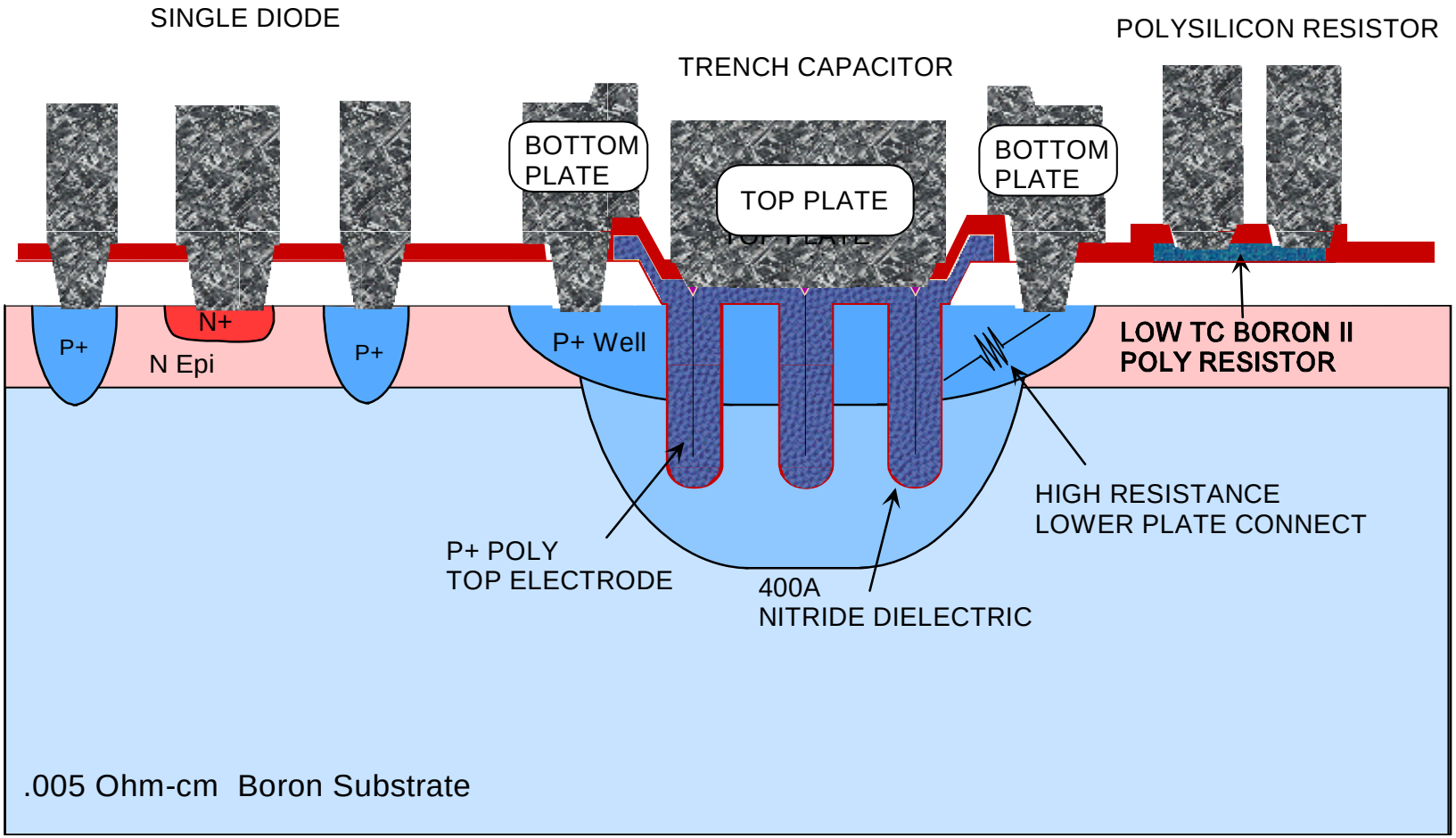
- The flexible capacitor design enables low Dt, drop-in capability across a number of technologies and has been qualified for both CMOS and BiCMOS applications.

➢ 2. High frequency trench capacitors

a) MIS trench capacitors

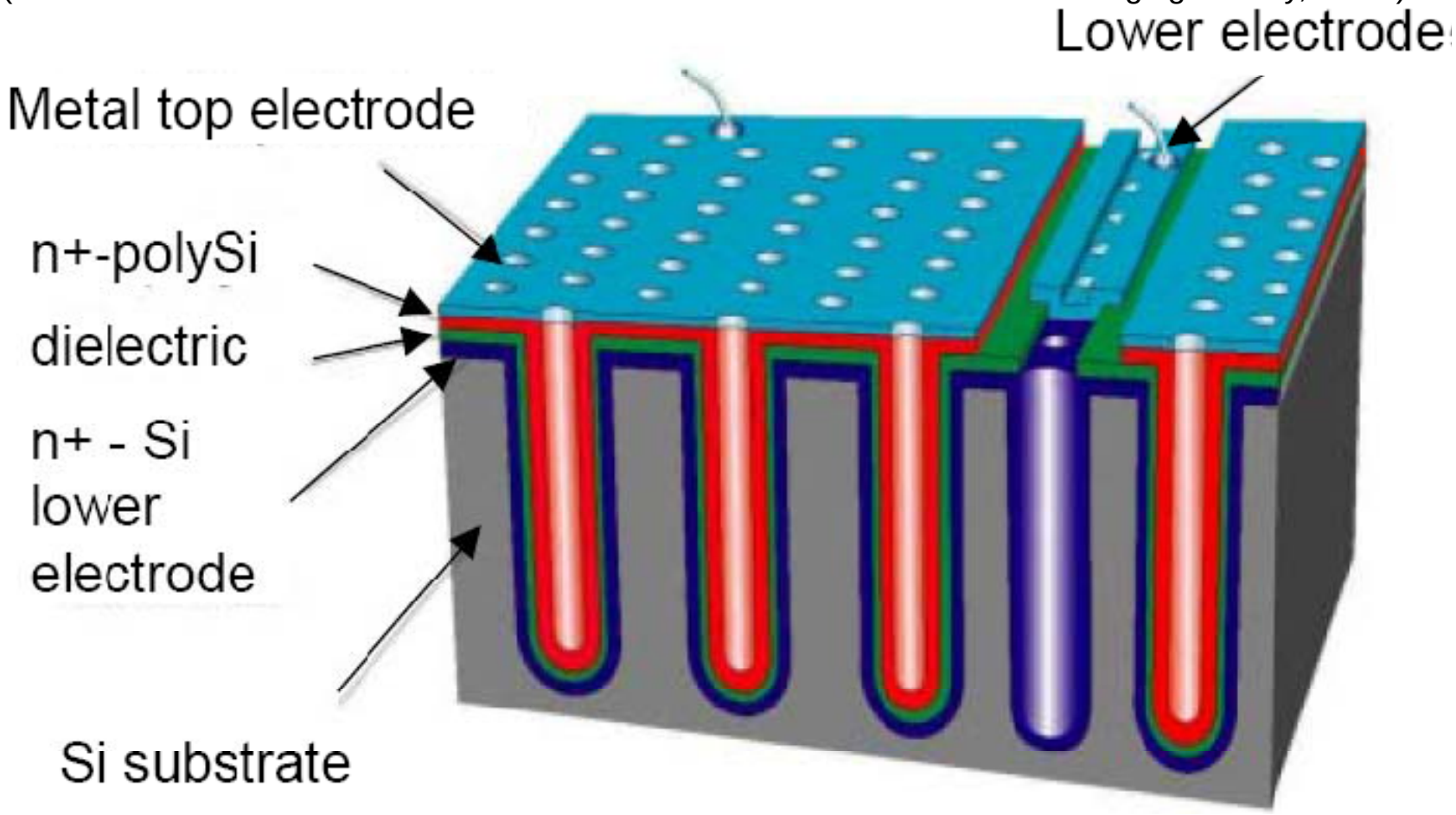
“Typical” MIS trench bypass capacitors suffer from large series resistance and consequent poor frequency response.

Structure of “typical” MIS type bypass trench capacitor with implanted bottom plate



Structure of high density RF MIS trench capacitor with laterally diffused bottom plate

(Extracted from F. Roozeboom et. al. -International Microelectronics and Packaging Society, 2001)



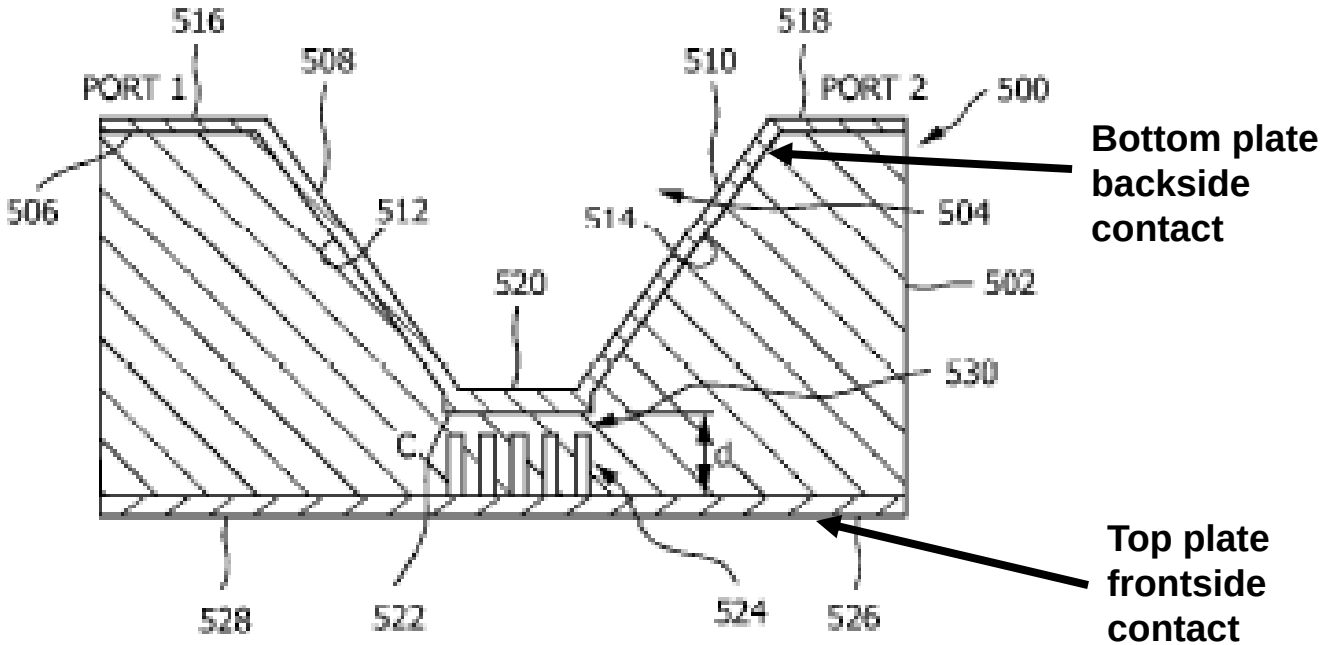
MIS Trench Capacitors

- **Diffused bottom plate trench capacitors lose their effectiveness as the capacitance per unit area increases, since the bottom plate resistance can become prohibitively large.**

- **As trench depth and capacitance per unit area increase further, low resistance access to the bottom plate becomes critical for high speed applications.**

Trench Capacitor Device Suitable for Decoupling Applications in High-Frequency Operation

Extracted from International Patent Publication Number WO 2007/054870 A1, May 2007



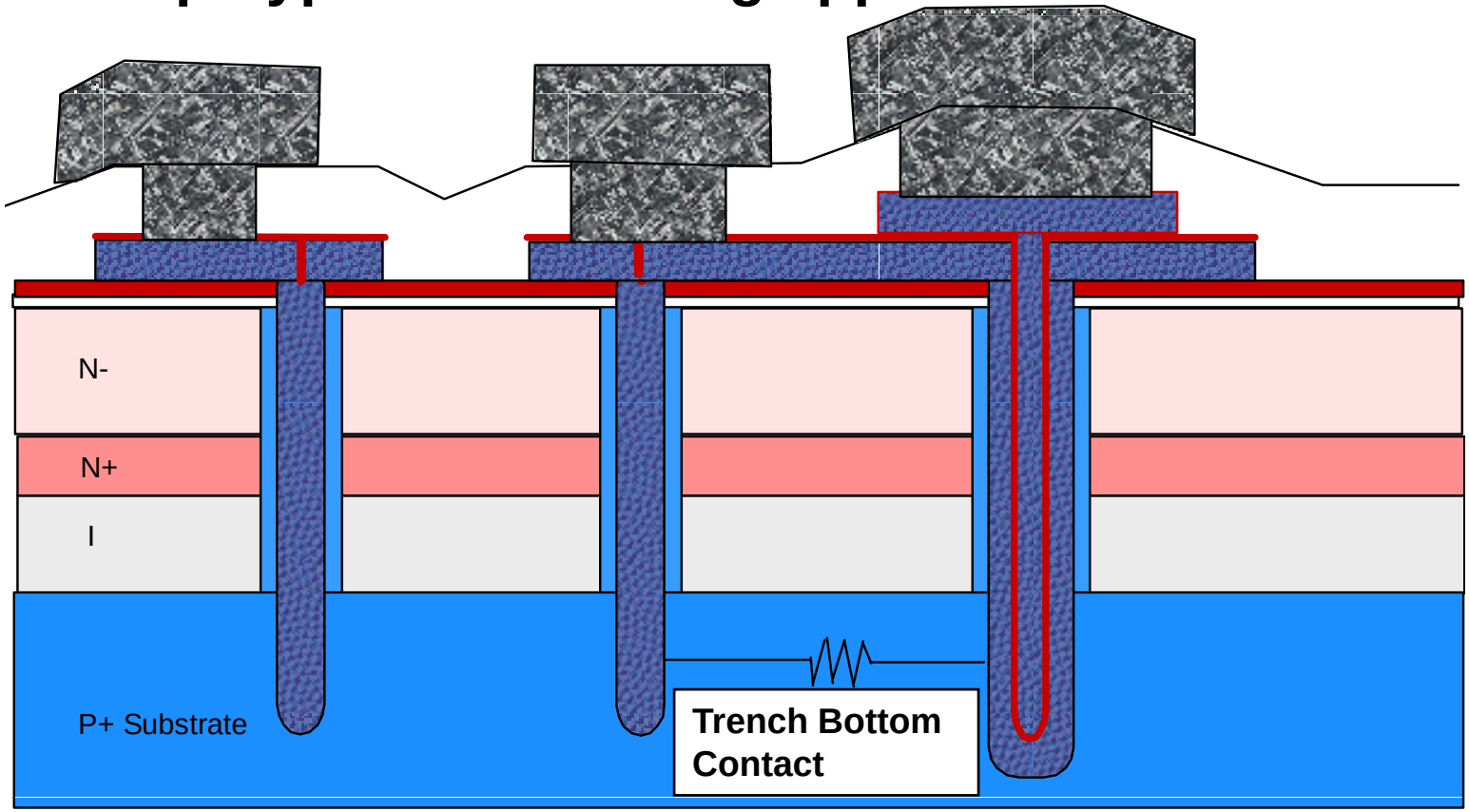
2. High frequency trench capacitors

a) MIS trench capacitors

b) High frequency “wrap-around” PIP capacitor

“Wrap-Around” PIP Capacitor

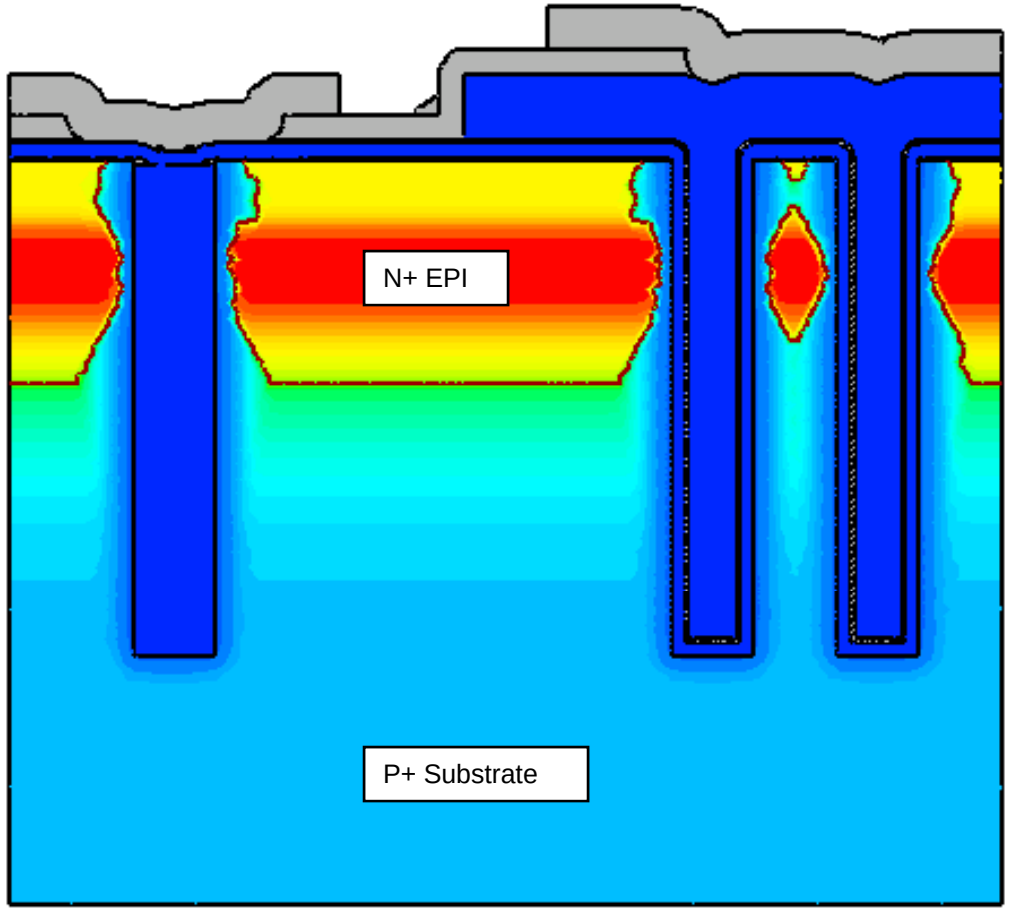
X-section view of “wrap-around” PIP capacitor for on-chip bypass and tuning applications



“Wrap-Around” PIP Capacitor

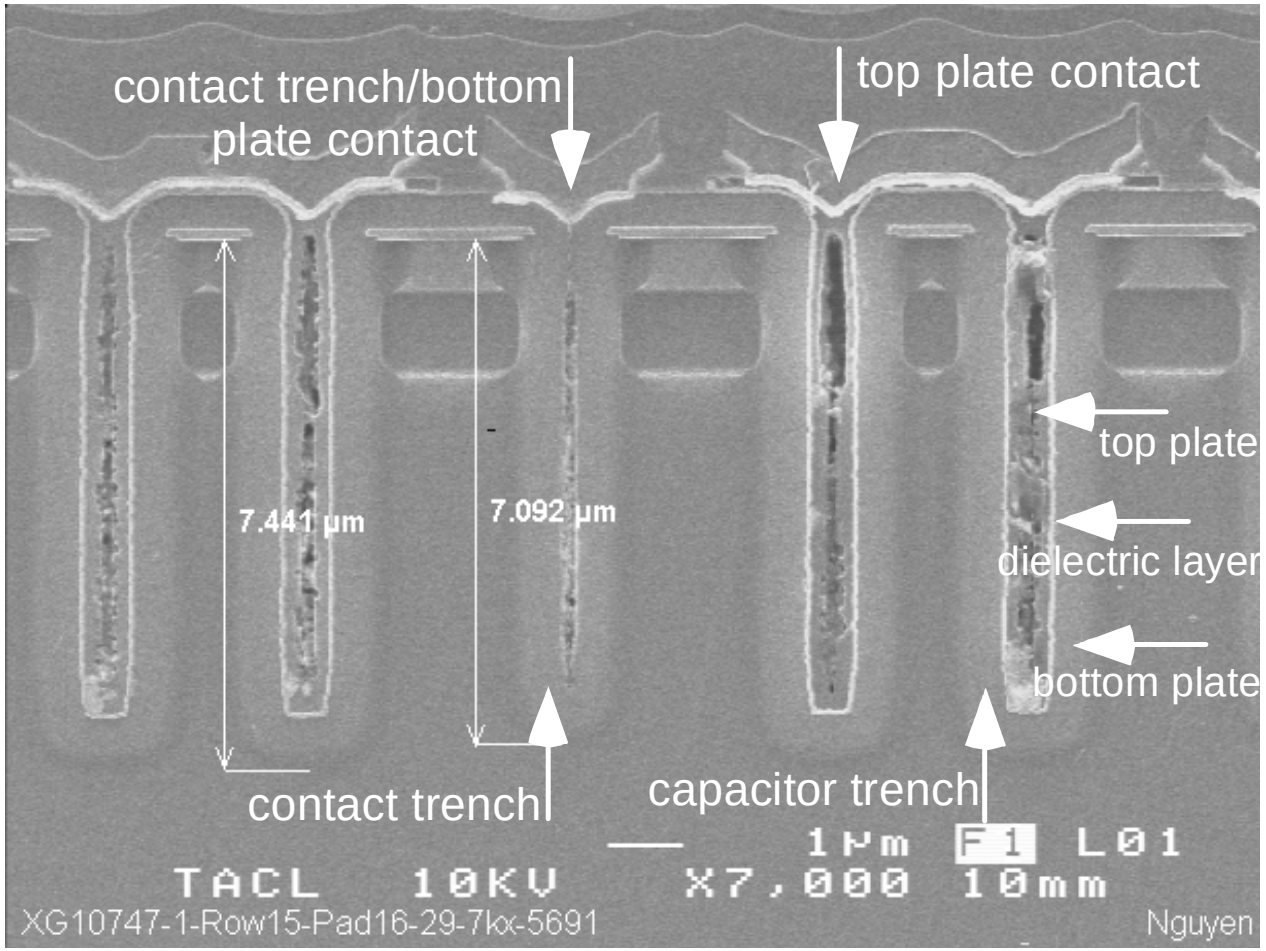
Diffusion model of trench bottom plate

- **The use of a highly-doped bottom liner poly electrode and the consequent outdiffusion makes this capacitor function even in the presence of highly-doped buried layers which may otherwise “break” the connection of the bottom electrode.**



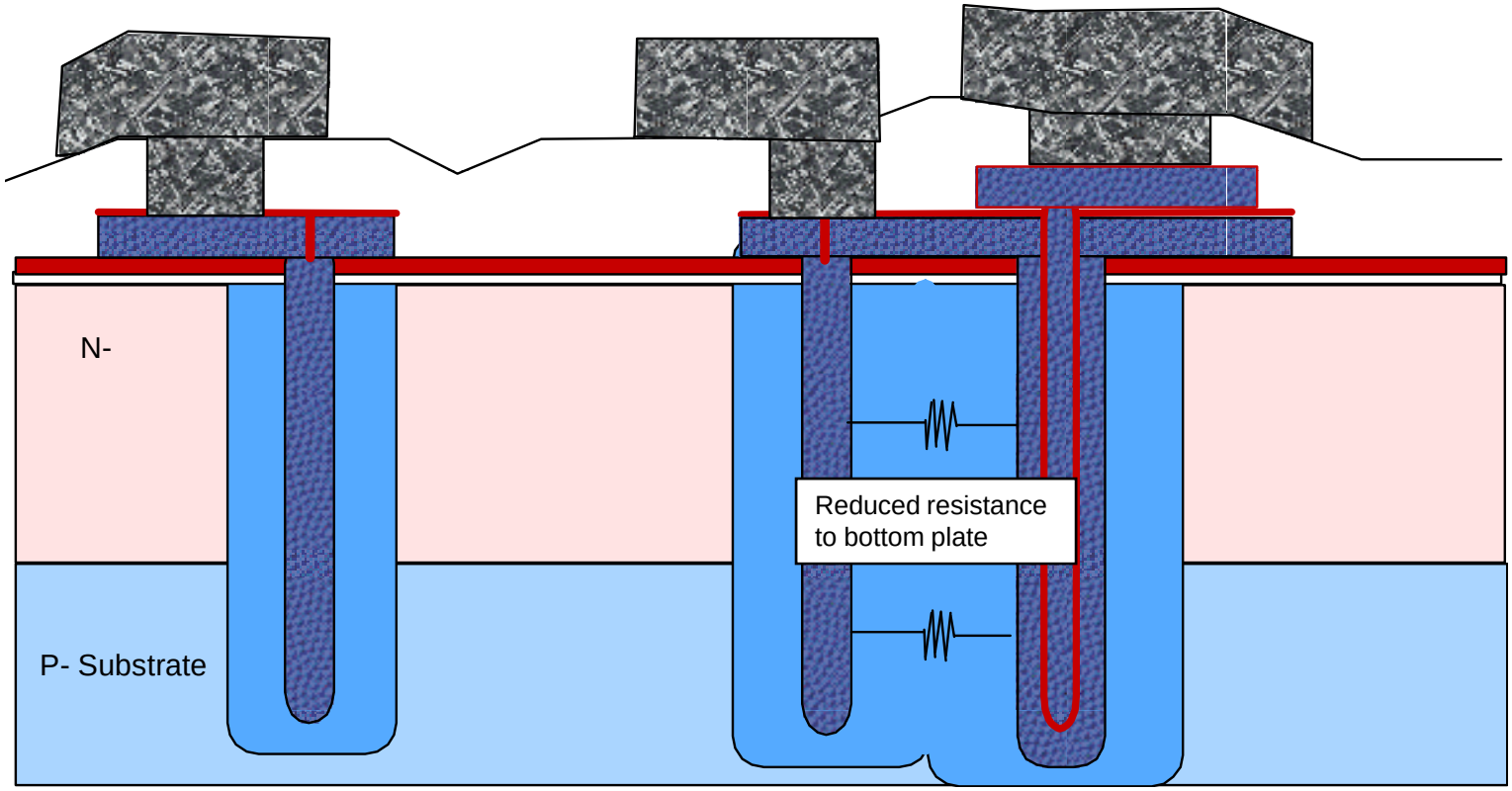
“Wrap-Around” PIP Capacitor

X-section view of “wrap-around” PIP cap



“Wrap-Around” PIP Capacitor

X-section drawing of “wrap-around” PIP capacitor in lightly doped substrate



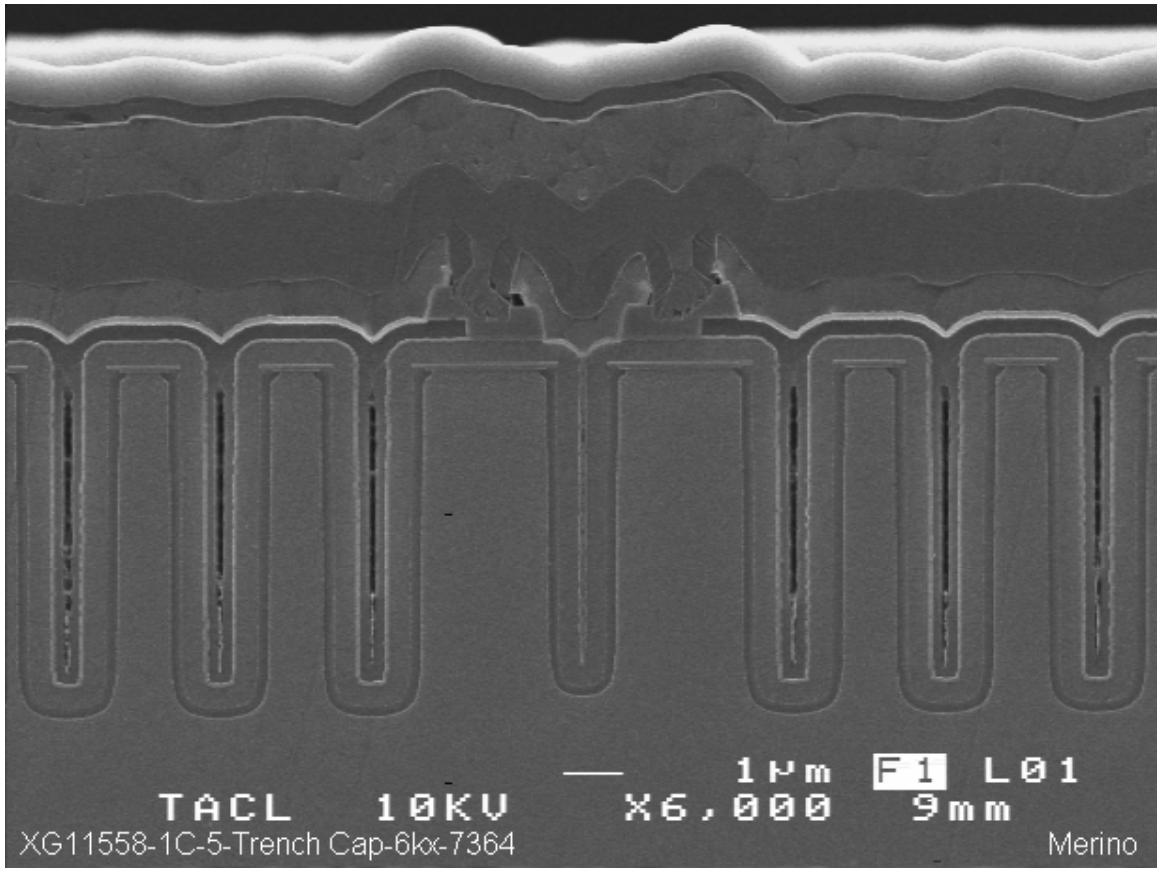
Substrate contact or isolation trench

Bottom plate contact trench

PIP capacitor “finger”

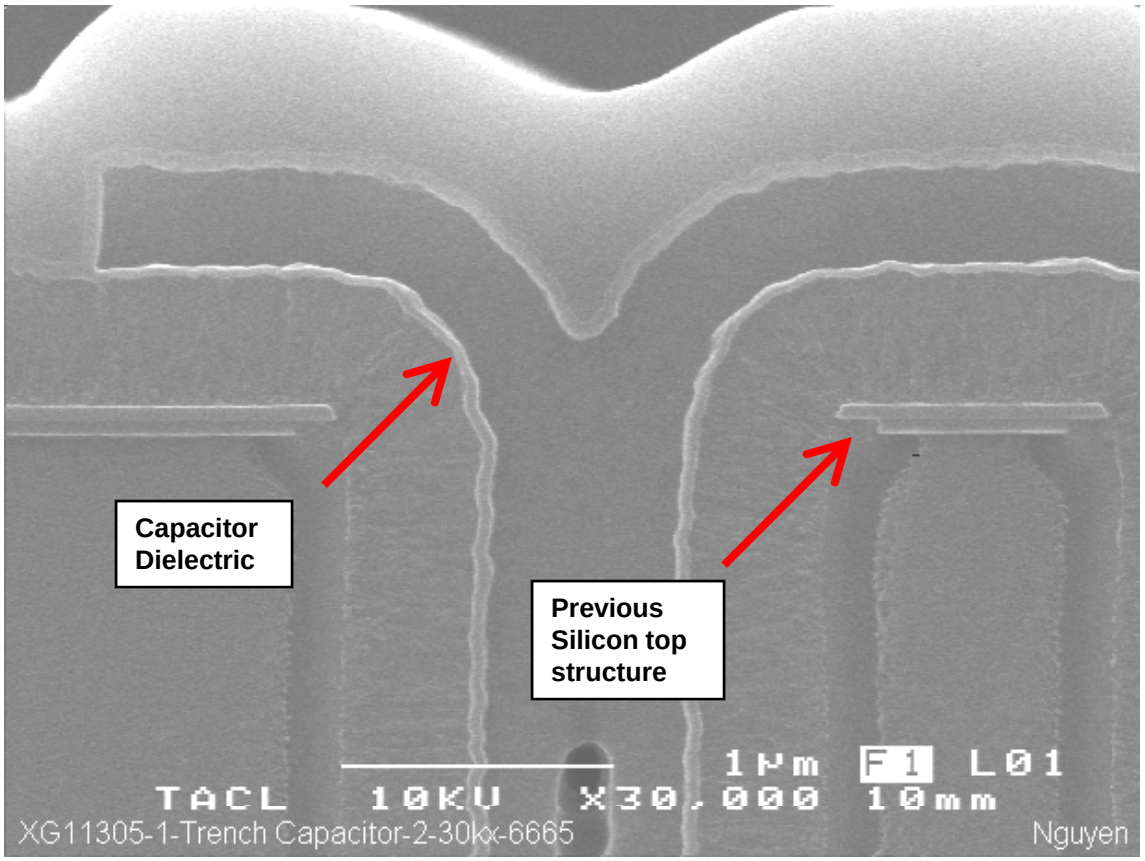
“Wrap-Around” PIP Capacitor

X-section SEM of “wrap-around” PIP capacitor in lightly doped substrate



“Wrap-Around” PIP Capacitor

- **The addition of a separate bottom plate enables “drop-in” capability irrespective of the substrate doping type, EPI layers, thermal budget, or substrate dielectric layers.**



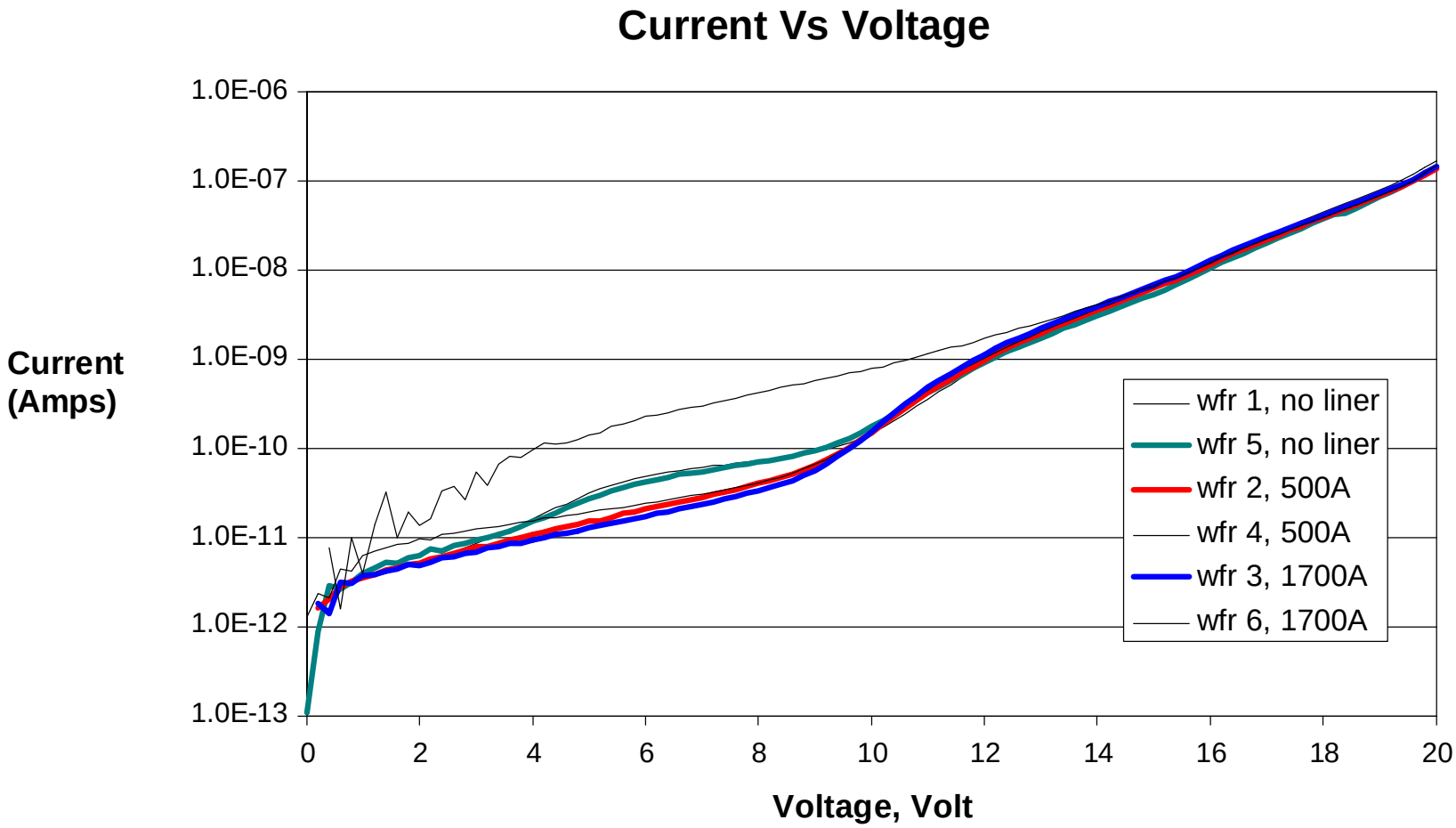
3. High frequency PIP capacitor characterization

a) Electrical characterization and modeling

b) Reliability evaluation

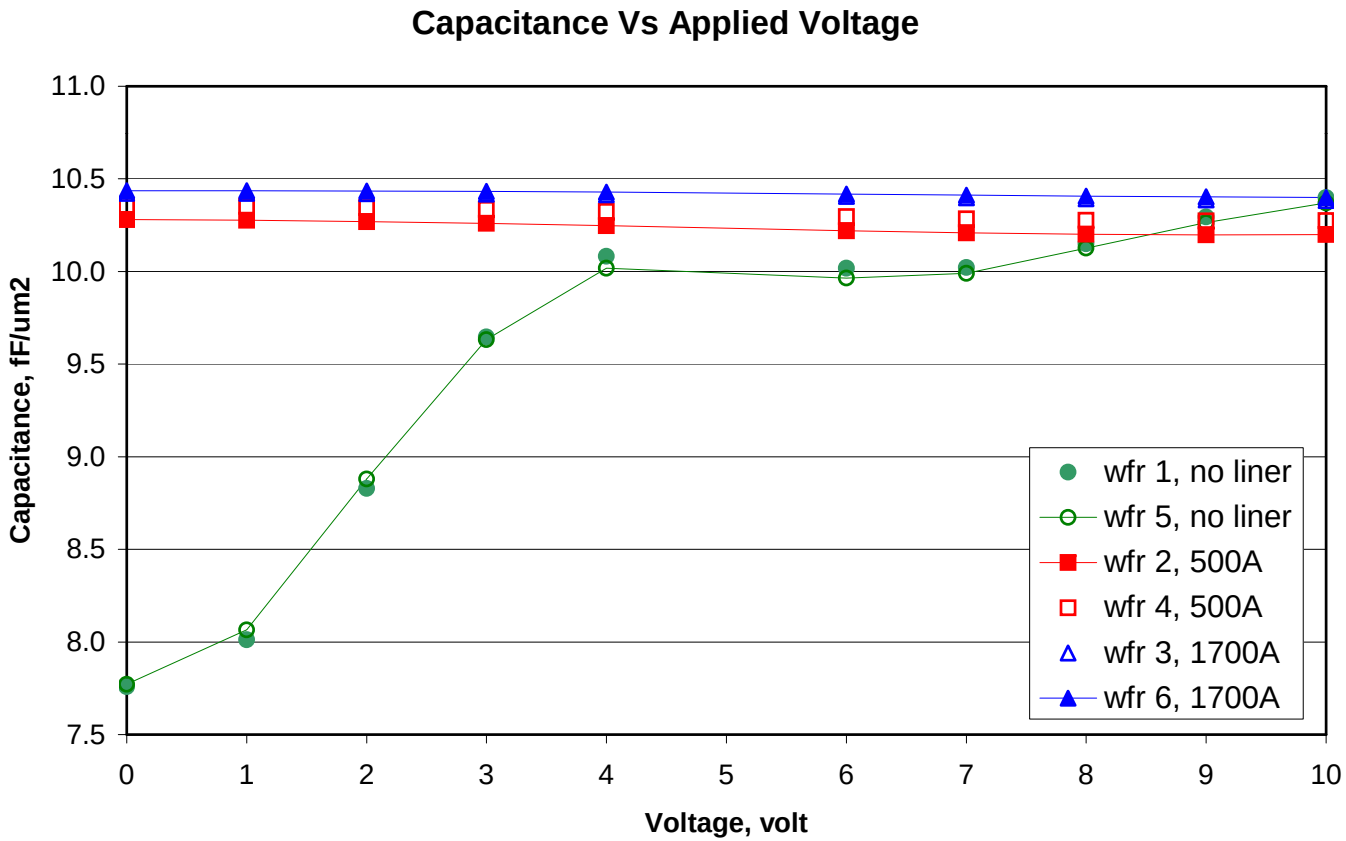
Electrical Characterization

Leakage comparison of MIS cap (no liner) on bare silicon substrate to PIP cap with bottom polysilicon liner



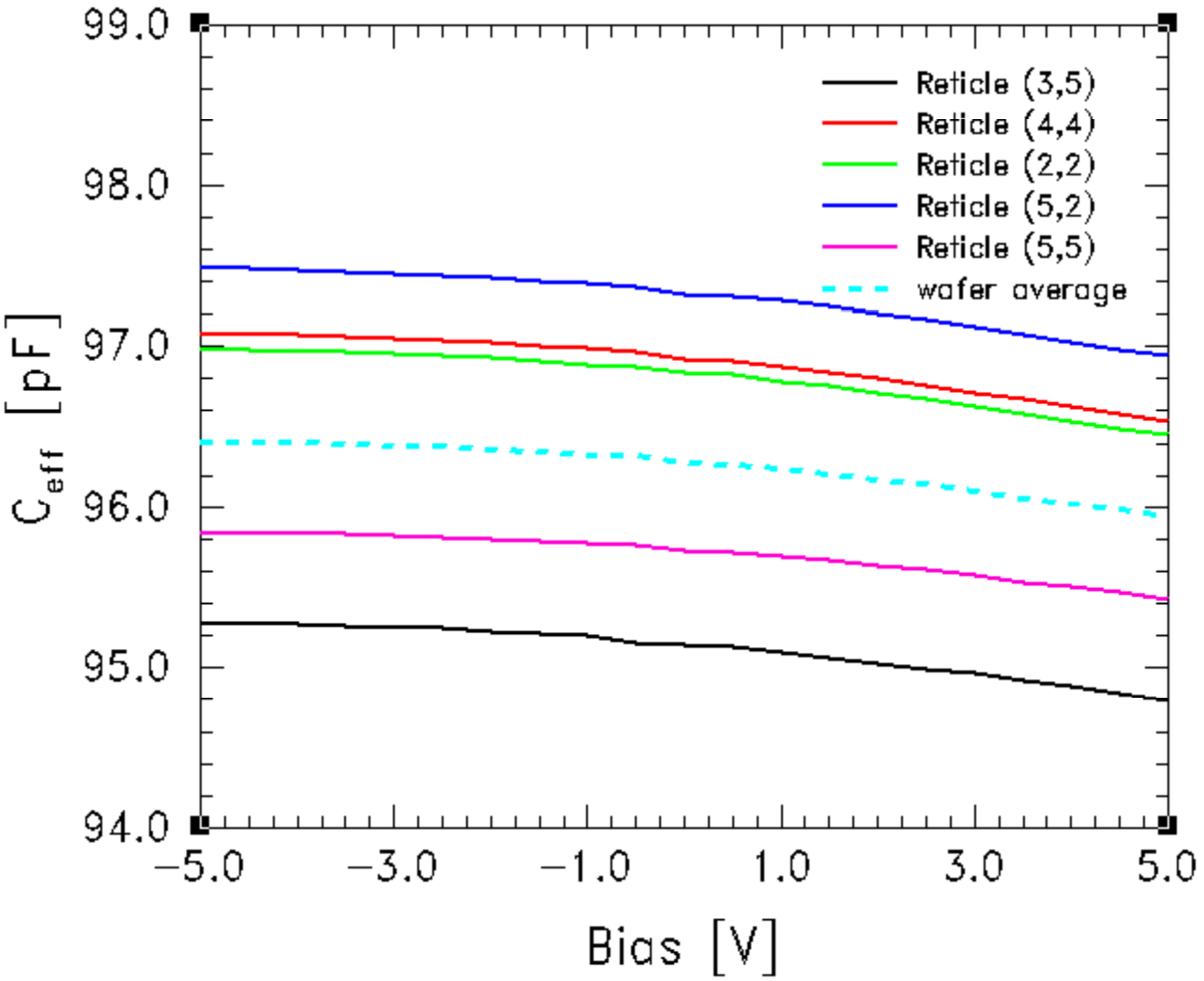
Electrical Characterization

Poly lined trench caps have improved linearity compared to standard MIS trench caps.



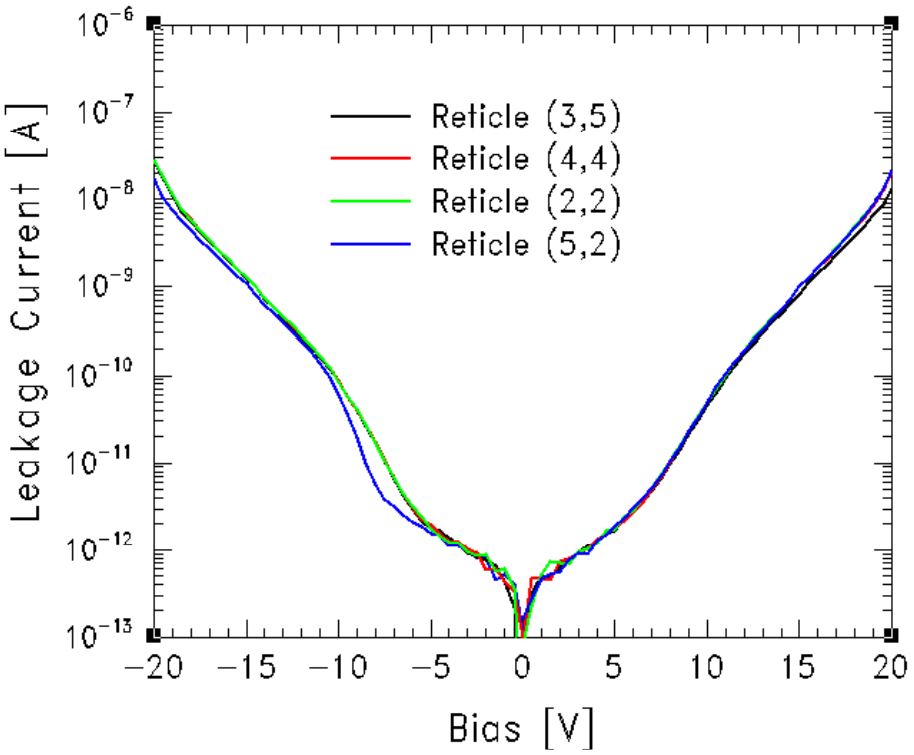
Electrical Characterization

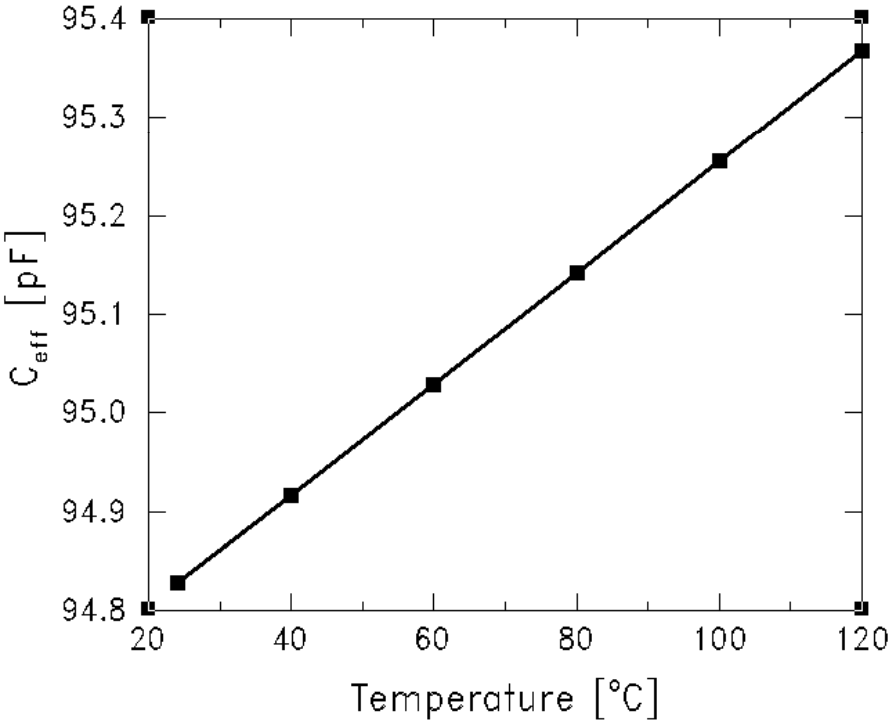
High linearity, good across-wafer uniformity (±1.25%)



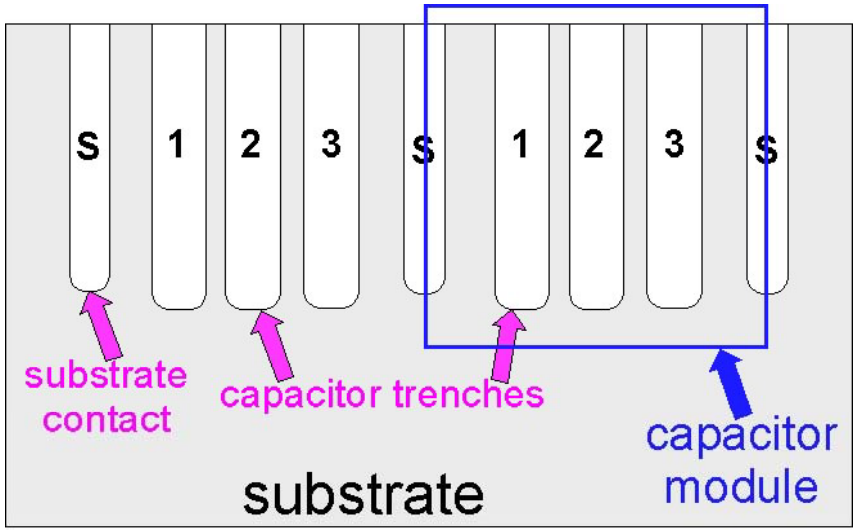
Electrical Characterization

Low leakage, excellent linearity over temperature





Device Modeling



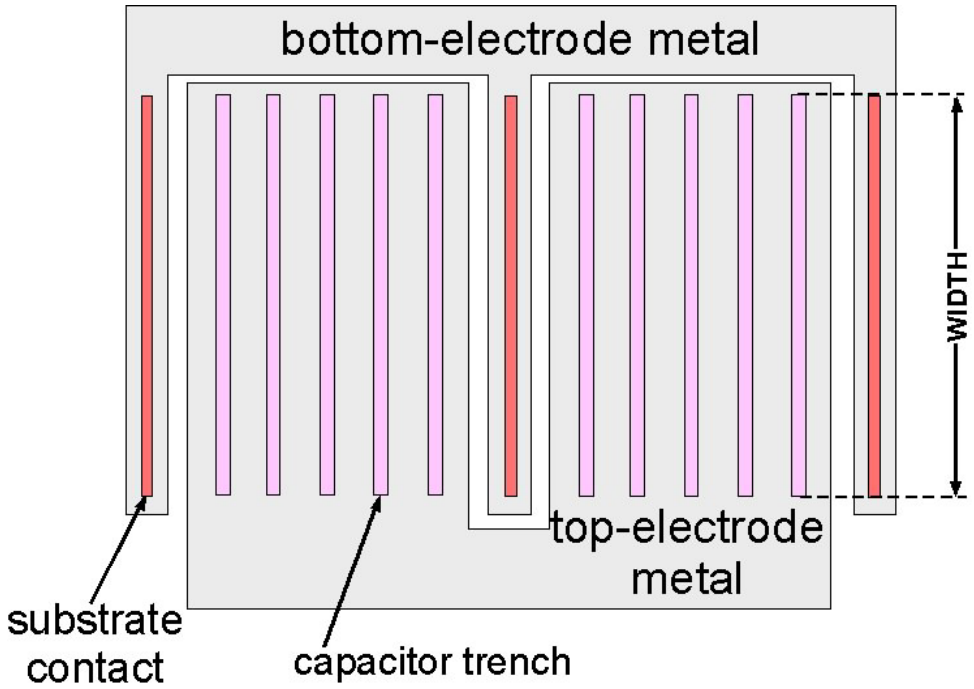
Cross-section

$n_{f\ (fingers)} = 3$,

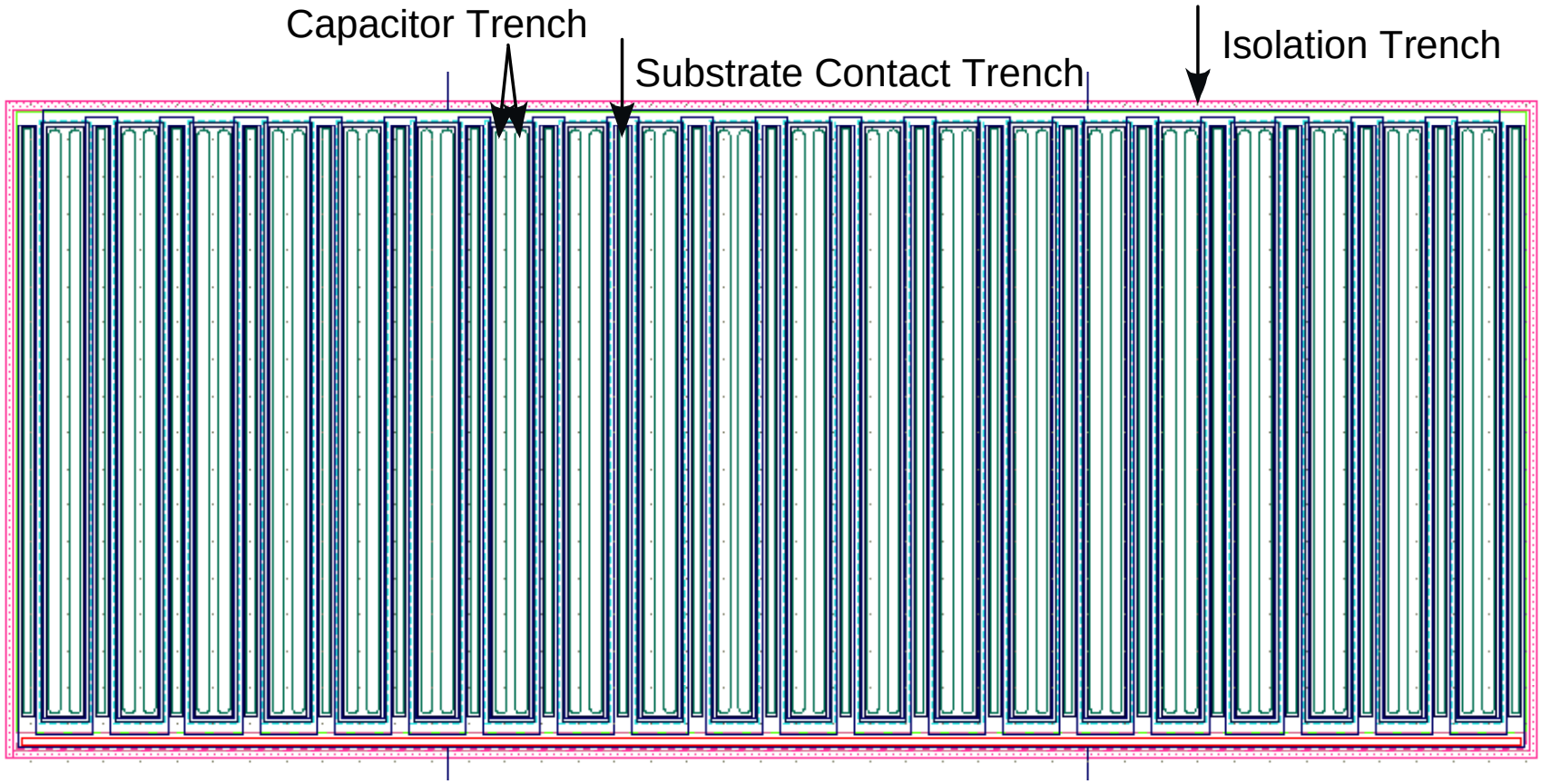
$n_{p\ (modules\ in\ parallel)} = 2$

Layout

$n_f = 5$, $n_p = 2$



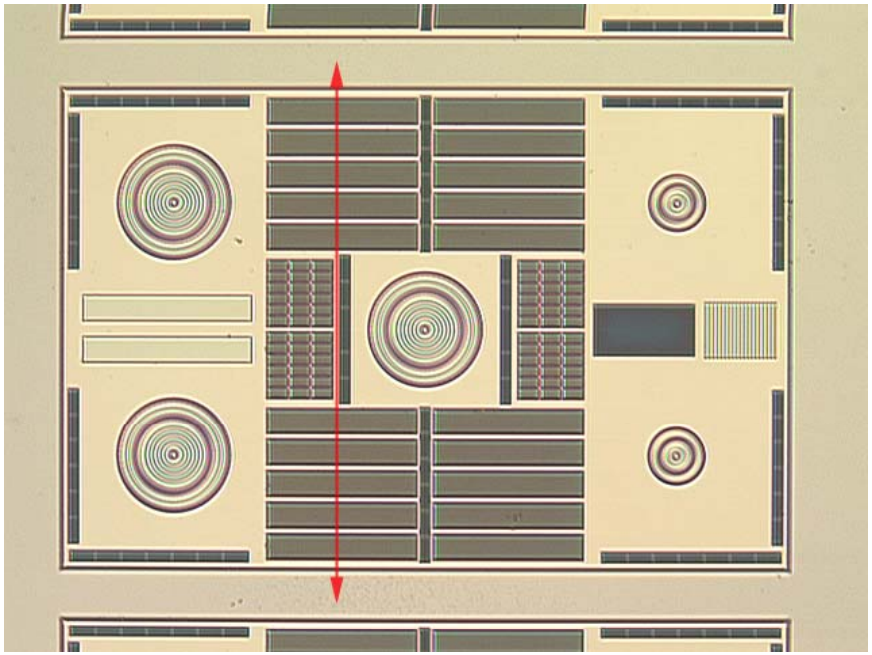
Very High Frequency Capacitor Layout n_f=2, n_p=20

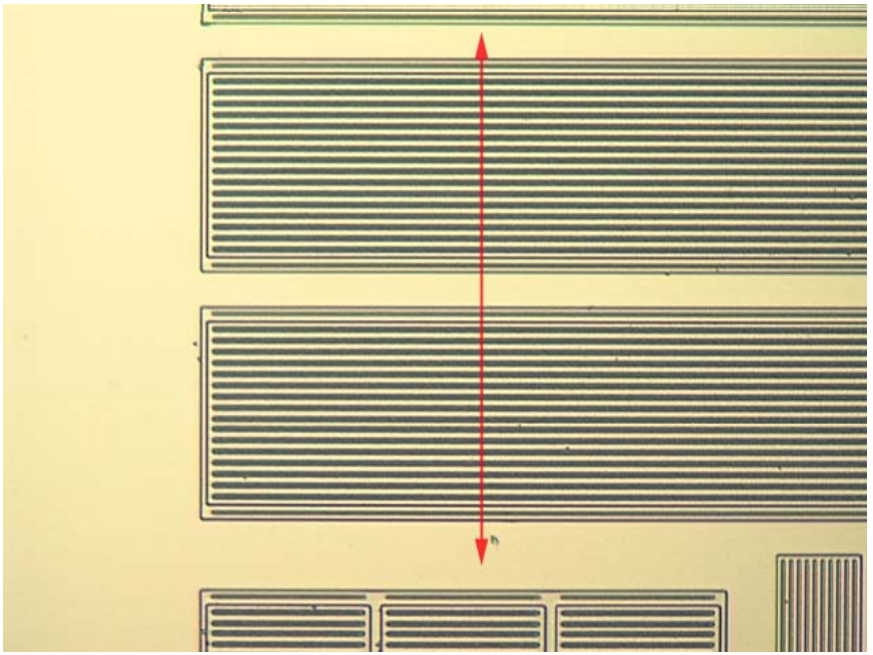


Device Modeling

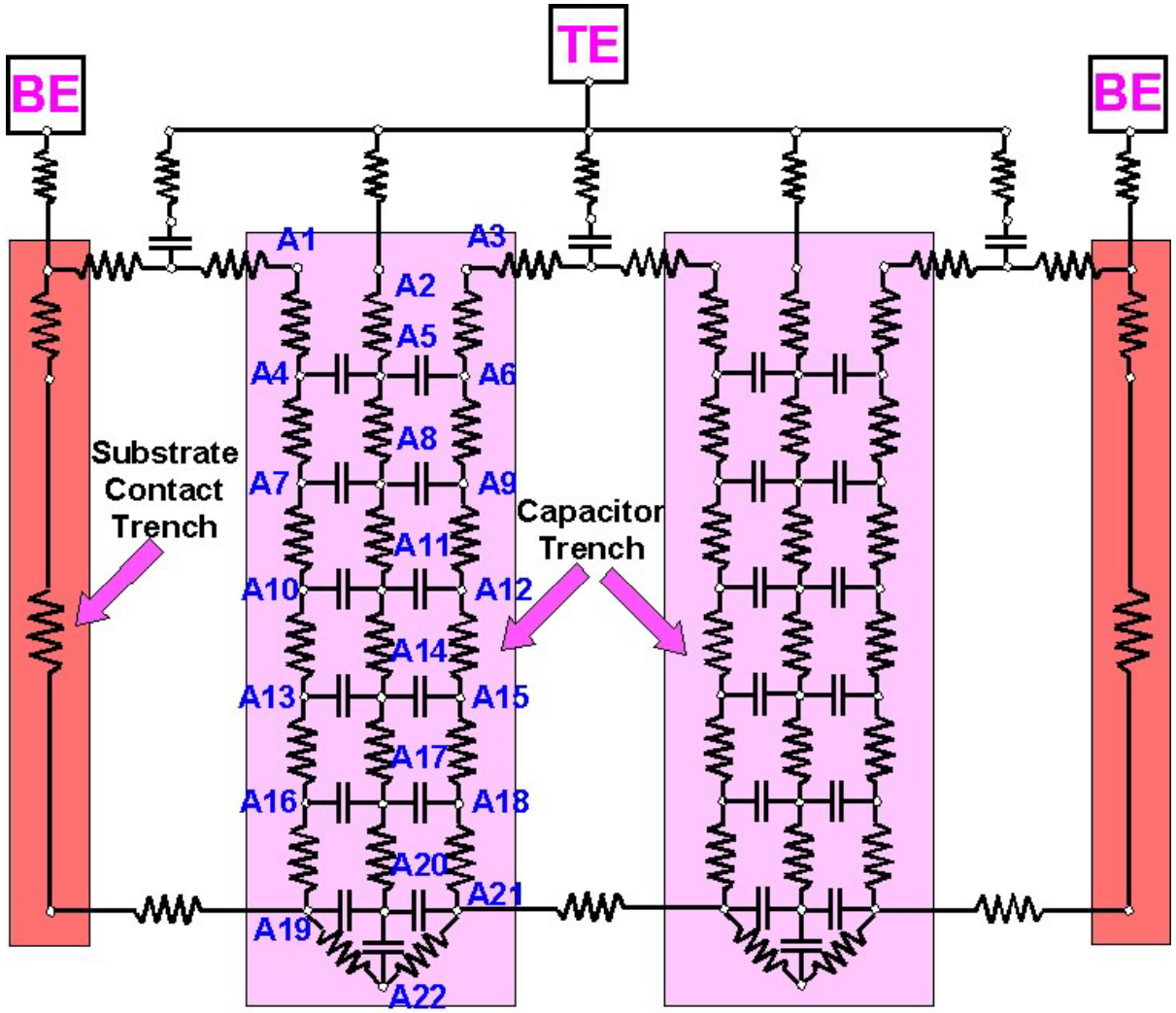
Reduced Frequency Capacitor for audio-band filter chip

$n_f=16,\ n_p=1$



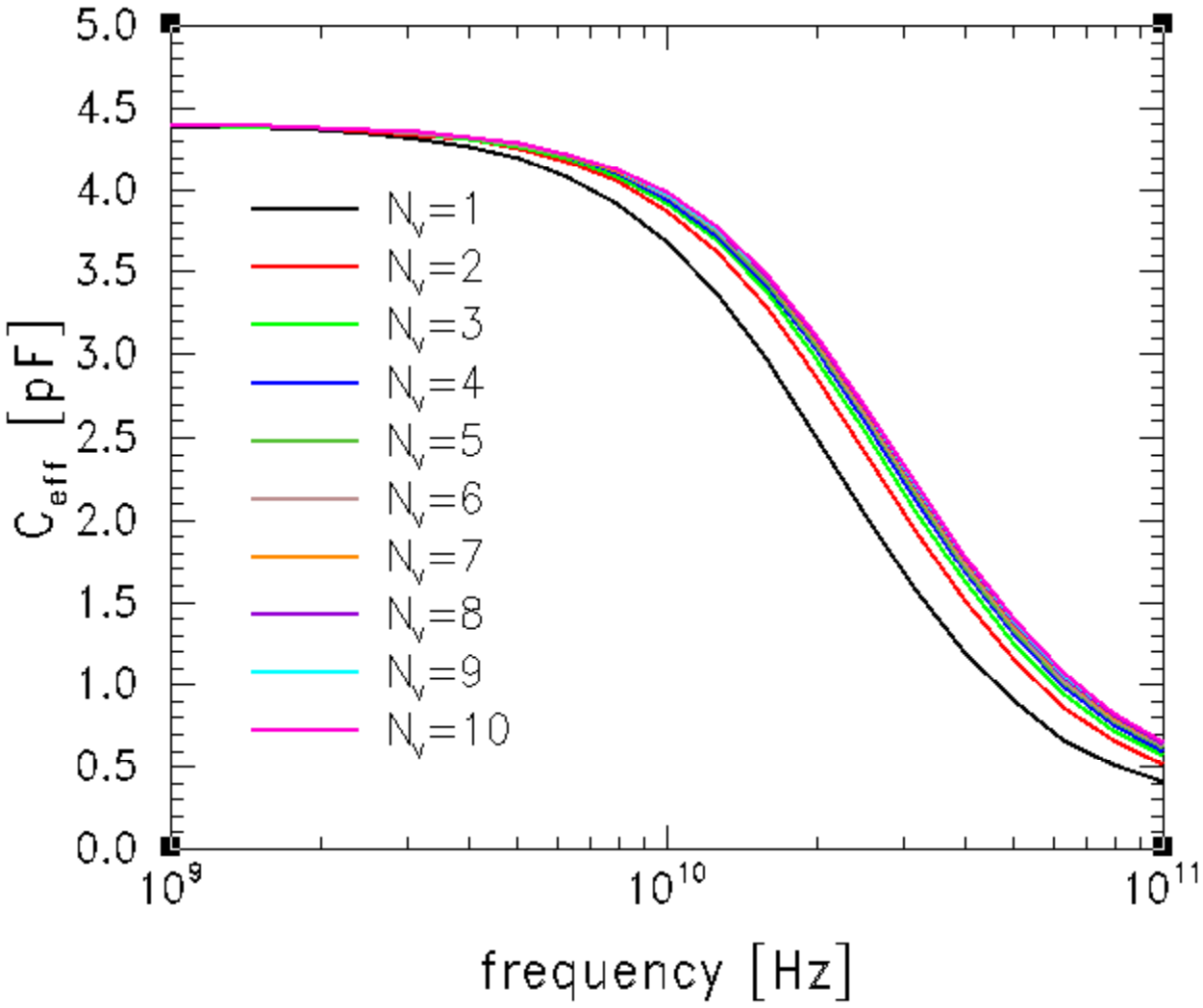


Device Modeling



Distributed R-C model for n_f=2, N_V=6. Metal inductance is optionally added.

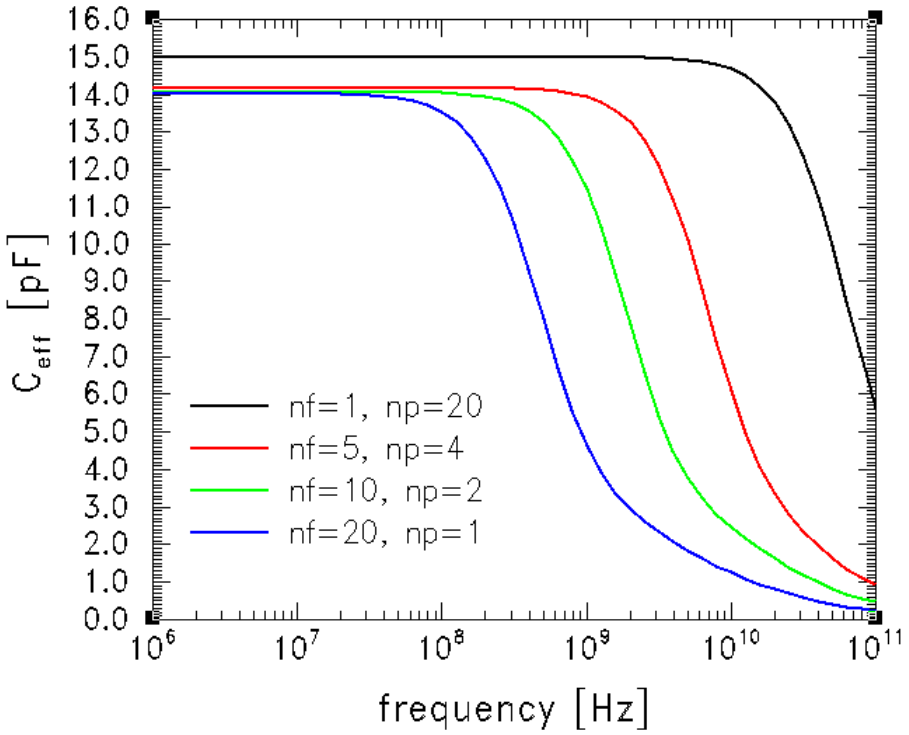
Device Modeling



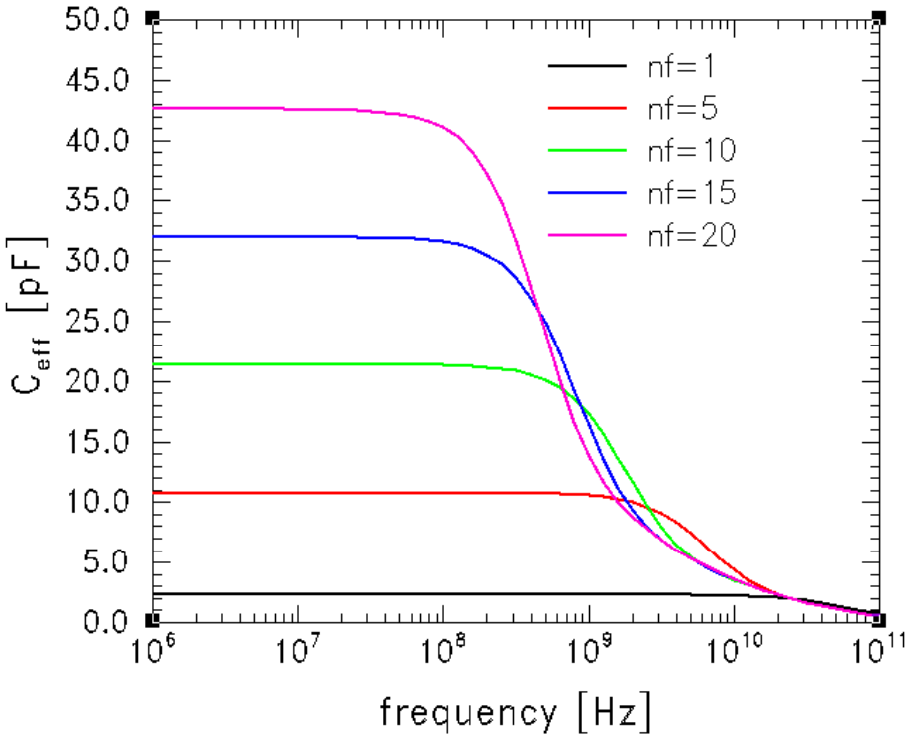
- **C_{eff}=Im(Yij)/(2πf), is the effective capacitance extracted from Y-parameters; it includes the effect of series resistance**

- **N_V~8 is sufficient for the model, *that is, eight vertical sections are enough for ensuring accuracy***

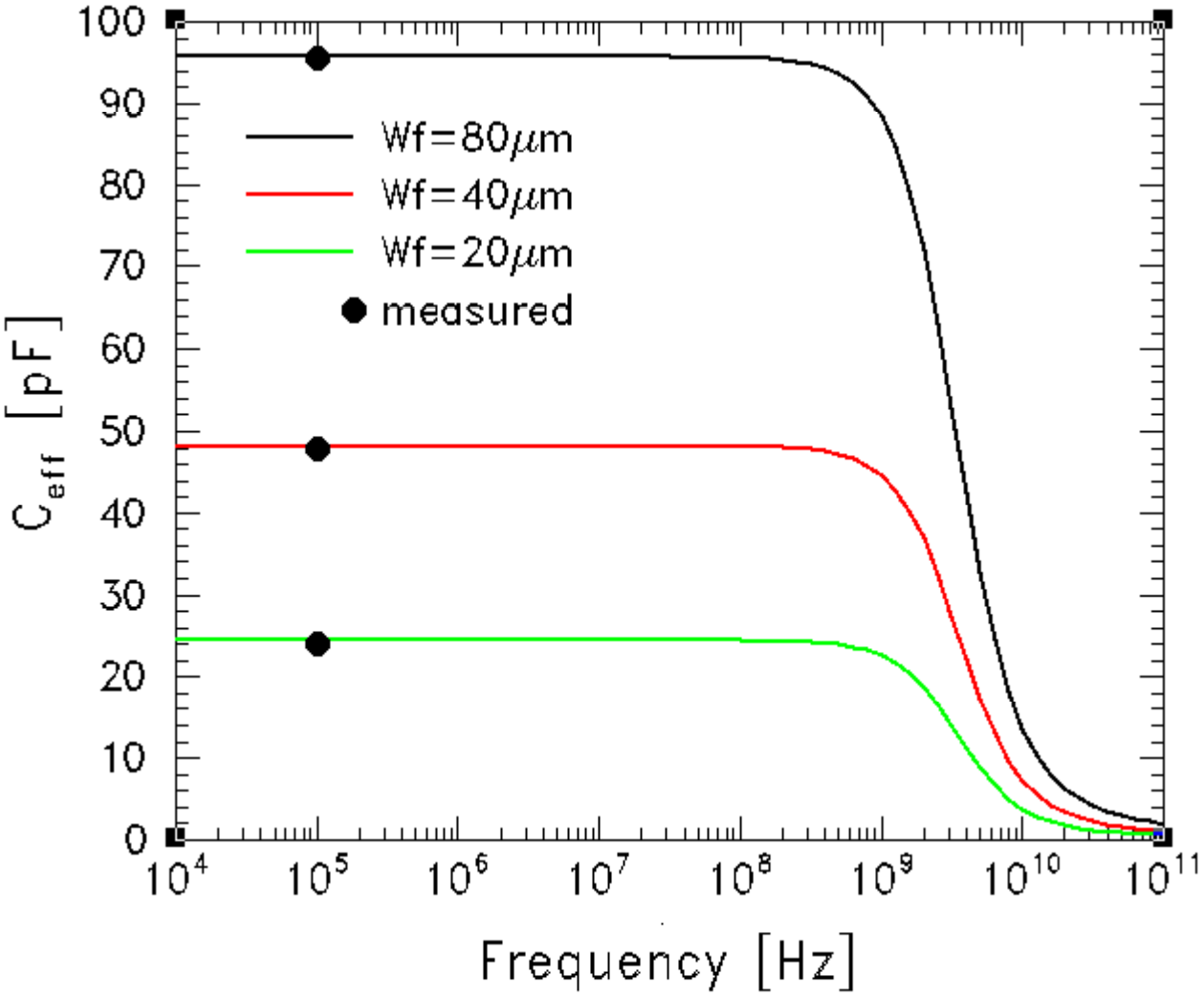
Device Modeling



- **A given target capacitance is obtained by a combination of fingers and parallel sections.**
- **The lower n_f is, the better is the frequency response.**

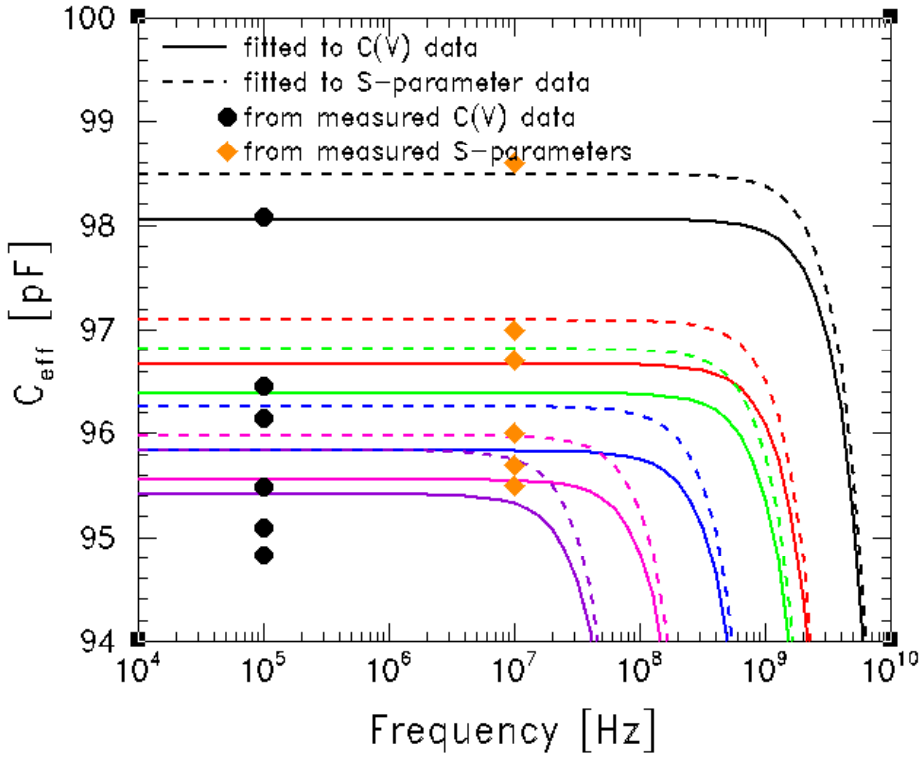


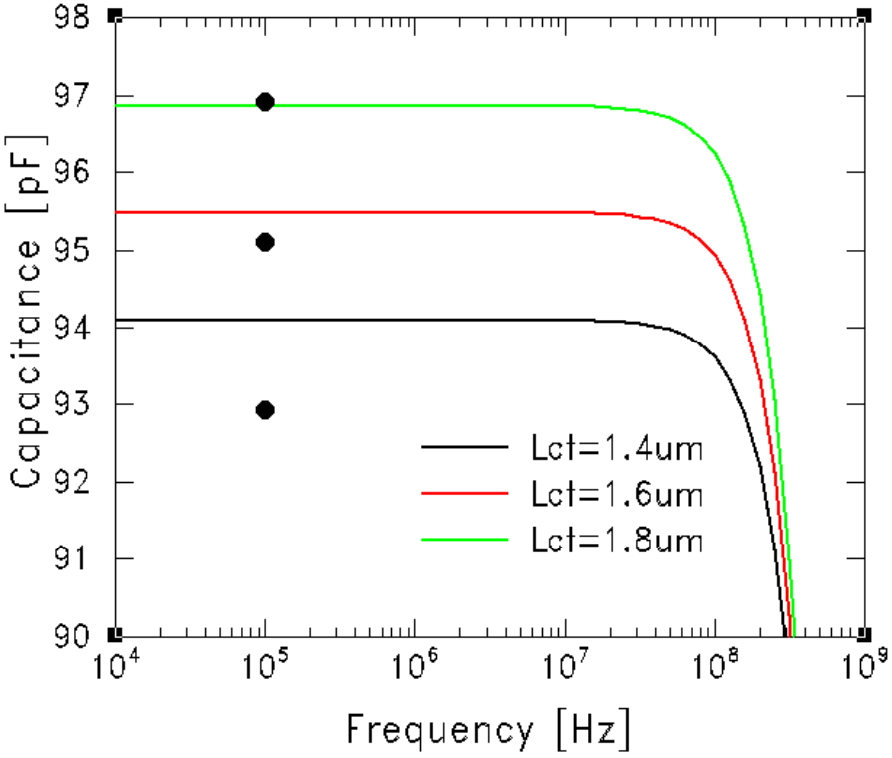
Model-Extraction



- **Pseudo-2D treatment is valid for the widths under consideration**

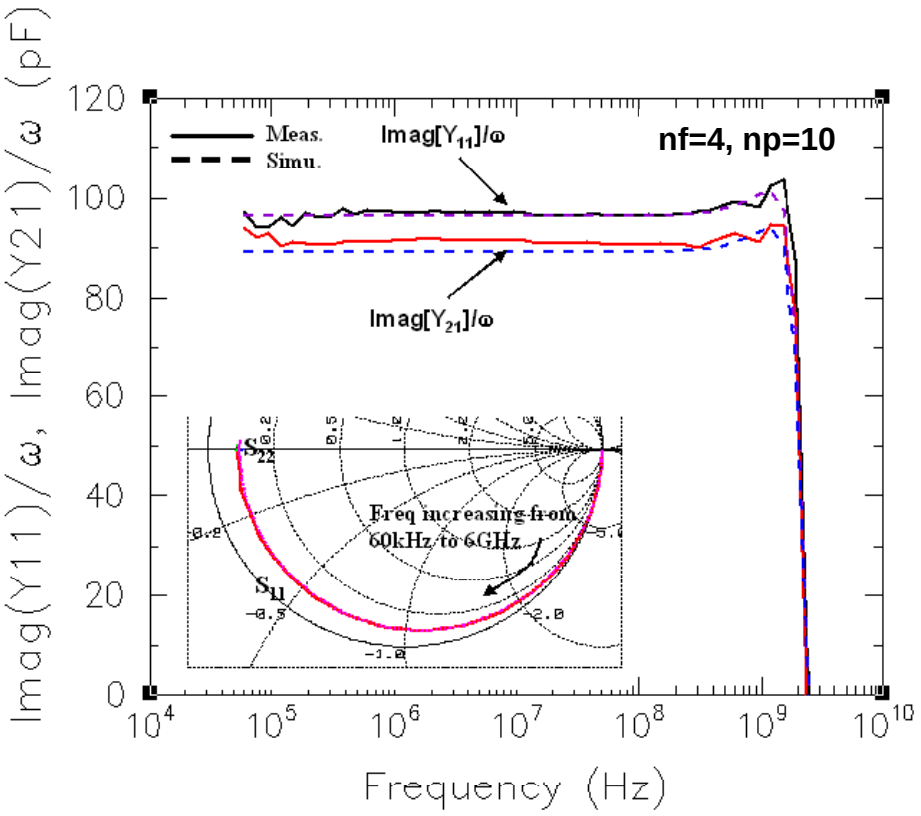
Model Extraction

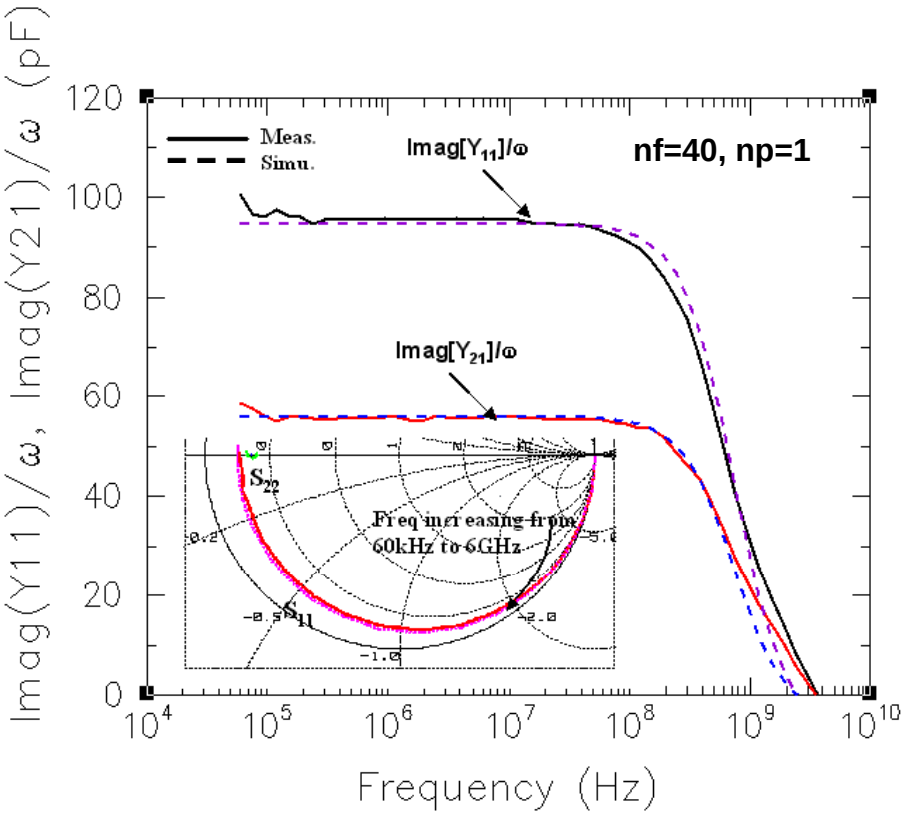




- **A low-frequency fit is first obtained: only 1-2 parameters are tweaked; the rest are geometry-based**
- **Y-parameters obtained from LCR meter and Spectrum Analyzer**

Model Extraction





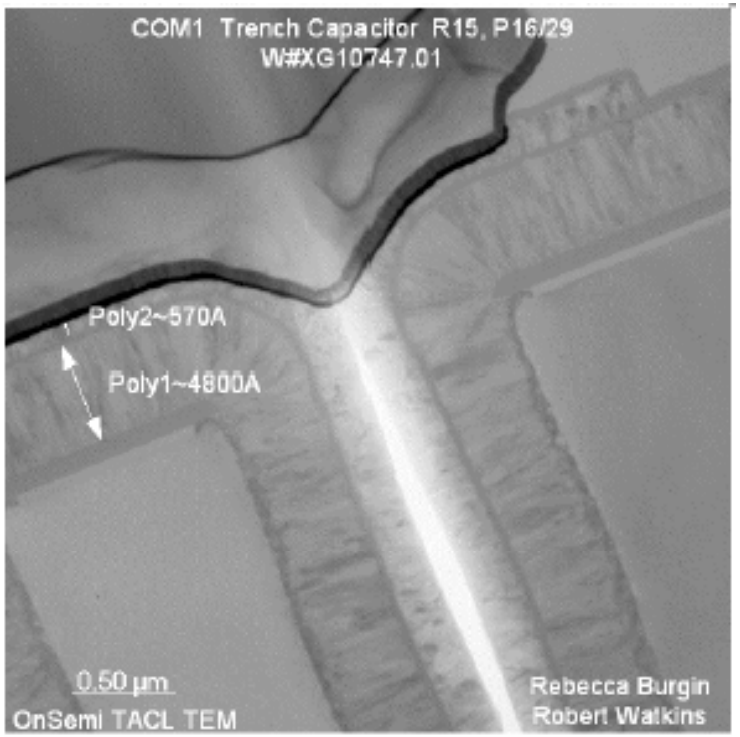
- **RF parameter extraction requires S-parameter data from 2-port GSG measurements**
- **Device asymmetry can predicted using lumped element model**
- **Correctly modeling substrate resistance is very important**

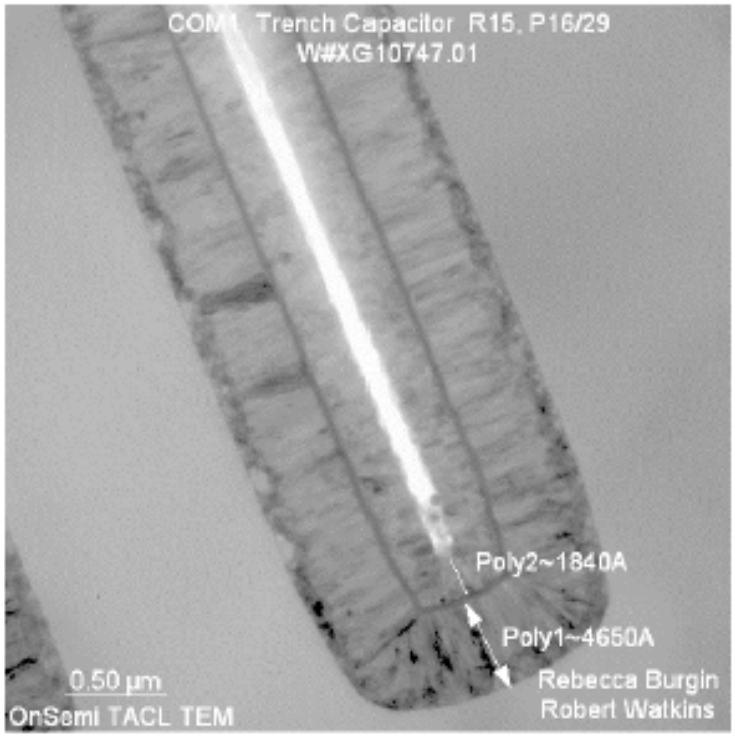
3. High frequency PIP capacitor characterization

a) Electrical characterization and modeling

b) Reliability evaluation

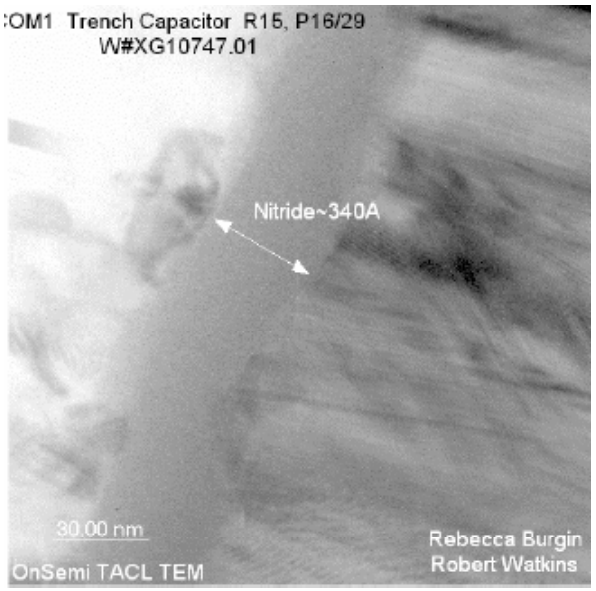
TEM Construction Analysis



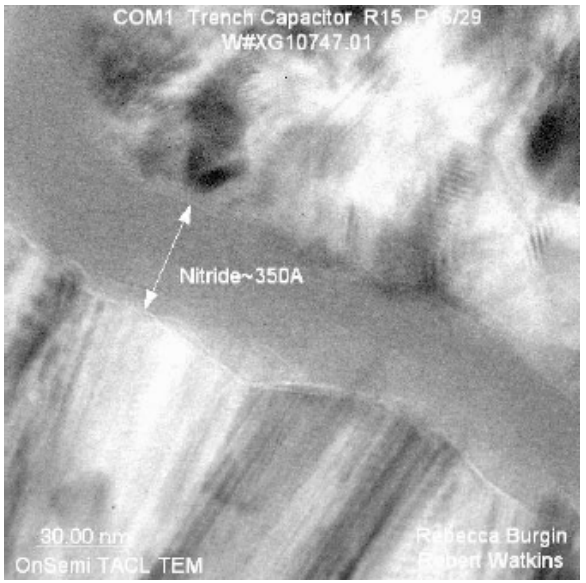


Reliability Evaluation

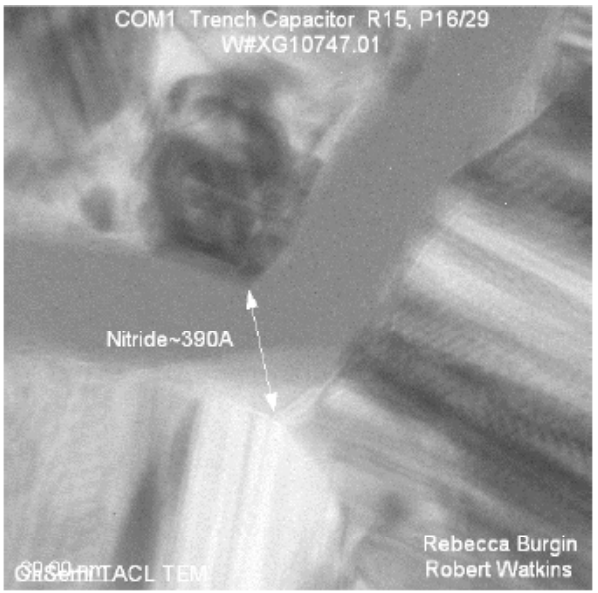
TEM Evaluation of Capacitor Dielectric



Trench Sidewall

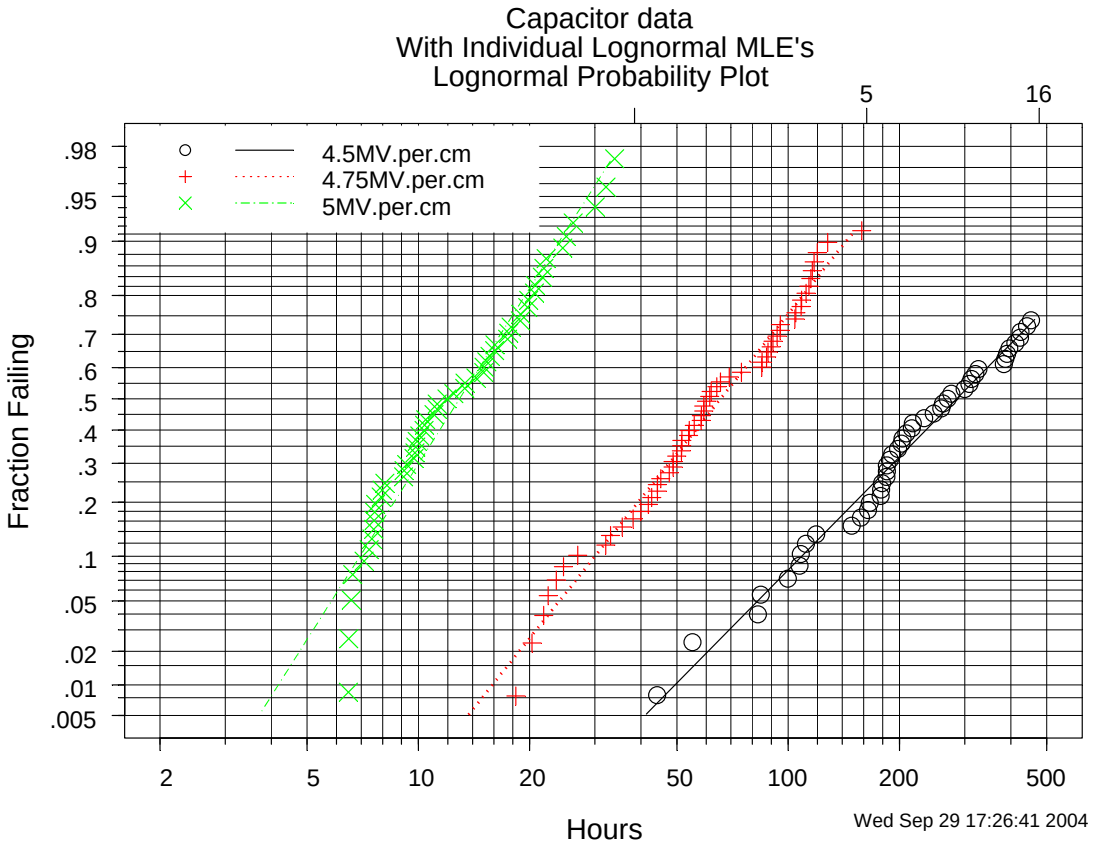


Trench Bottom

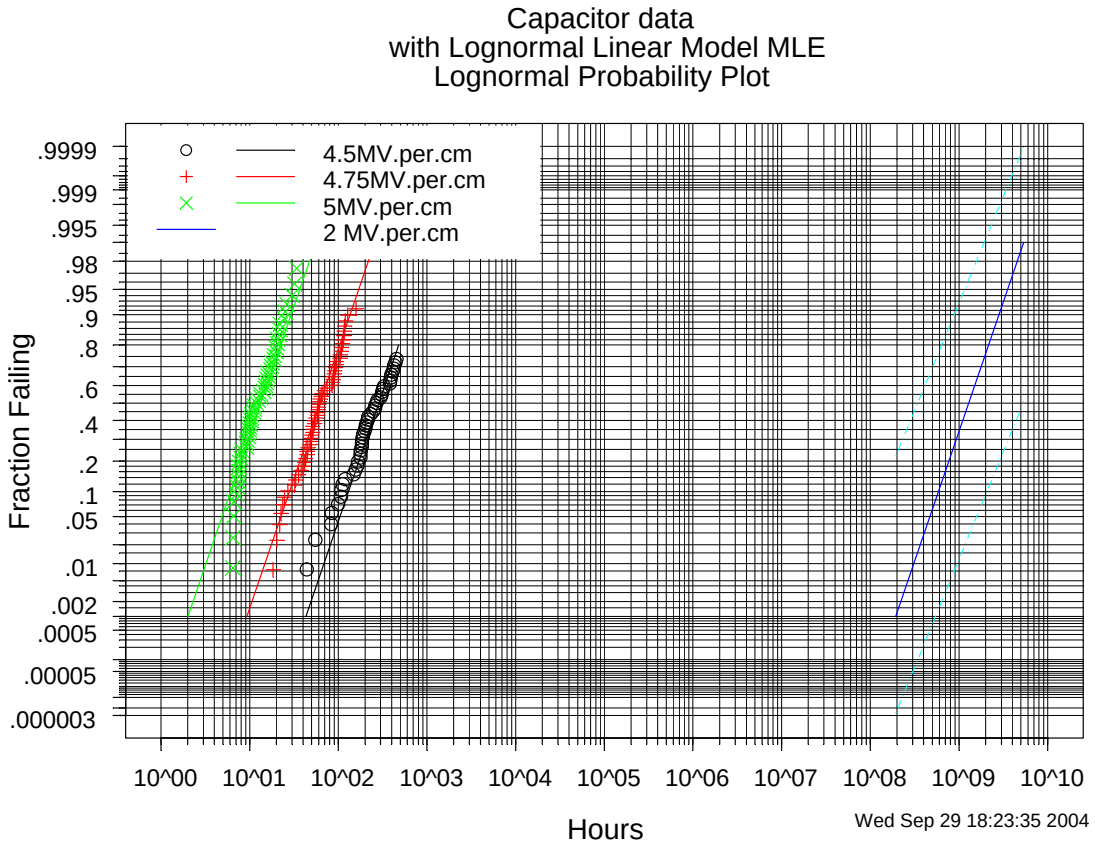


Trench Bottom “Corner”

Lognormal Distributions of Intrinsic TDDB Failures



Maximum Likelihood Fit
Extrapolation to 10 V @ 150 °C



Reliability Evaluation

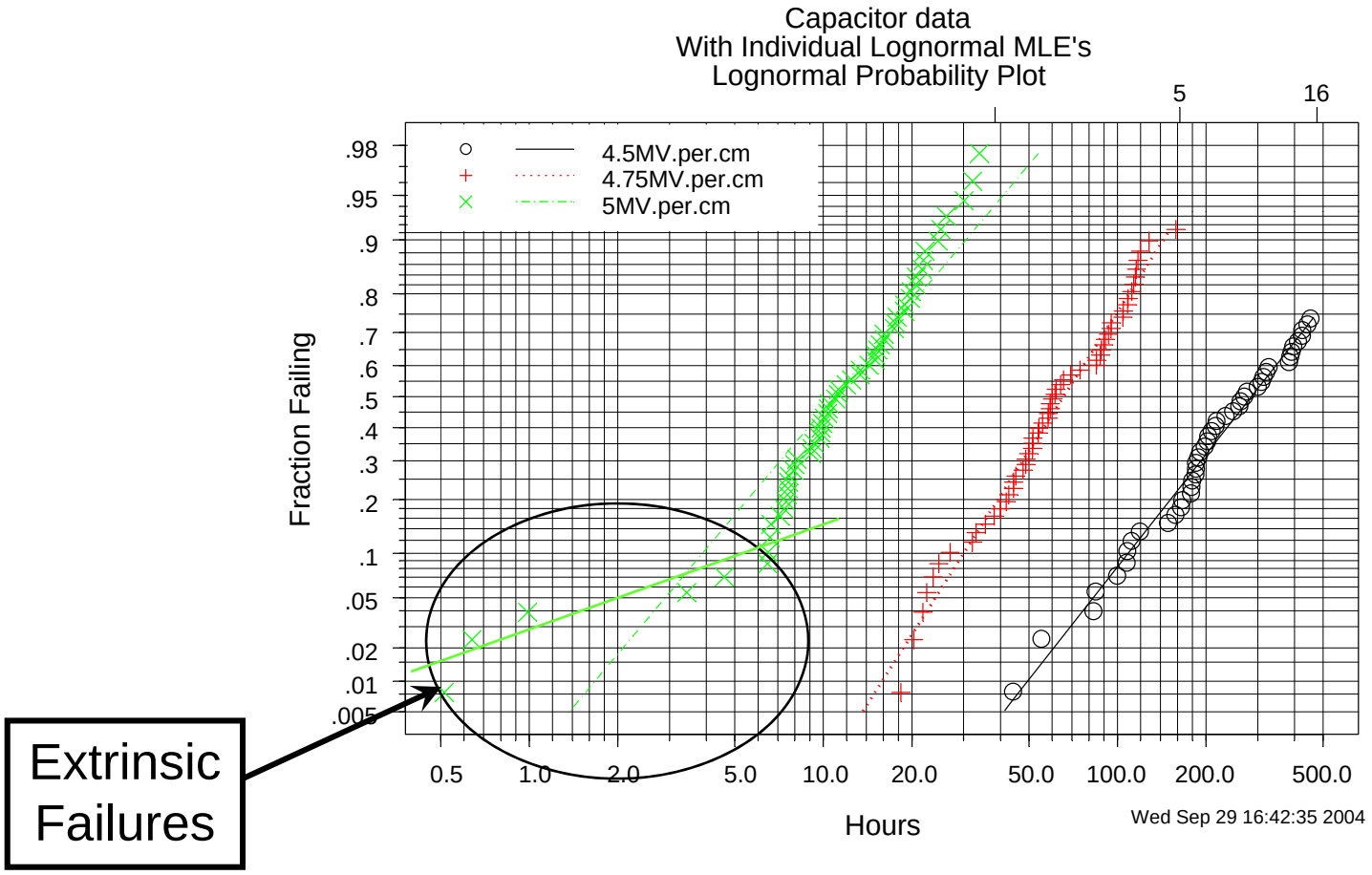
Lifetime Estimates 10 V @ 150 °C

- Quantile Estimates
- From Capacitor data at 2 MV.per.cm
- Lognormal MLE and Pointwise Approximate 90% Confidence Intervals

7,895 years

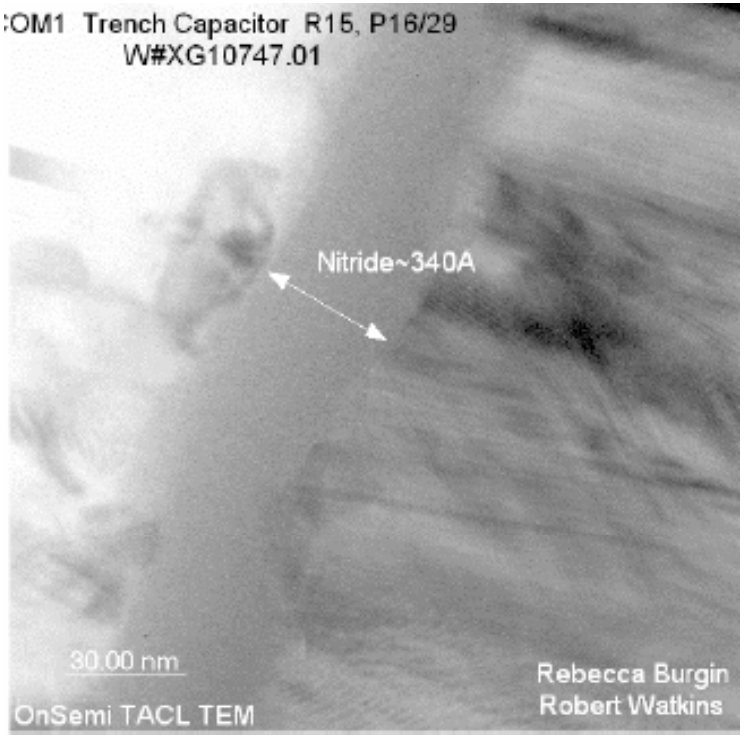
p	Quanhat	Std.Err.	90% Lower	90% Upper
0.001	193509360	121049290	69157870	5.415e+008
0.005	265309753	165510803	95085143	7.403e+008
0.010	309187546	192684448	110928051	8.618e+008
0.050	469668005	292159050	168820772	1.307e+009
0.100	586927866	364961308	211052126	1.632e+009
0.200	768766377	478075427	276413038	2.138e+009
0.300	933922386	581039386	335643103	2.599e+009
0.400	1102876638	686586047	396108502	3.071e+009
0.500	1288325603	802673961	462337302	3.590e+009
0.600	1504957855	938577225	539528708	4.198e+009
0.700	1777217127	1109797762	636294633	4.964e+009
0.800	2159021141	1350632142	771571247	6.041e+009
0.900	2827916269	1774365391	1007511006	7.937e+009
0.990	5368207358	3399989142	1894045950	1.521e+010

Lognormal Distributions
Extrinsic Failure Mode Evident

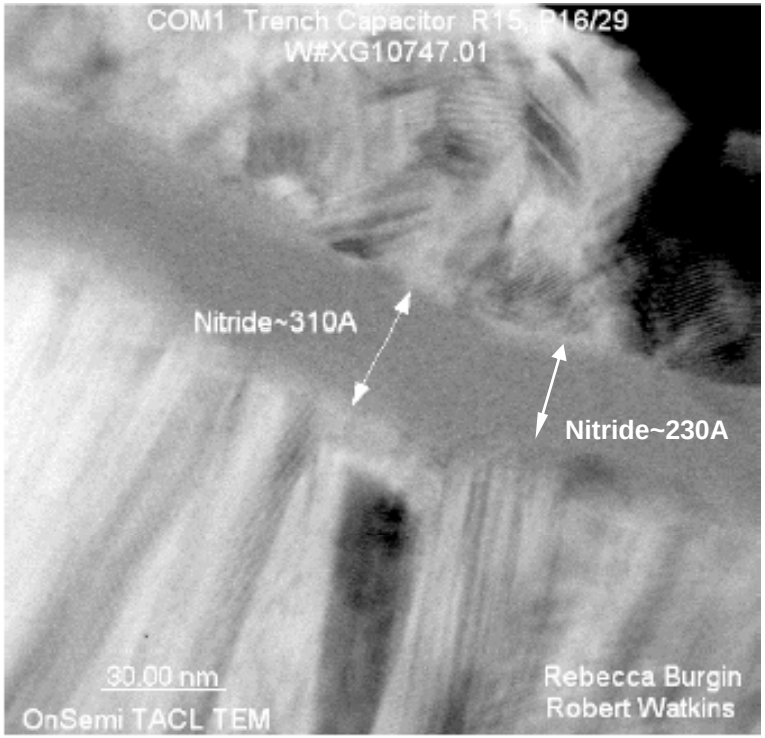


Reliability Evaluation

Capacitor dielectric thinning on top surface after poly etchback found as source for extrinsic failures



Nitride on trench sidewall

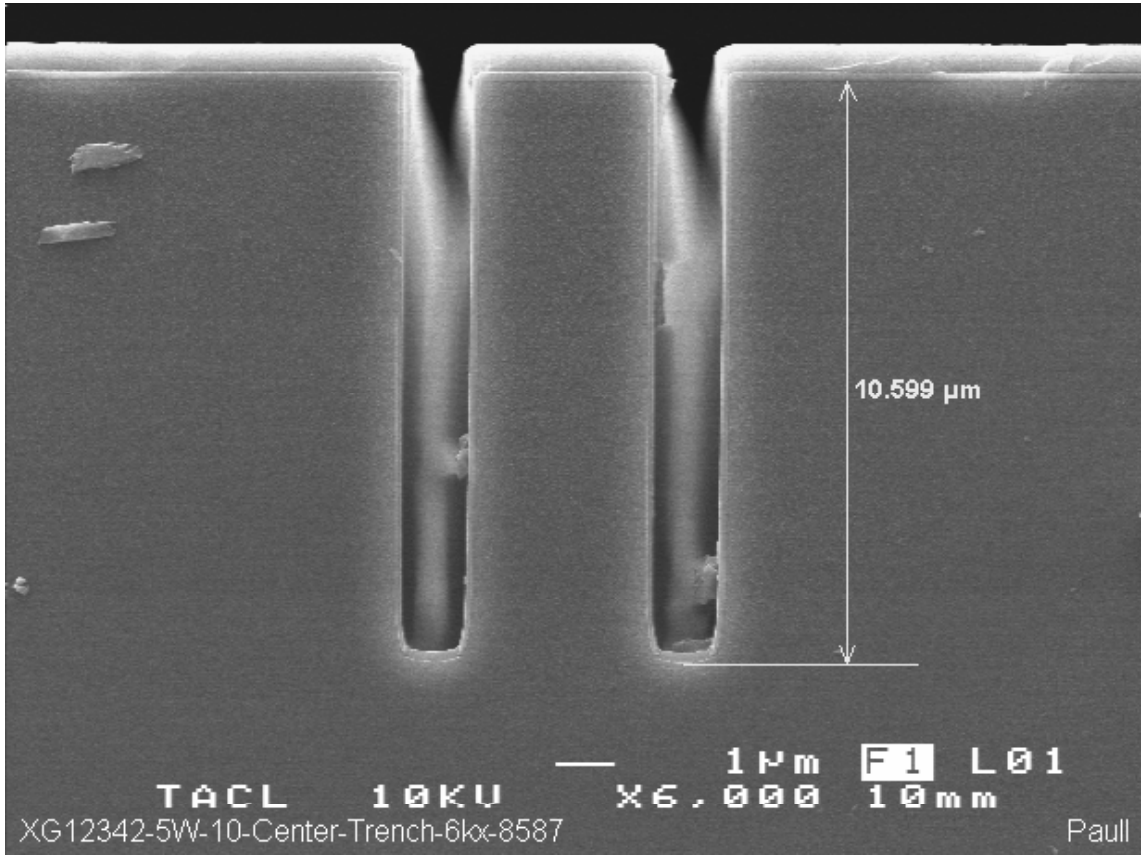


Top nitride after polysilicon etchback

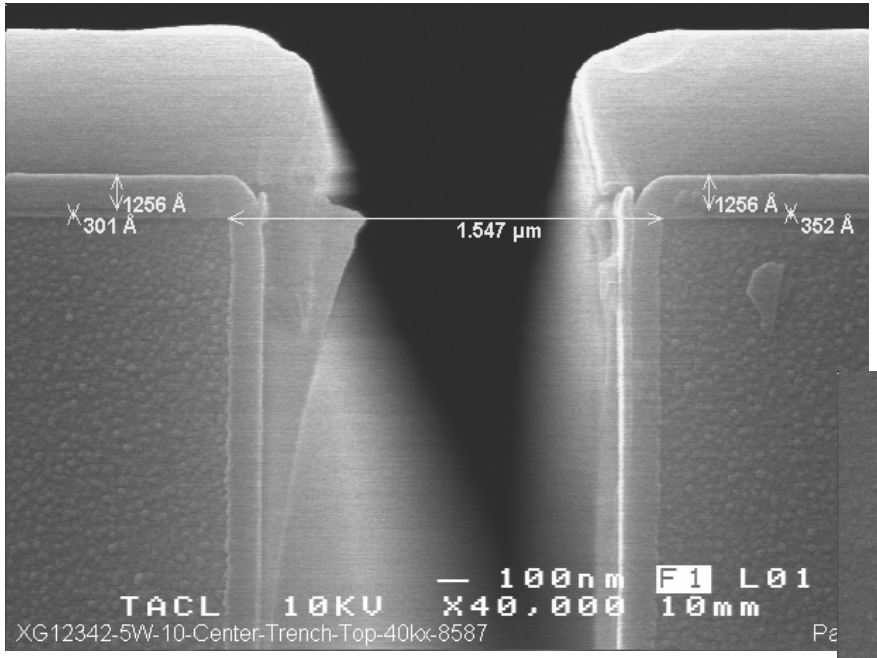
4. Potential enhancements and applications

Enhancements

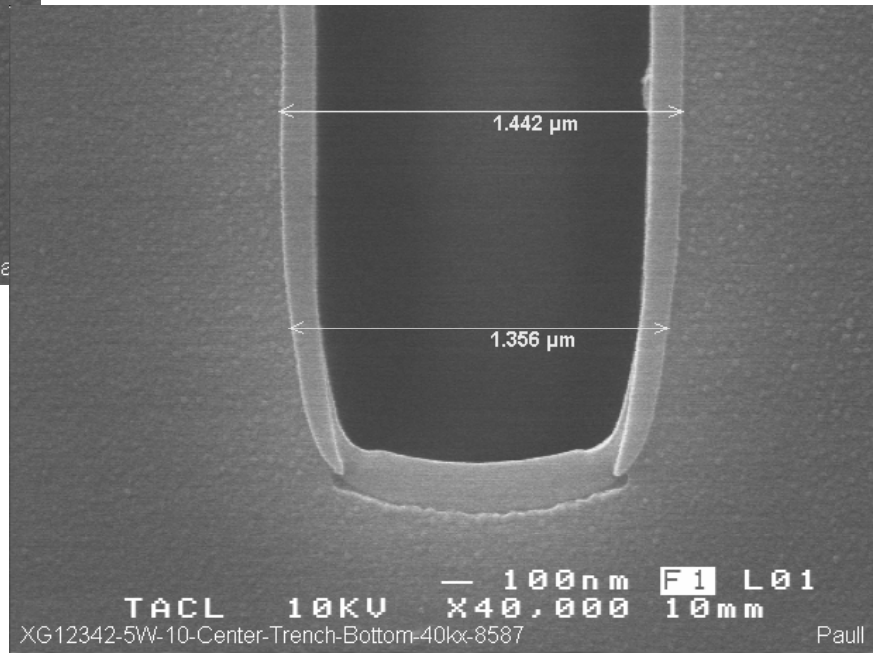
Multi-use trench process: isolation, oxide termination, substrate contact, bottom plate contact



Enhancements

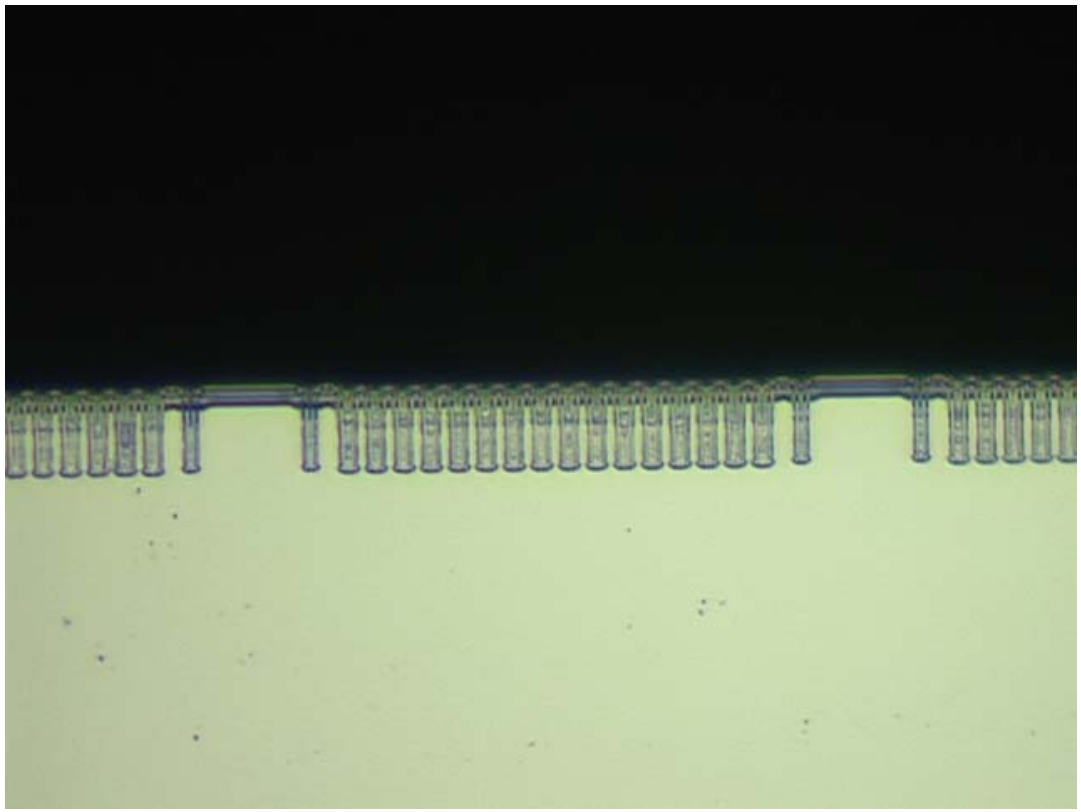


Oxide lined trench with substrate contact opening

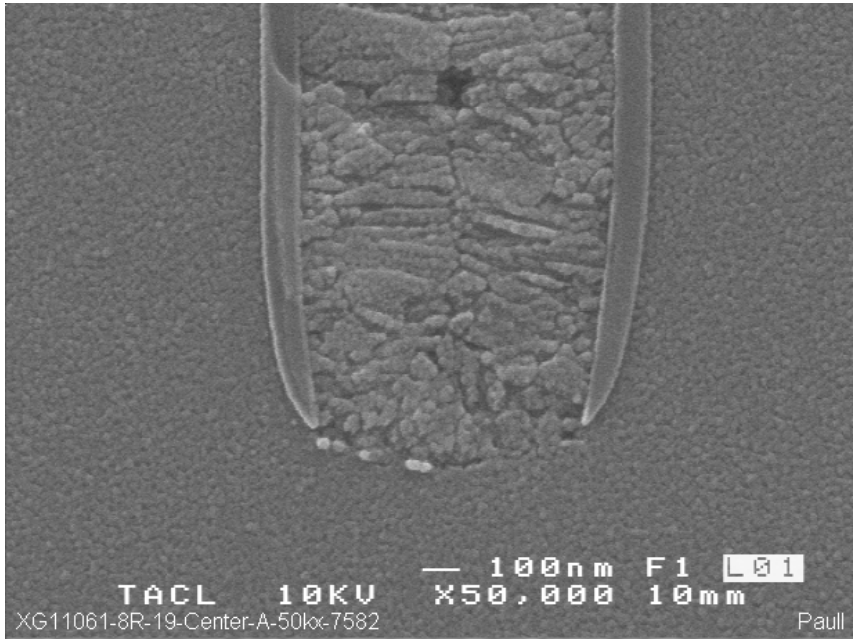


Enhancements

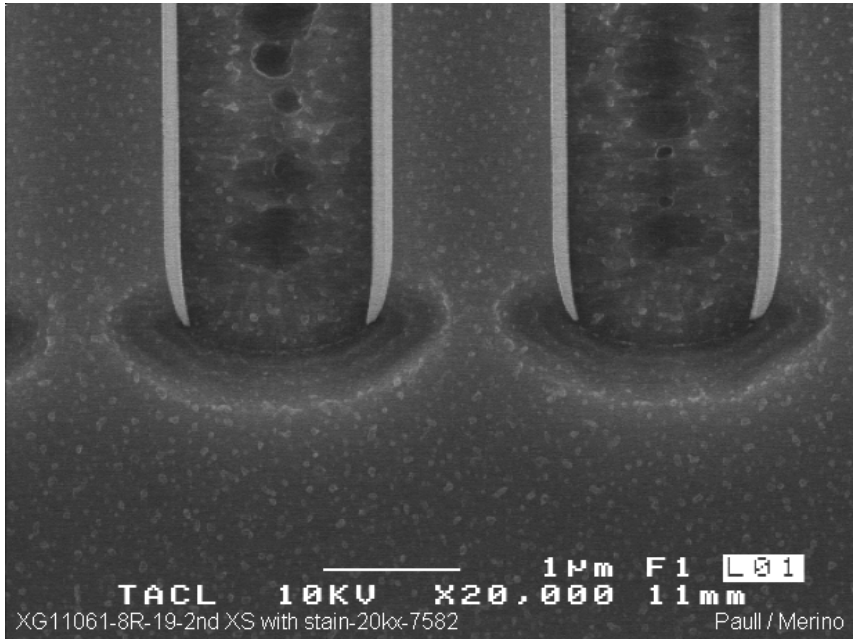
Optical X-section view of oxide lined trenches with substrate contact



Oxide isolated substrate contacts

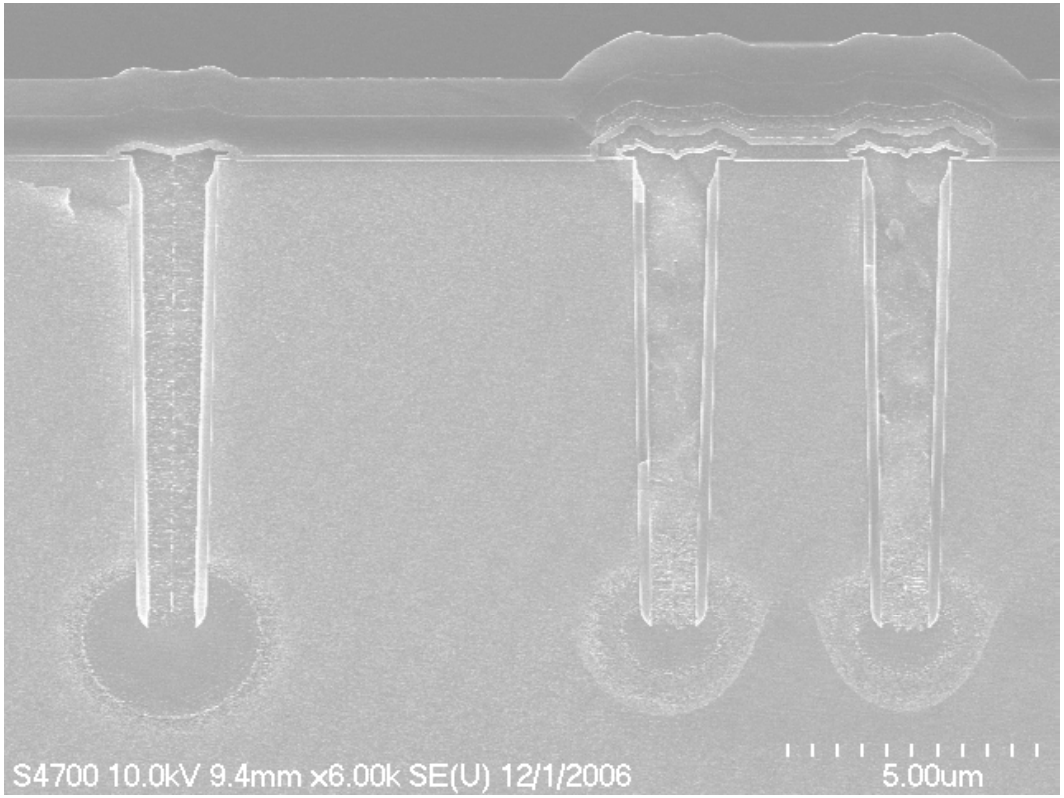


SEM Highlighting deep polysilicon contact



SEM highlighting dopant outdiffusion

Oxide isolated substrate contacts

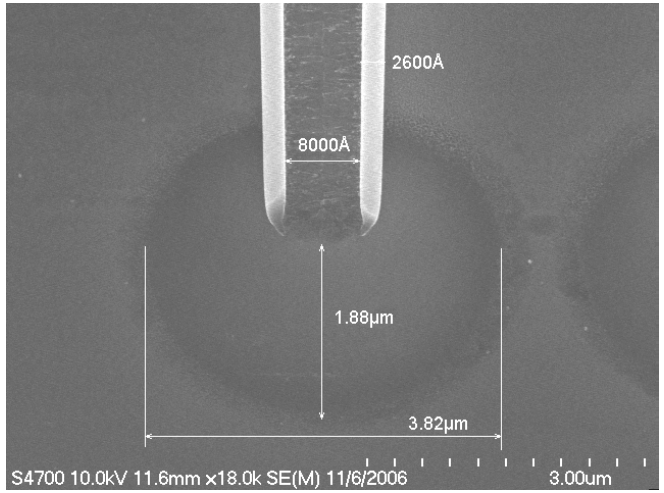


Boron doped poly fill

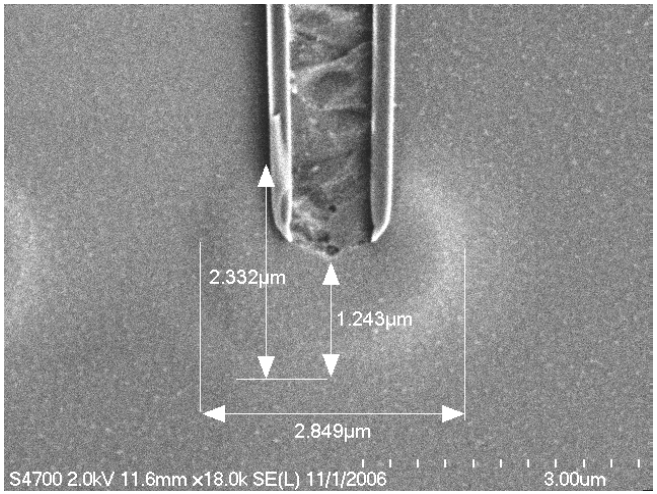
Phosphorous doped poly fill

Enhancements

Insitu doped trench (post 1100C 45min anneal)



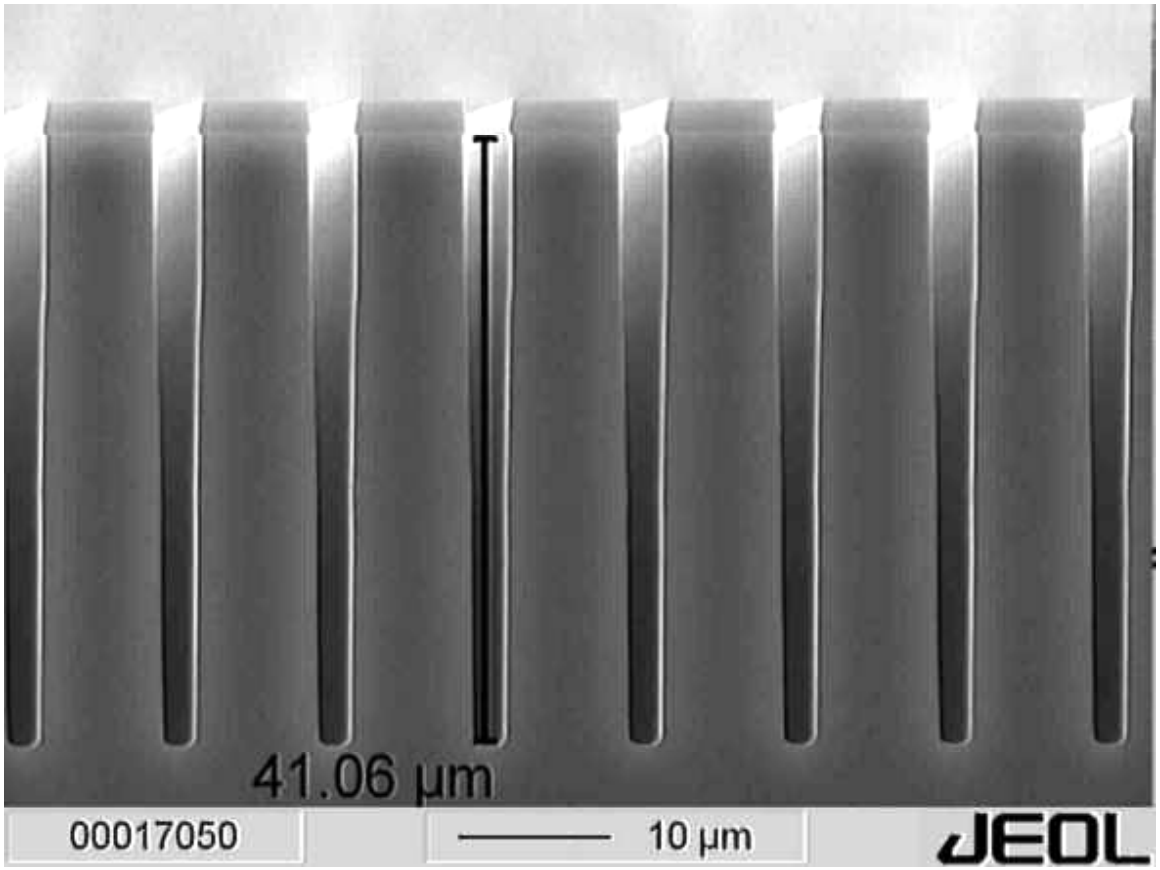
Boron doped



Phos doped

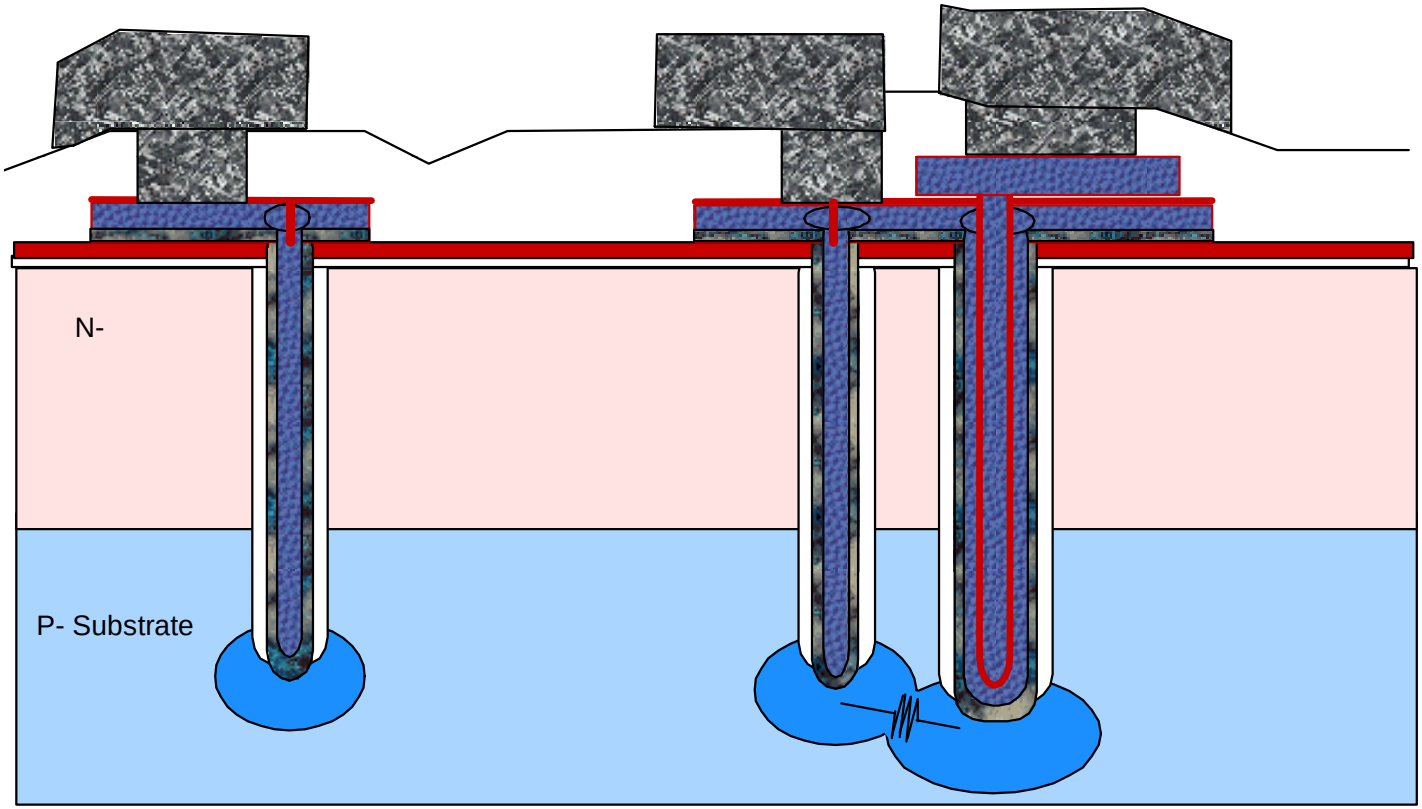
Enhancements

Extreme trench depth for very high capacitance on chip



Enhancements

Potential for silicided bottom plate for further resistance reduction.



5. Summary

- A high-performance trench capacitor has been integrated into RF BiCMOS and other technologies.

- A distributed trench-capacitor model has been developed and implemented in SPICE.

Summary

- Models have been successfully used in several high-frequency designs.
- Capacitor has been successfully added to multiple substrates and process integrations.
- Several potential enhancements have been demonstrated.

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