MOSFETs Make Step Change in Performance to Meet New Application Requirements

Low voltage MOSFET devices (<40 V) are used extensively in the power systems of portable electronic devices, domestic appliances, data communication servers, medical equipment and telecom infrastructure deployments. Exacting demands continue to be placed on the engineers involved in the design of such MOSFETs. The article will look at the forces at work and how significant, yet potentially conflicting, technical challenges need to be tackled. **Wharton McDaniel, Product Marketing Manager Power MOSFETs, ON Semiconductor, Phoenix, USA**

Our everyday lives are now almost totally reliant on the use of various forms of electronics equipment, however there are major concerns about the rise in worldwide energy consumption that this is leading to - its depletion of fossil fuels, the impact it has on the environment (in terms of carbon emissions, etc.) and the enlargement of utility bills too. Greater consumer awareness, the implementation of hard-hitting legislative measures (such as EnergyStar), plus OEMs' testing performance roadmaps, are all compounding the acute pressure being placed onto power semiconductor manufacturers. Next generation of power systems will consist of components that possess a number of highly favorable attributes.

Important drivers

There are two main dynamics that are currently responsible for defining MOSFET development. On one side you have the high end processing being required by sever farms. Here the power demand and density of the microprocessors found in racks has grown immensely - presenting electricity consumption, real estate and thermal management obstacles that need to be overcome. Conversely, in computing it is not the processing capacity that is now the main concern. As computer platforms have migrated from bulky desktop PCs to lightweight, streamlined portable products, such as tablets and smartphones, this is no longer the key selling point for customers. The criteria by which the power systems are outlined have changed here, with battery life and system compactness now being prioritized. The switching frequencies of both these types of power systems must be raised, so that smaller magnetics and passive components can be used, with less space thus needing to be allocated.

Having established what the drivers are at the application level, how does this translate into the components specs? There are three main parameters which should be scrutinized when specifying MOSFETs for a power system. These are:

1. On resistance (R_{DSON}) is vital when it comes to mitigating a MOSFET's conduction losses, so this should be as low as possible.
2. Figure-of-Merit (FOM) - defined by R_{DSON} x Q_G (total gate charge), this is an indicator of both the switching and conduction losses of the MOSFET, so it is used as an important selection criteria when deciding on which component to use.
3. Switching performance - The better switching characteristics of the MOSFET are, the lower the switching losses will be. With increased switching frequencies being witnessed all the time, this will become even more crucial in the coming years.

MOSFET design and its implications

MOSFET usage became more common in the 1980's, and in the decades that have passed since then a lot has changed in terms of the way these devices are fabricated and the performance specs they can deliver. Though it is for very different reasons, the MOSFETs serving both of the very disparate applications scenarios we discussed earlier need to dissipate as little power as possible (when active and also when inactive), so keeping R_{DSON} low must be one of the fundamental goals. Support very high conversion efficiencies is also a huge plus point, as is having a small die size - as in both portable products and server implementations board space is at a premium. The question is how to go about achieving this performance 'wish list' at the component level.

There are two elementary constituents that MOSFET design can be broken down into. In the past it was possible for component manufacturers to get away with just doing one of these really well, then dealing with the other solely as an afterthought. Now though they need to be addressed simultaneously, with equal emphasis.

Process technology - ten years ago a CPU generally required a current of around 10 A to drive it, today it is more likely to be 100 A. This has dictated an order magnitude reduction in R_{DSON} simply to keep form factors and heat dissipation levels in check, otherwise a substantial expansion in the size and cost of electronic equipment would have been unavoidable. Furthermore, a MOSFET's overall switching performance can be greatly augmented through a reduction in its capacitances. Continued development of new semiconductor processes have allowed the MOSFET R_{DSON} and capacitance reductions needed by OEMs to be realized. These reductions should remain scalable - keeping pace with smaller semiconductor geometries for the foreseeable future. The advent of shielded-gate trench topology is helping to keep the industry ahead of the game, with features which minimize switching overshoot, complementing the lowered R_{DSON}. With switching frequencies rising, as already stated, overshoot is becoming more of an issue, so this topology's ability to mitigate its effect is highly advantageous.

Package technology - a great deal of

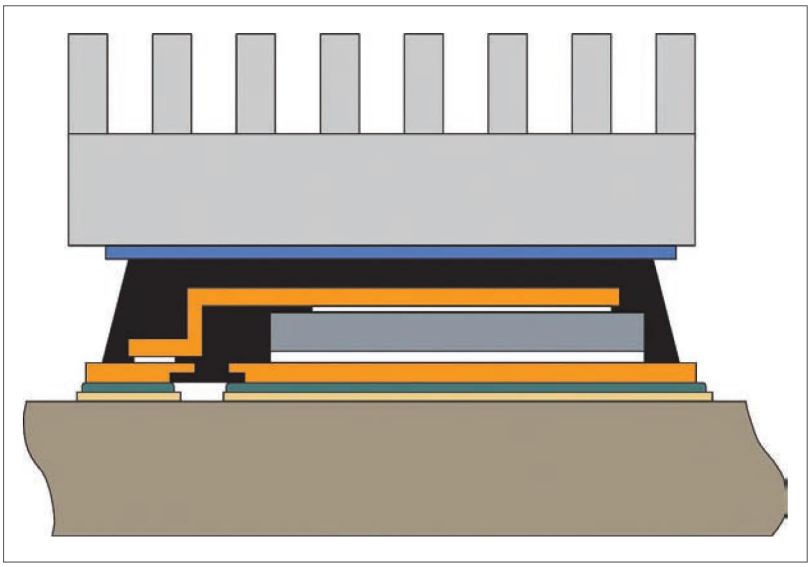

Figure 1: **Thermally enhanced SO8FL package with heatsink**

effort must be put into curbing the interconnect and thermal resistances of any power MOSFET package. The interconnect resistance has to be minimized with respect to the R_{DSON} values of the die (especially as we are now reaching sub milliohm levels) - otherwise any improvement in the Silicon will not be worthwhile. The use of clips in place of bondwires has been the main means of keeping interconnect resistance as a small percentage of the total RDSON. The exposed pad on the bottom of surface mount packages provides the primary low resistance thermal path. Now there are surface mount packages which have reduced thermal resistance to the top of the package, allowing heatsinking from the top of the package (see Figure 1). This type of package is important where the PCB cannot be an effective heatsink. It is clearly no good if semiconductor expertise has managed to provide strong performance qualities only to then be let down by poorly implemented packaging.

The continuing reduction in die size over the years brought on the migration from leaded power packages, such as TO220, to surface mount packages for single MOSFETs and now to dual packages. High power phase pairs of MOSFETs now are available in 5 mm x 6 mm packages. Performance is enhanced due to the reduction of the interconnect resistances and inductances. Also, this gives the designer a great advantage where space is at a premium as is shown in Figure 2.

The specification of MOSFETs which offer engineers an optimized balance of conduction loss characteristics and switching efficiency can prove vital to end product development. Utilization of the latest semiconductor processes and packaging technologies have helped to minimize the losses being experienced as well as reducing the energy dissipated from system designs so that the accompanying thermal management mechanisms take up less space. This means that the end products can be placed in to sleeker, less cumbersome form factors. Also greater system reliability and longer lifespan can be assured.

Conclusions

In conclusion, there needs to be continued investigation and then implementation, within the power electronics arena, of more effective ways by which to curb the losses that are related to the MOSFET switching activity and improve conversion efficiency levels, while simultaneously reducing R_{DSON}. Technological progression is enabling processes where both R_{DSON} and the capacitances associated with the switching circuit can both be lowered substantially. The upshot of this is that the PCB area that needs to be utilized and switching performance characteristics are both being improved as more compact passive components can be employed and higher switching frequencies can be utilized. Difficulties still lie ahead, however - eventually die sizes will start to get so small that the approaches to interconnect and thermal management will have to change dramatically again.

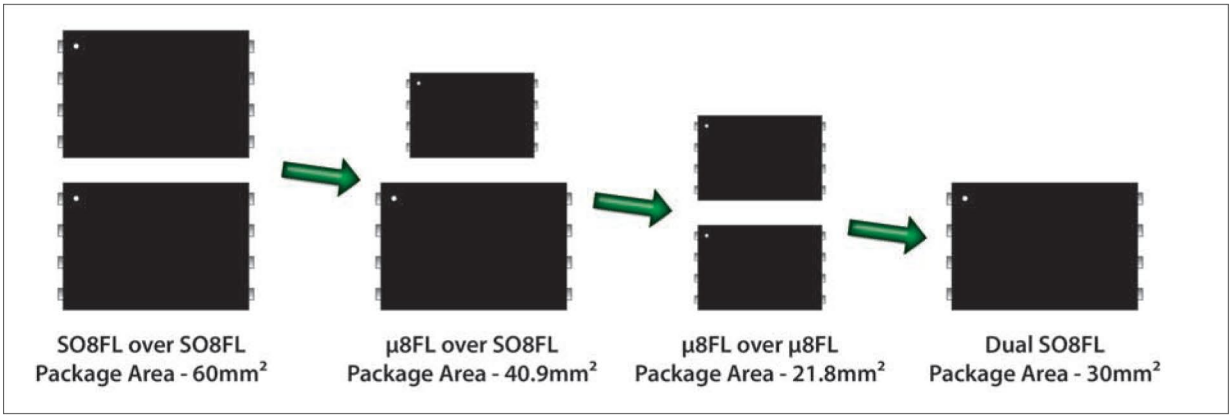

Figure 2: **Progression of package technology**