Efficient Architectures for Internal and External Computer Power Supplies

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Agenda

- Efficiency Drivers
- ATX power requirements overview
  - PFC solution
  - SMPS solution
  - Post regulation
- Notebook adapter power requirements overview
  - PFC solution
  - SMPS solution
  - Single stage option
- Conclusions

Power Efficiency Drivers

- Market forces (small size, weight expectations)
- Competitive pressures
- System level savings (easing of thermal load, improved reliability)
- End customer specifications (e.g. Intel)
- Regulatory requirements (emerging)

Regulatory Challenges

- Standby Power Reduction
  - 25% of total energy consumption is in low power/sleep/standby mode
  - Concerted effort by CECP, Energy Star, IEA and other international agencies to limit standby power
- Active Mode Efficiency Improvement
  - 75% of total energy consumption is in active mode
  - Changing efficiency from 60% to 75% can result in 15% energy savings
  - Next focus area for agencies
- Power Factor Correction (or Harmonic Reduction)
  - Applicable with IEC 1000-3-2 (Europe, Japan)
  - Some efficiency specifications also require >0.9 PF

Standby Certification Programs
(External Power Supplies)

Code	Region/Country & Timing	No Load Power Consumption
CUC1	CECP (China) & Energy Star (US) From January, 2005 (Tier 1)	= 0.50 W for 0-10 W = 0.75 W for 10-250 W
CUC2	CECP and Energy Star From July 1, 2006 (Tier 2)	= 0.30 W for 0-10 W = 0.50 W for 10-250 W
CE1	Europe (EC Code of Conduct) From January 1, 2005	= 0.30 W for <15 W = 0.50 W for 15-50 W = 0.75 W for 50-60 W = 1.00 W for 60-150 W
CE2	Europe (EC Code of Conduct) From January 1, 2007	= 0.30 W for non-PFC = 0.50 W for PFC
CA1	Australia (High Efficiency) From April, 2006	= 0.50 W For 0-180 W

Active Efficiency Certification Programs

(External Power Supplies)

Code	Region/Country & Timing	Active Mode Efficiency
CUC1 **CE2**	CECP (China) & Energy Star (US) From January, 2005 (Tier 1) Europe (EC Code of Conduct) From January 1, 2007	=0.49*Pno for 0-1 W =[0.09*Ln(Pno)]+0.49 for 1-49 W =0.84 for >49 W
CE1	Europe (EC Code of Conduct) From January 1, 2005	=0.70 for 6-10 W =0.75 for 10-25 W =0.80 for 25-150 W
CUC2	CECP and Energy Star (Tier 2) From July, 2006	TBD (More stringent than Tier 1)
CA1	Australia (High Efficiency) From April, 2006	=0.48*Pno for 0-1 W =[0.089*Ln(Pno)]+0.48 for 1-60 W =0.84 for >60 W

- Note: Pno is defined as the nameplate output power.

ON Semiconductor

80-plus program

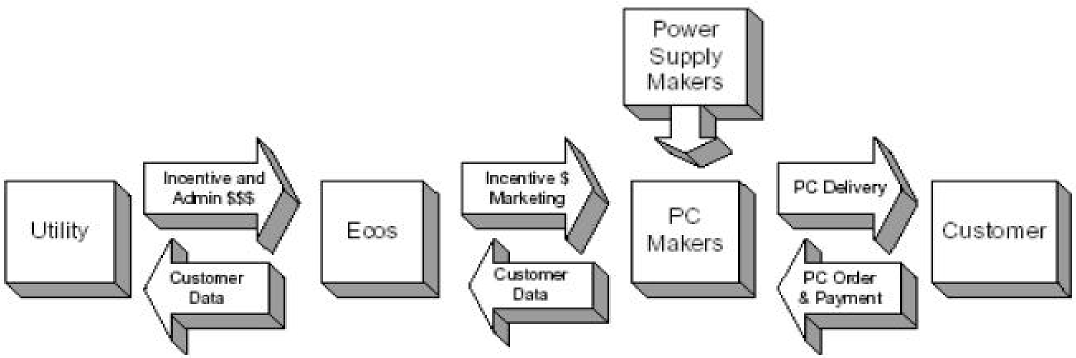
ecos CONSULTING

80+ Power Supply Program for Computers

An immediate opportunity to secure energy and peak savings for less than 3 cents per lifetime kWh

New Design Assures Major Reduction in Computer Energy Use

Specification	Efficiency Measurements			Maximum heat output in a 250 watt power supply	Typical power supply energy consumption[4]
	20% Load	50% Load	100% Load		
2003 measured average	65%	71%	69%	112 watts	127 kWh/yr
2004 Intel required spec	60%	70%	70%	107 watts	149 kWh/yr
2004 Intel recommended spec	67%	80%	75%	83 watts	113 kWh/yr
80+ power supply	82%	87%	85%	44 watts	61 kWh/yr

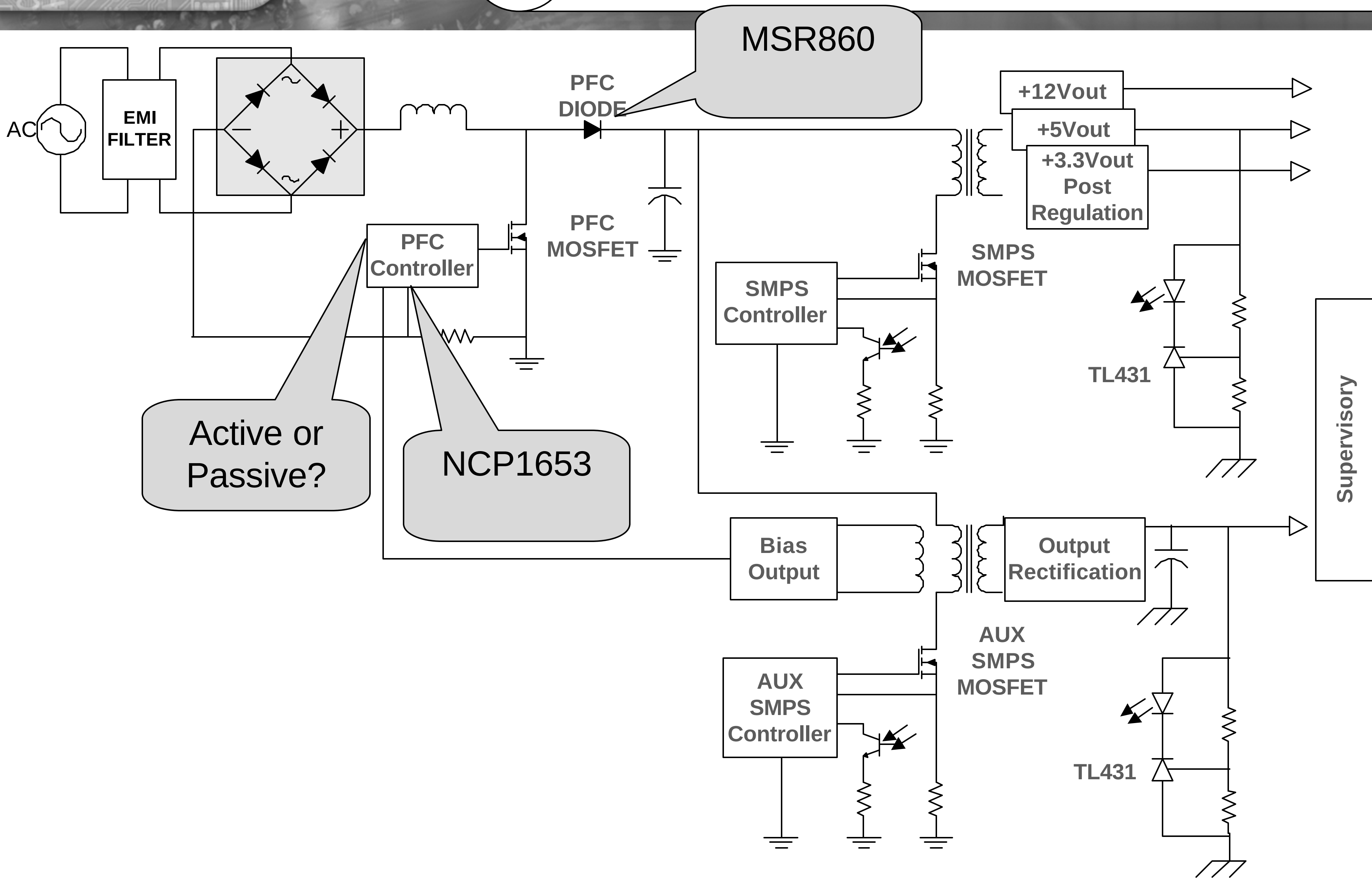


www.80plus.org

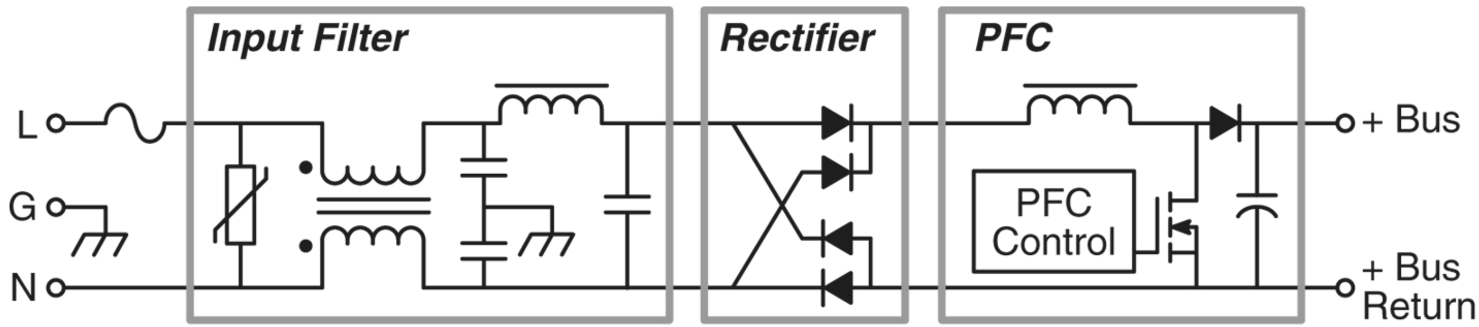
ATX Power Requirements

- Power Level in the 250-350 W range
- +12/+5/+3.3/-12 V outputs
- Need for standby power (10-15 W)
- Better post regulators for 3.3 V needed
- Improvement in efficiency sought
- More compact solution required

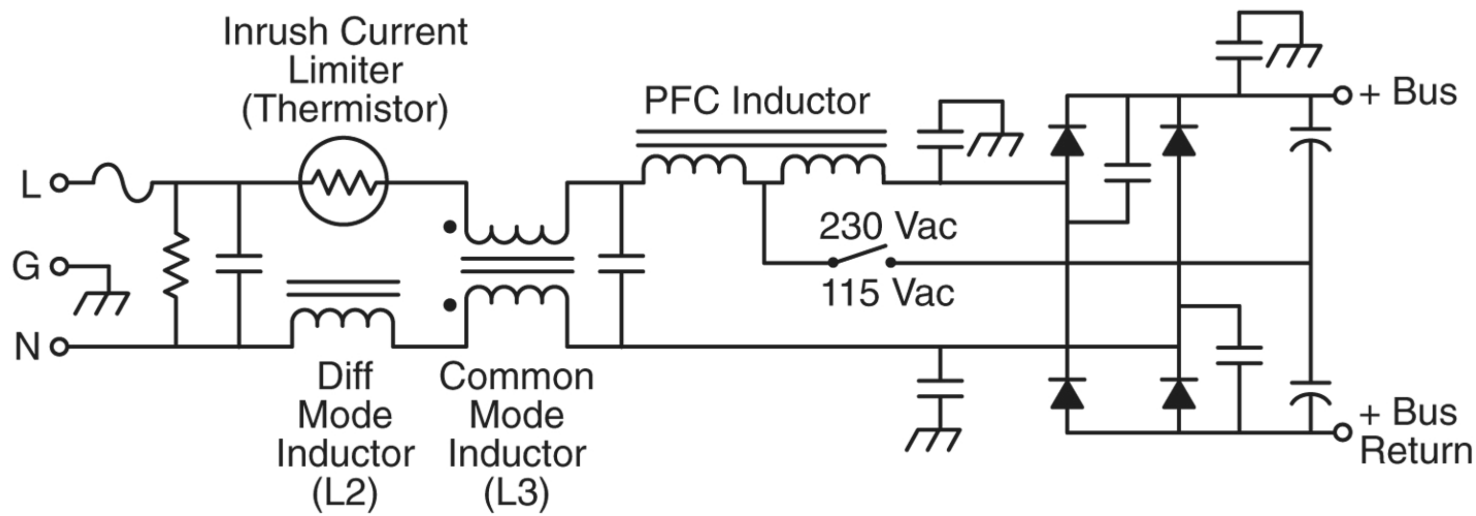
ATX Block Diagram



Active vs. Passive PFC



Active PFC

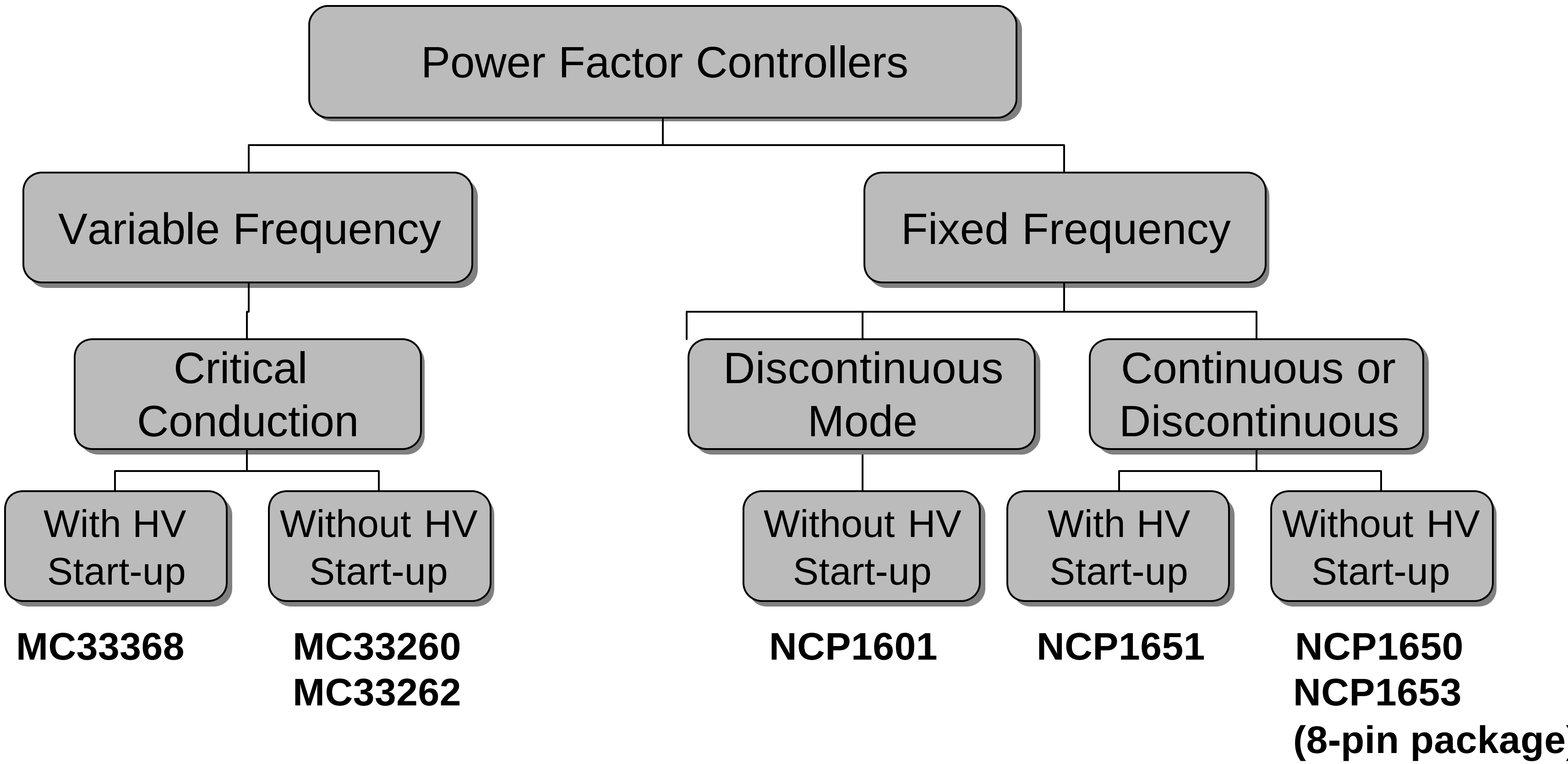


Passive PFC

Solution Comparison

Attribute	Active PFC	Passive PFC	Comments
Electrical Complexity	Medium (full power stage needed)	Low (choke, range switch, extra bulk cap)	Reduced complexity for active PFC with newer components
Input rms current	3.0 A	3.69 A	Higher current leads to larger filter size
Output voltage range	300-415 V	200-375 V	Impact on SMPS stage operation
Bulk capacitance	220 uF, 420 V	2x1000 uF, 200 V	Passive value often traded off against Vo range
Protection features	Incorporated	Not available	Added circuit costs
Reliability	Foolproof (no range switch)	Potential failure due to range switch	
Efficiency at 115 V	~94 %	~96 %	Active efficiency can improve with better semiconductors

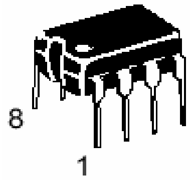
Full Coverage of PFC Solutions



NCP1653 CCM PFC Controller

The NCP1653 is ideal in systems where **cost-effectiveness, reliability and high power factor** are the key parameters. It incorporates all the necessary features to build **compact and rugged PFC stages.**

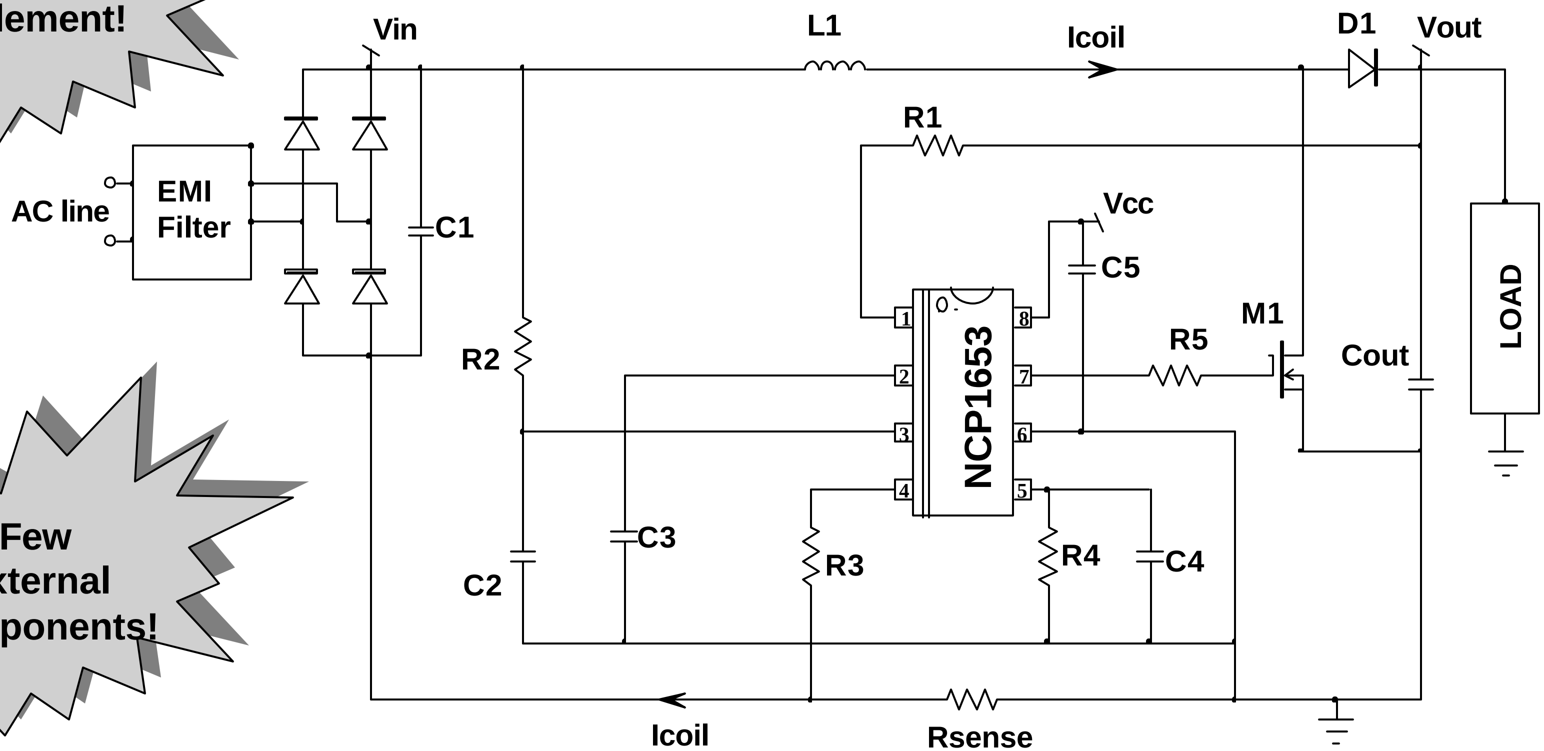
- Near-Unity Power Factor
- Fixed Frequency (100 kHz), Continuous Conduction Mode
- High Protection Level for a safe and robust PFC stage
  - Soft-Start
  - Over-Current Limitation, Over-Voltage Protection
  - In-rush Currents Detection
  - Feed-back Loop Failure Detection…
- “Universal” 8 pins package (DIP8 and SO8)
- Low Start-up Consumption, Shutdown Mode
- Few external components, ease of implementation
- Follower Boost Capability => flexibility, up-graded efficiency and cost-effectiveness



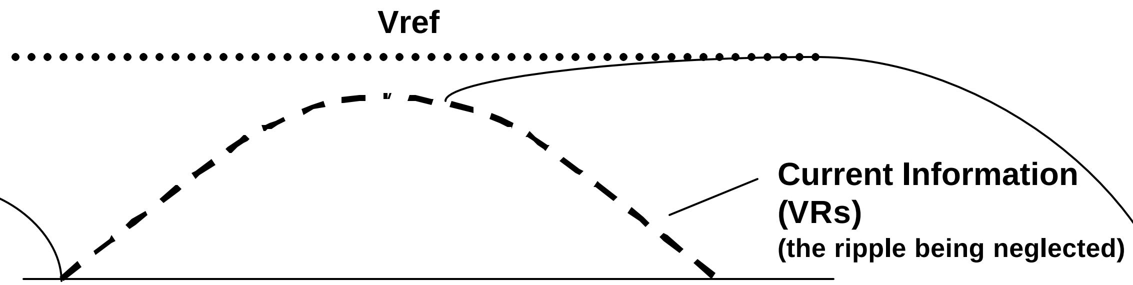
Generic Application Schematic

Simple to Implement!

Few External Components!



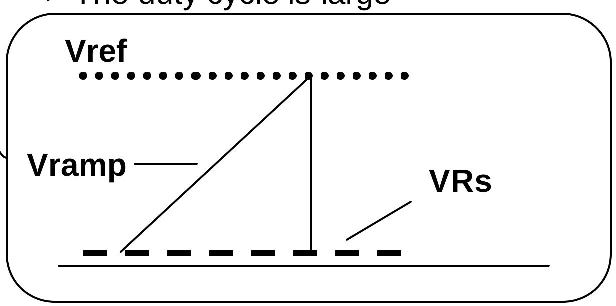
Duty-Cycle Modulation

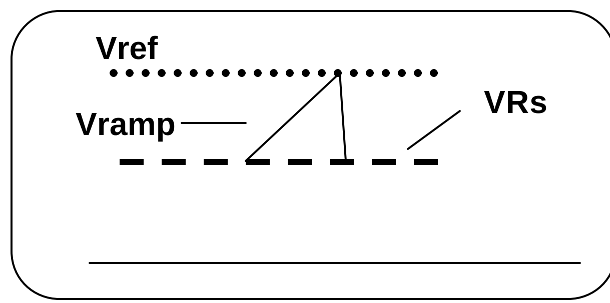


When the coil current is small:
The sum (Vramp + VRs) needs a long time to exceed Vref

=> The duty-cycle is large

When the coil current is high (top of the sinusoid):
The sum (Vramp + VRs) needs a shorter time to exceed Vref => The duty-cycle is smaller





Four Steps to Design the PFC Stage

Four steps:

1. Dimension the coil inductance, the MOSFET, the diode, the bulk capacitor and the input bridge, as you would do for any PFC stage
2. Select the feedback arrangement
3. Select the input voltage circuitry
4. Dimension the current sense network

Step 1 is “as usual”, Steps 2, 3 and 4 are straightforward

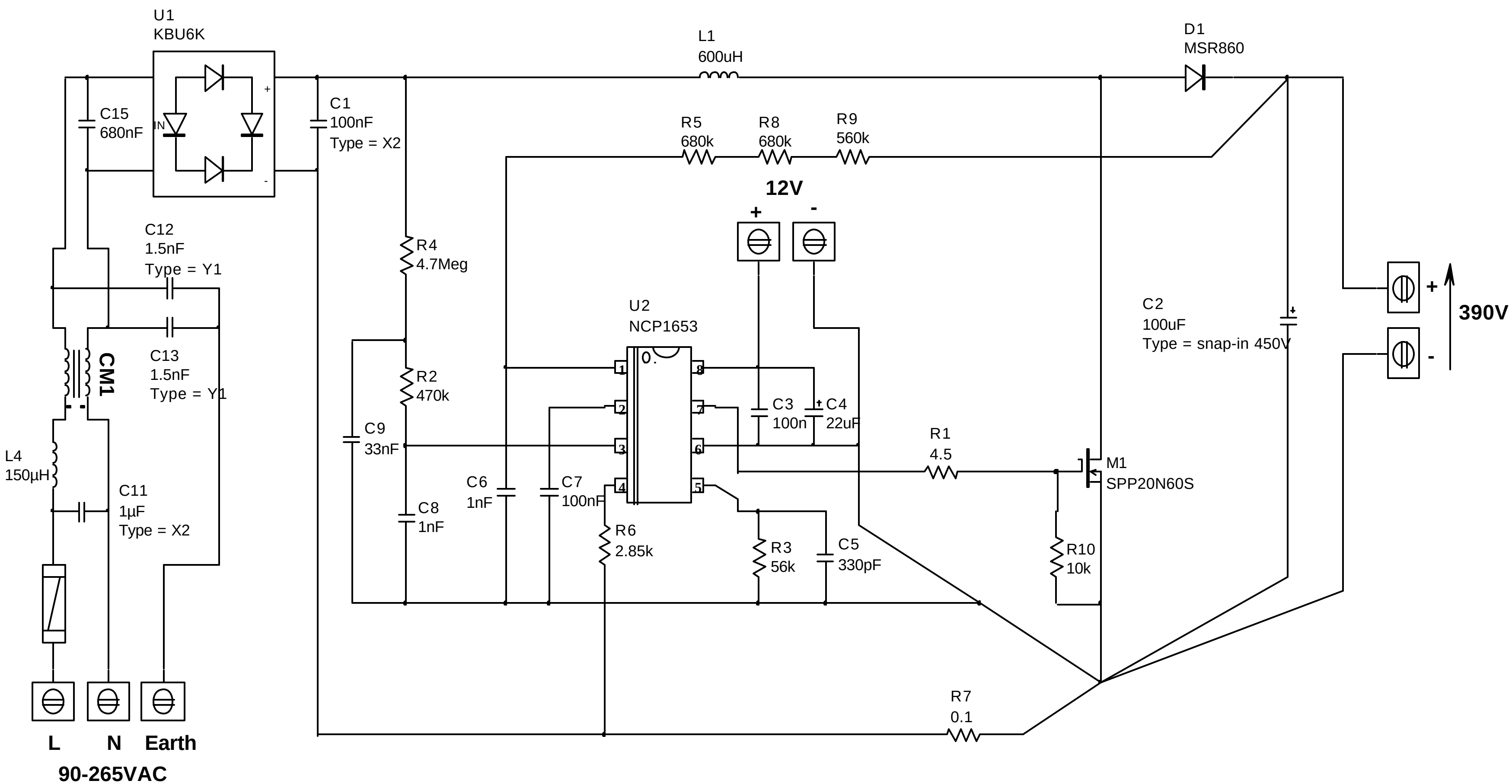
(see table of next slide)

=> Ease of implementation

Dimensioning Table

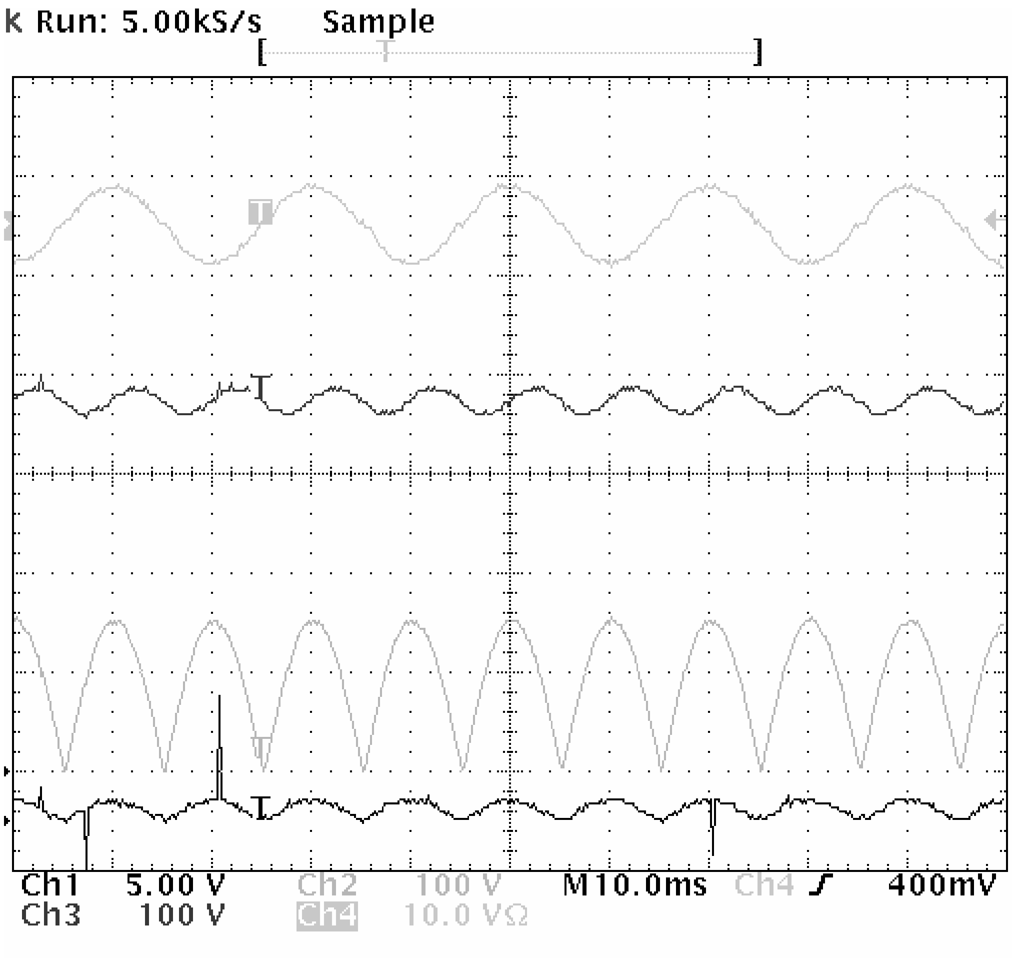
2 - Feedback arrangement	Rfb1 + Rfb2 + Rfb3	$Rfb1+Rfb2+Rfb3=\frac{Vout-4V}{200\ \mu A}$	Rfb1 = 680 kΩ Rfb2 = 680 kΩ Rfb3 = 560 kΩ
	Cfb1	Cfb1=1nF	Cfb1 = 1 nF
	C2	C2 = 100 nF	C2 = 100 nF
3 – Input voltage sensing	Rin1 and Rin2	$Rin=\frac{(2*\sqrt{2}*VacLL/\pi)-4V}{15\ \mu A}$ (Rin=Rin1+Rin2) Choose: $Rin1\approx 10*Rin2$	Rin1 = 4.7 MΩ Rin2 = 470 kΩ
	Cin1	1 nF	Cin1 = 1 nF
	Cin2	$Cin2=20\ ms/Rin2$	Cin2 = 33 nF / 63 V
4 – Current sense network	Rsense	Choose Rsense so that its dissipation keeps reasonable (as a rule of the thumb, select Rsense so that: pRsense is less 0.5%*(Pout)max)) $(pRsense)max=Rsense*\left(\frac{(Pout)max}{\eta*VacLL}\right)^2$	Rsense = 0.1 Ω / 3 W
	Rcs1	$Rcs1=\frac{Rsense*(Icoil)max}{200\ \mu A}$	Rcs1 = 2.85 kΩ
	Rcs2	$Rcs2=k*\frac{\eta*Rcs1*(Rin1+Rin2)*VacLL}{Rsense*(Pout)max*VoutLL}$ where: $K=250\pi/\sqrt{2}\ \ (\mu W)$	Rcs2 = 56 kΩ
	Ccs2	$Ccs2\approx 20\ \mu s/Rcs2$	Ccs2 = 330 pF

Application Schematic



Pout = 300 W, universal mains (90 Vac <-> 265 Vac)

Waveforms @ full load and 110 Vac



Ac line current (10 A / div)

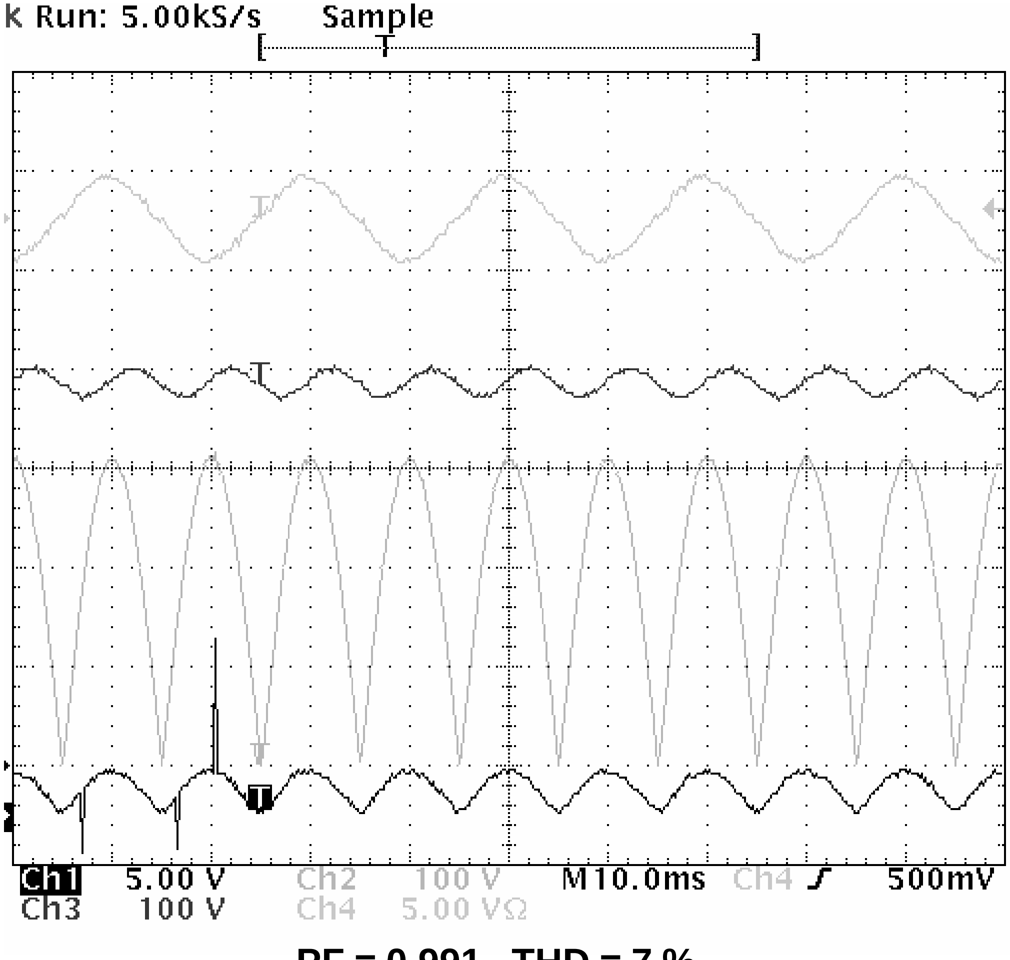
Bulk Voltage (100 V / div)
(375 V mean)

Rectified ac line voltage
(100 V / div)

NCP1653 pin5 Voltage
(5 V / div)

PF = 0.998 , THD = 4 %

Waveforms @ full load and 220 Vac



Ac line current (5 A / div)

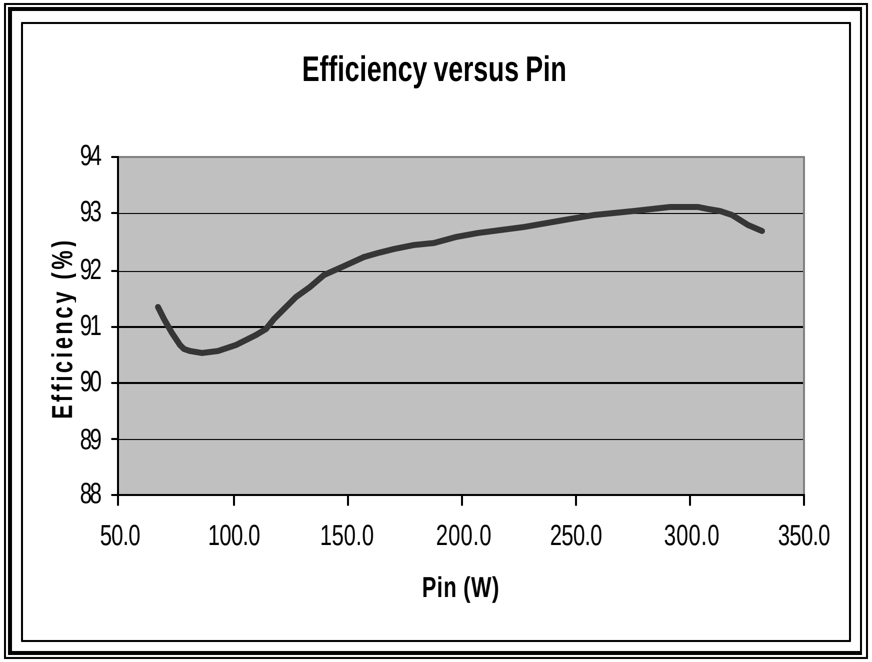
Bulk Voltage (100 V / div)
(386 V mean)

Rectified ac line voltage
(100 V / div)

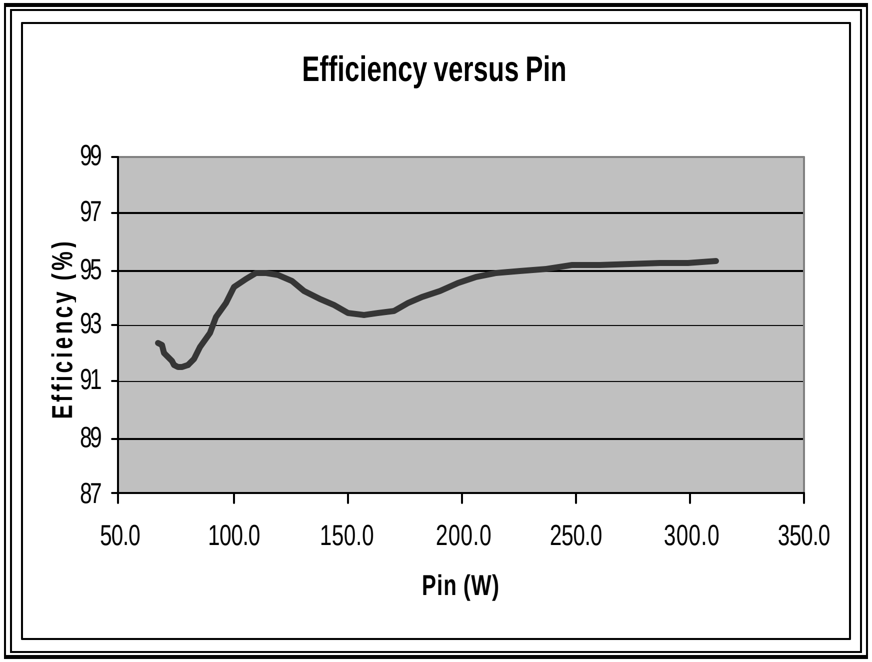
NCP1653 pin5 Voltage
(5 V / div)

PF = 0.991 , THD = 7 %

Efficiency vs P_{in}



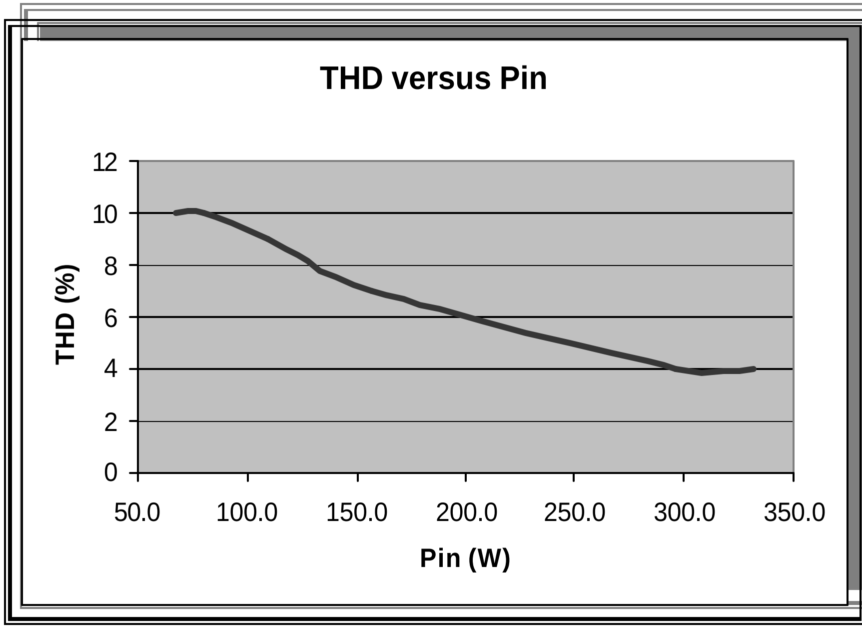
110 Vac



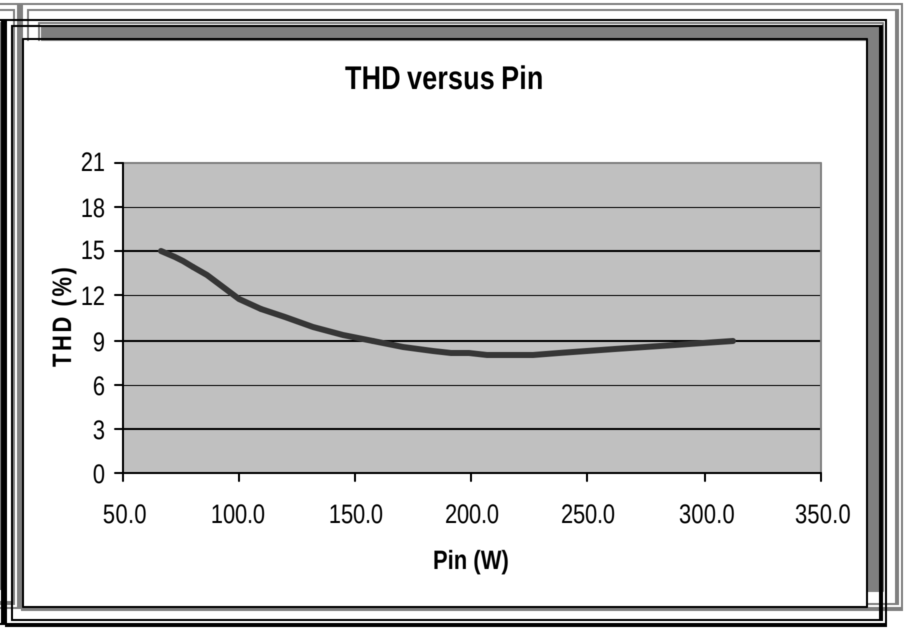
220 Vac

At full load, the efficiency is around 93 % @ 110 Vac and 95 % @ 220 Vac. The efficiency keeps high from Pmax to Pmax/5 (over 90 % @110 Vac and 91 % @ 220 Vac)

THD versus P_{in}



110 Vac

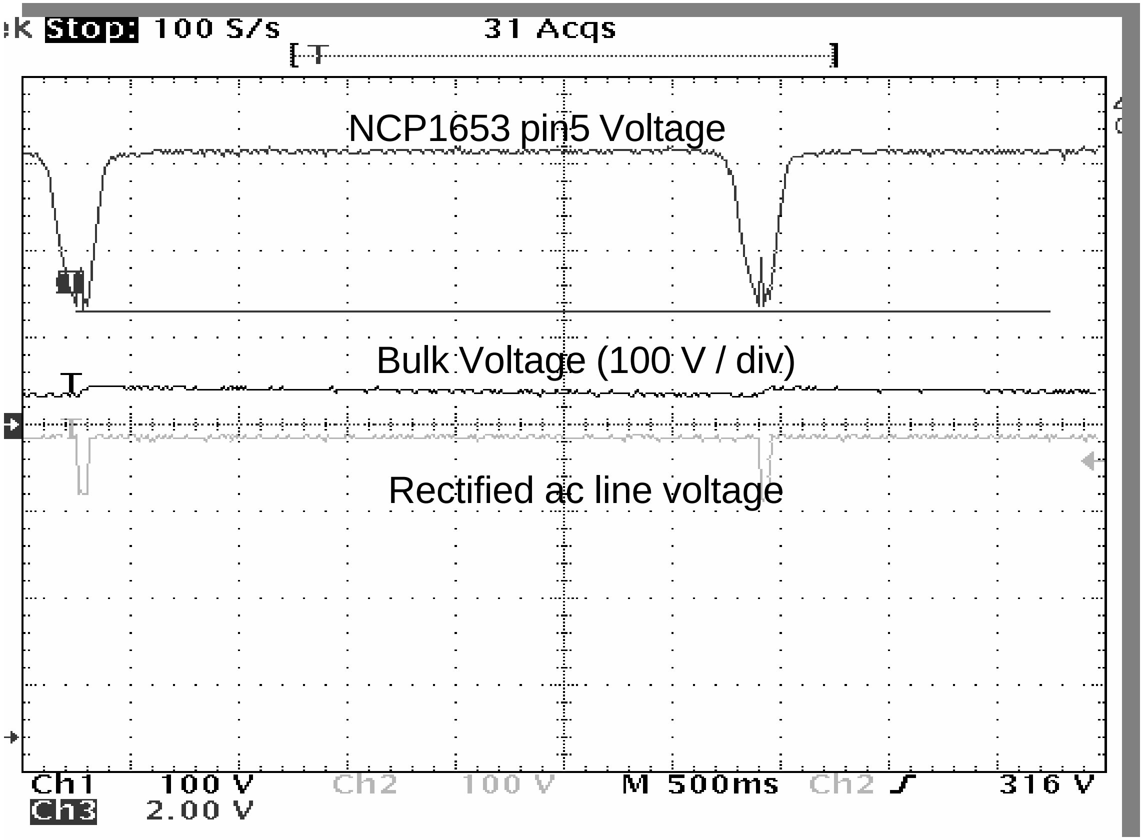


220 Vac

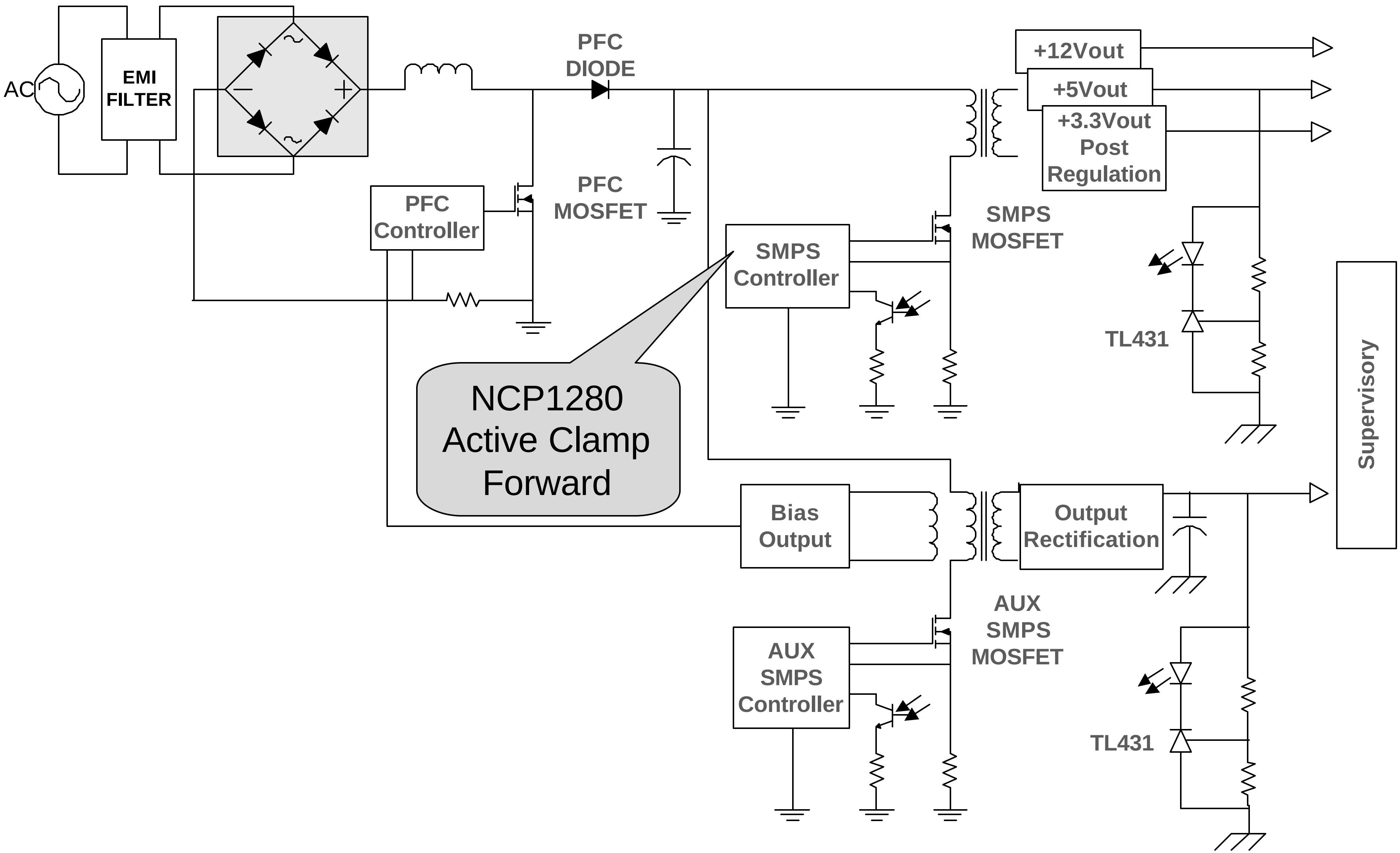
☺ **The THD keeps low over a large power range.**

No Load Operation

- The NCP1653 keeps regulating in the 300 W application by entering a low frequency burst mode
- The power losses @ 250 Vac, are: 200 mW (Burst mode frequency: around 0.3 Hz)



ATX Block Diagram

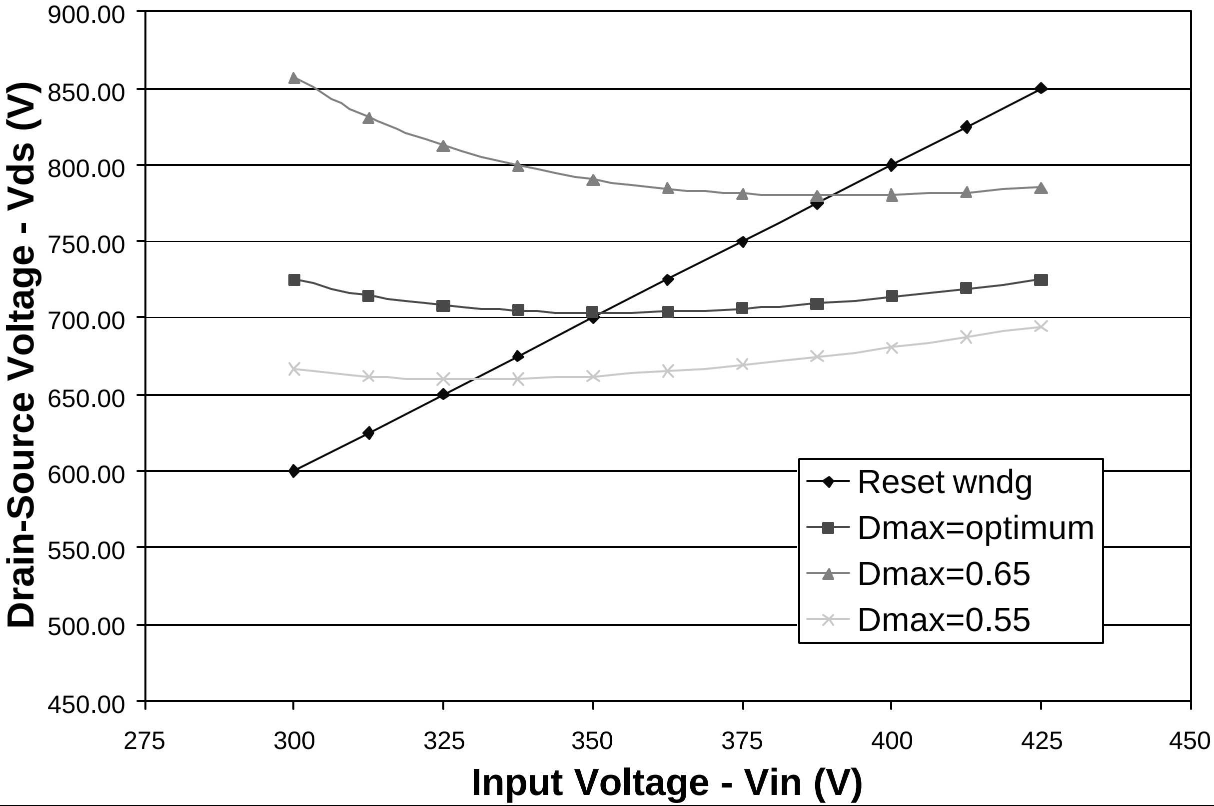


Converter Specifications

- Vin = 300-425 V (with PFC front-end but allowing for single cycle dropout)
- Vo1=12 V (+/- 10%), 15 A; Vo2 = 5 V (+/- 10%), 15 A; Vo3 = 3.3 V (+/- 10%), 13.6 A
- Pomax = 310 W
- Fsw = 250 kHz

Advantage of the Active Clamp

Vds against of Vin (Active Clamp vs Forward)



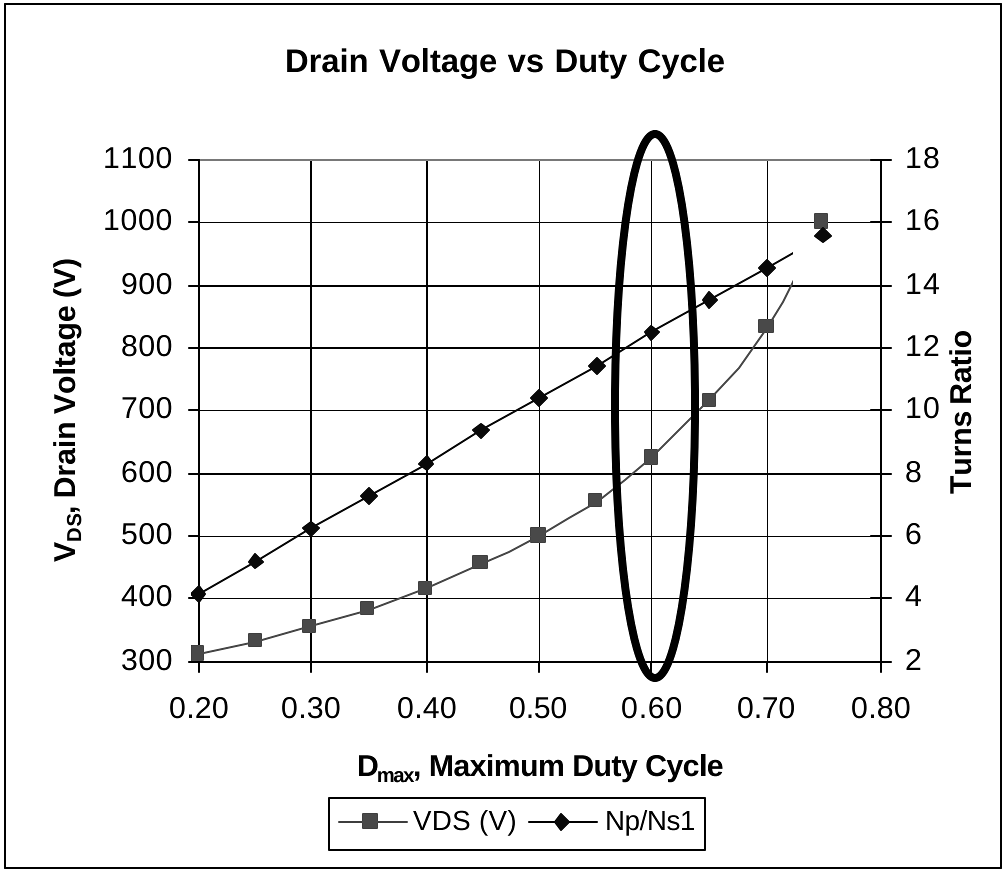
- Non-monotonic nature of the Vds plot offers a MAJOR benefit for wide Vin applications
  - Vds varies <50 V over Vin range vs. 250 V for 1-sw forward

Design Steps

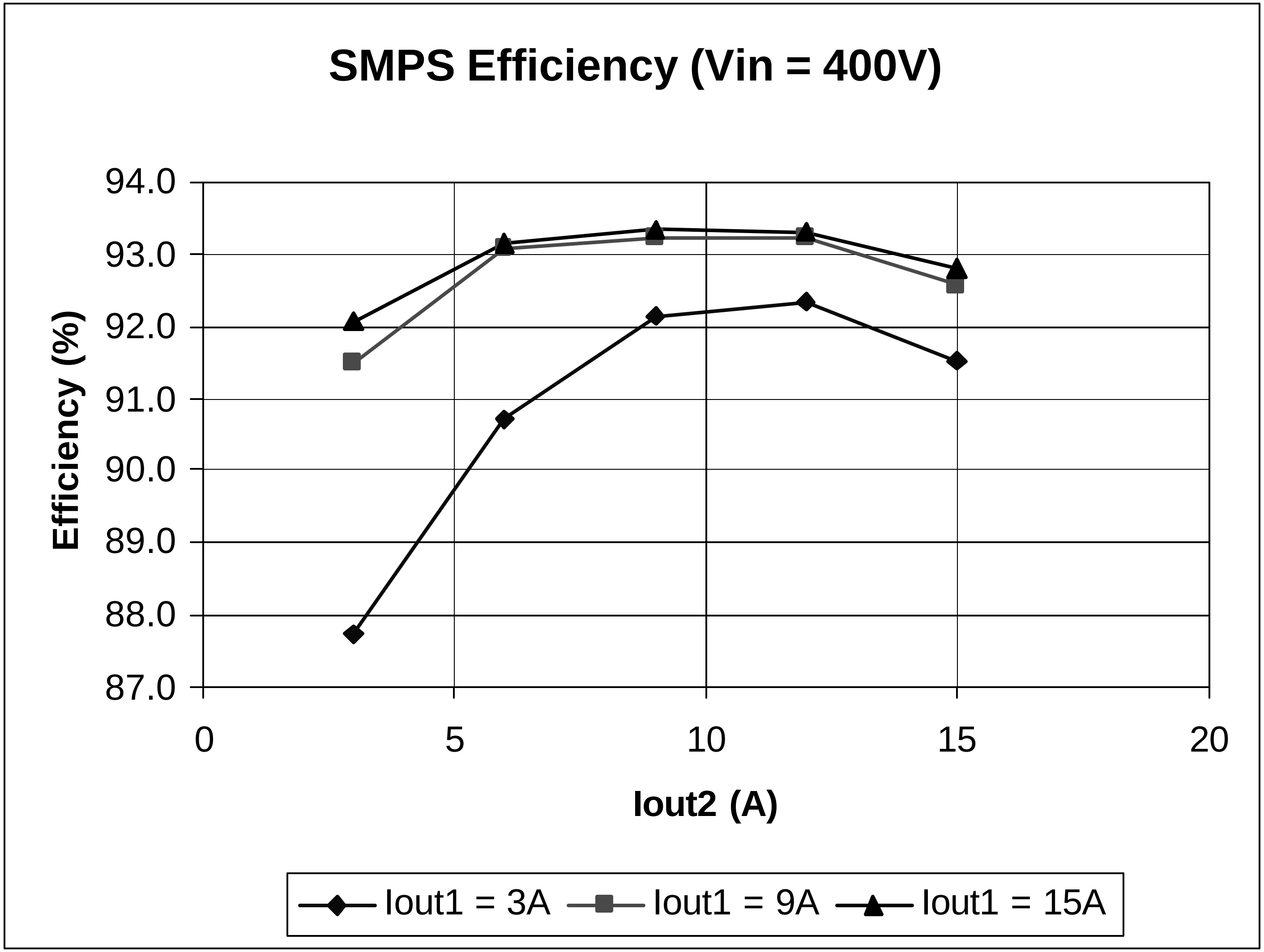
1. Select turns ratio and max D
2. Select switching frequency
3. Transformer design (core and windings)
   - Gapping the core is helpful in this design
4. Select power semiconductors
   - Choice of diodes or FETs on secondary
5. Clamp circuit design
   - Trade off between reverse saturation and higher Vds ripple
6. Output filter design (similar to forward)

Turns Ratio Selection

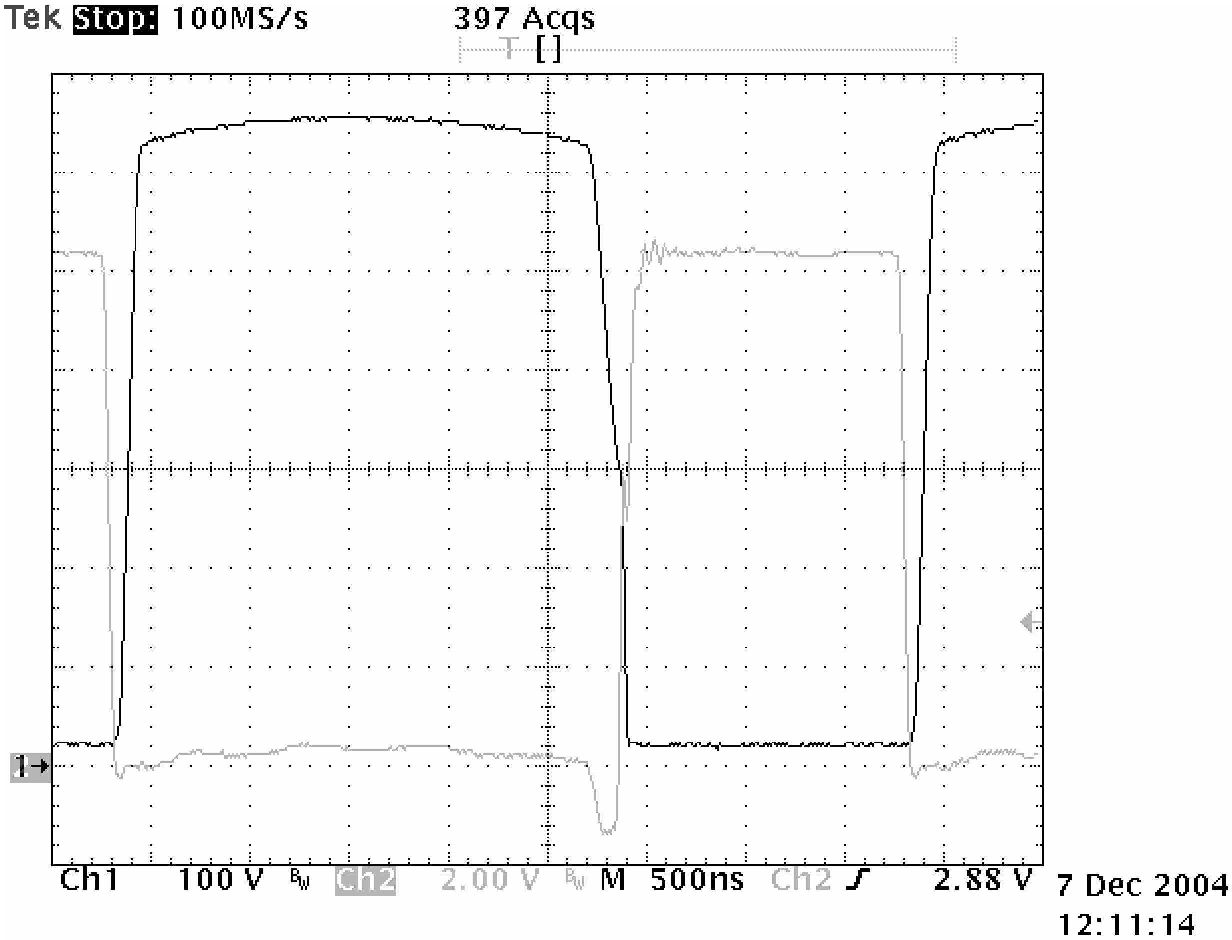
- Higher turns ratio(N) requires higher D_{max}
- Trade-off with high Vds stress
- Higher N reduces primary current and secondary voltage
- In this example, select 0.60 D_{max}
- Choose 0.55 for more Vds margin



Results at nominal line



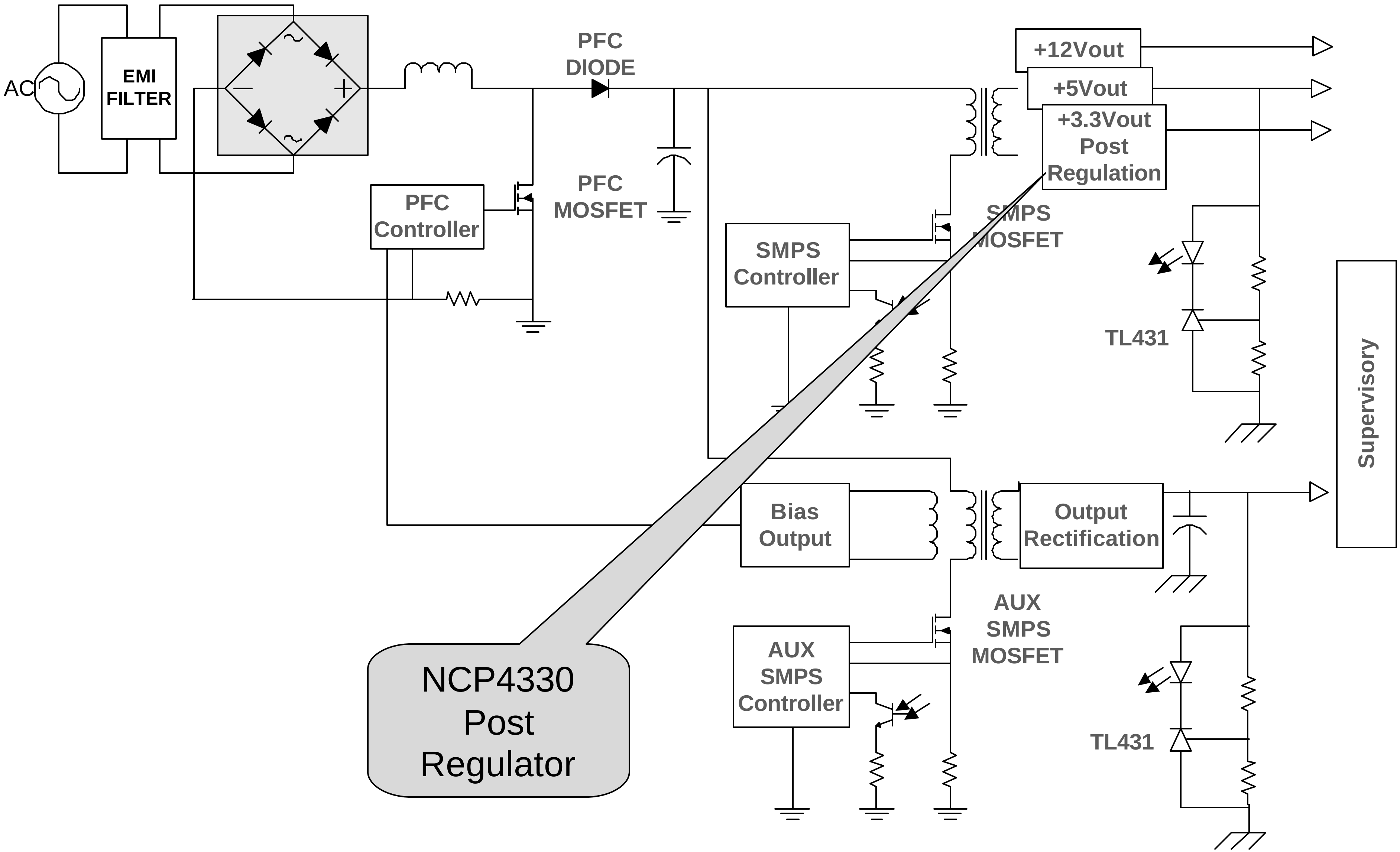
Switching waveforms



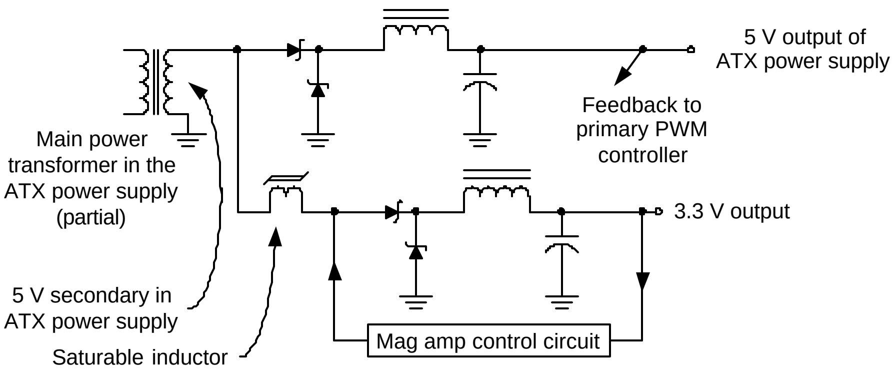
Active Clamp vs. 1-sw Forward (1:1 reset)

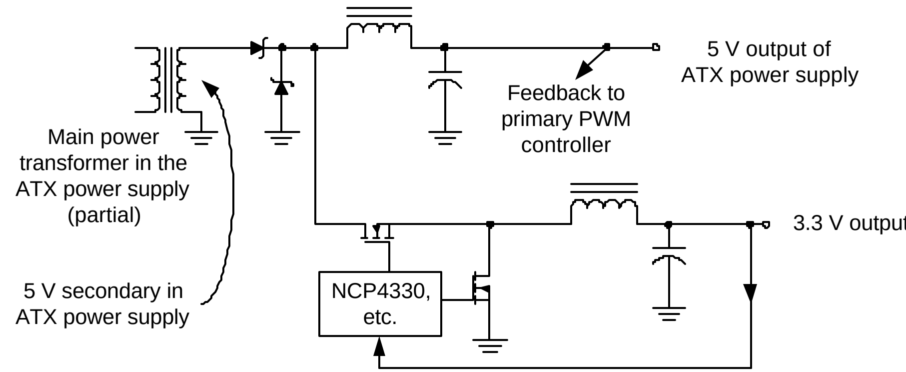
Attribute	1-Sw Forward	Active Clamp	Active Clamp Comments
Dmax	0.5 (0.46)	0.65 (0.6)	Higher D leads to several advantages
Vds/rating	850/900 V	656/800 V	Limits switch voltage, no leakage spike effects
Np/Nreset	115/115	150/None	No reset winding
Iprim (rms/pk)	1.78/2.81 A	1.56/2.15 A	Lower currents
Additional needs	Reset wndg Reset diode Snubbers	Clamp switch Drive ckt Clamp cap	⇒Low current ⇒Floating drive req'd ⇒Low value (nF), HV
Inductor	2.08 uH	1.6 uH	23% reduction in Inductor for same freq.
Sec. peak V	18.5 V	14.2 V	More margin for 24 V
Transformer	1-Q operation	2-Q operation	Better core utilization

ATX Block Diagram



3.3 V Post Regulation





Mag-amp regulation

- Traditional solution
- Works at low freq.
- No synchronous rectification – low eff.

Switching regulation

- Emerging solution
- Can go to high freq.
- Synchronous rectifier leads to >2% gain in efficiency
- More integration feasible

NCP4330 at a Glance

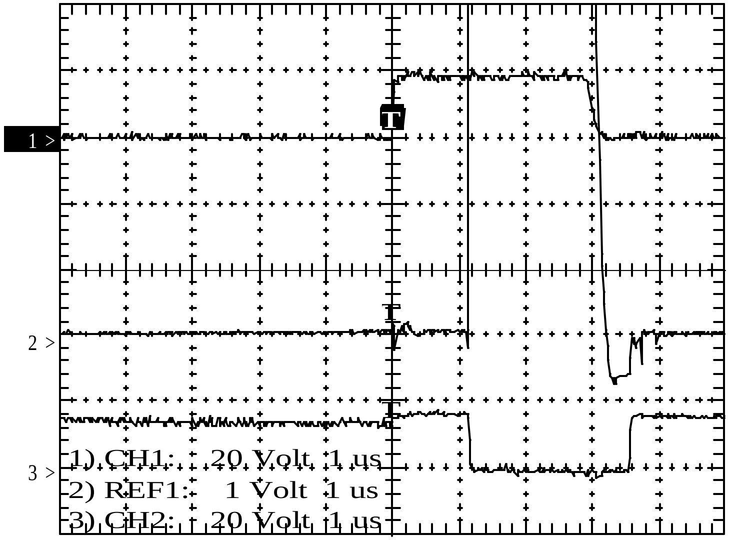
Features

- Undervoltage Lockout
- Thermal Shutdown for Over-Temperature Protection
- PWM Operation Synchronized to the Converter Frequency
- High Gate Drive Capability (Source 0.5 A - Sink 0.75 A)
- Bootstrap for N-MOSFET High-Side Drive
- Over-Laps Management for Soft Switching (3 out of 4 are smooth switching)
- High Efficiency Post-Regulation
- Ideal for Frequencies up to 400 kHz

Typical Applications

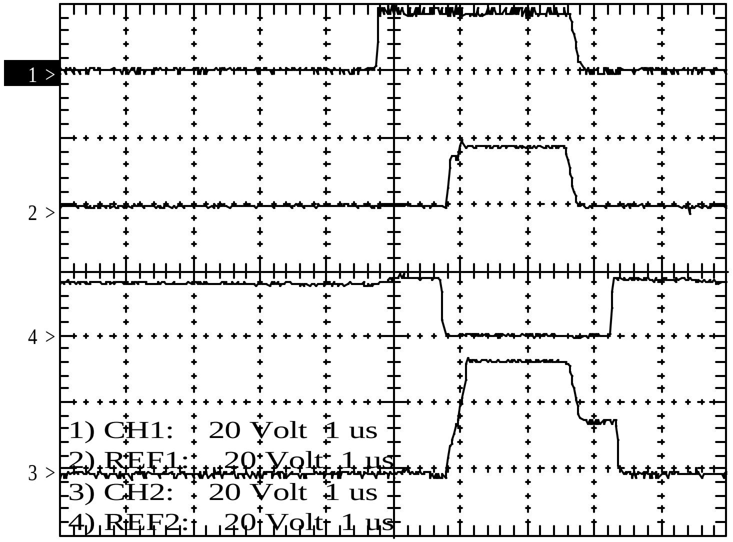
- Off-line Switch Mode Power Supplies
- Power DC-DC Converters

NCP4330 Based Solution



NCP4330 CCM Waveforms

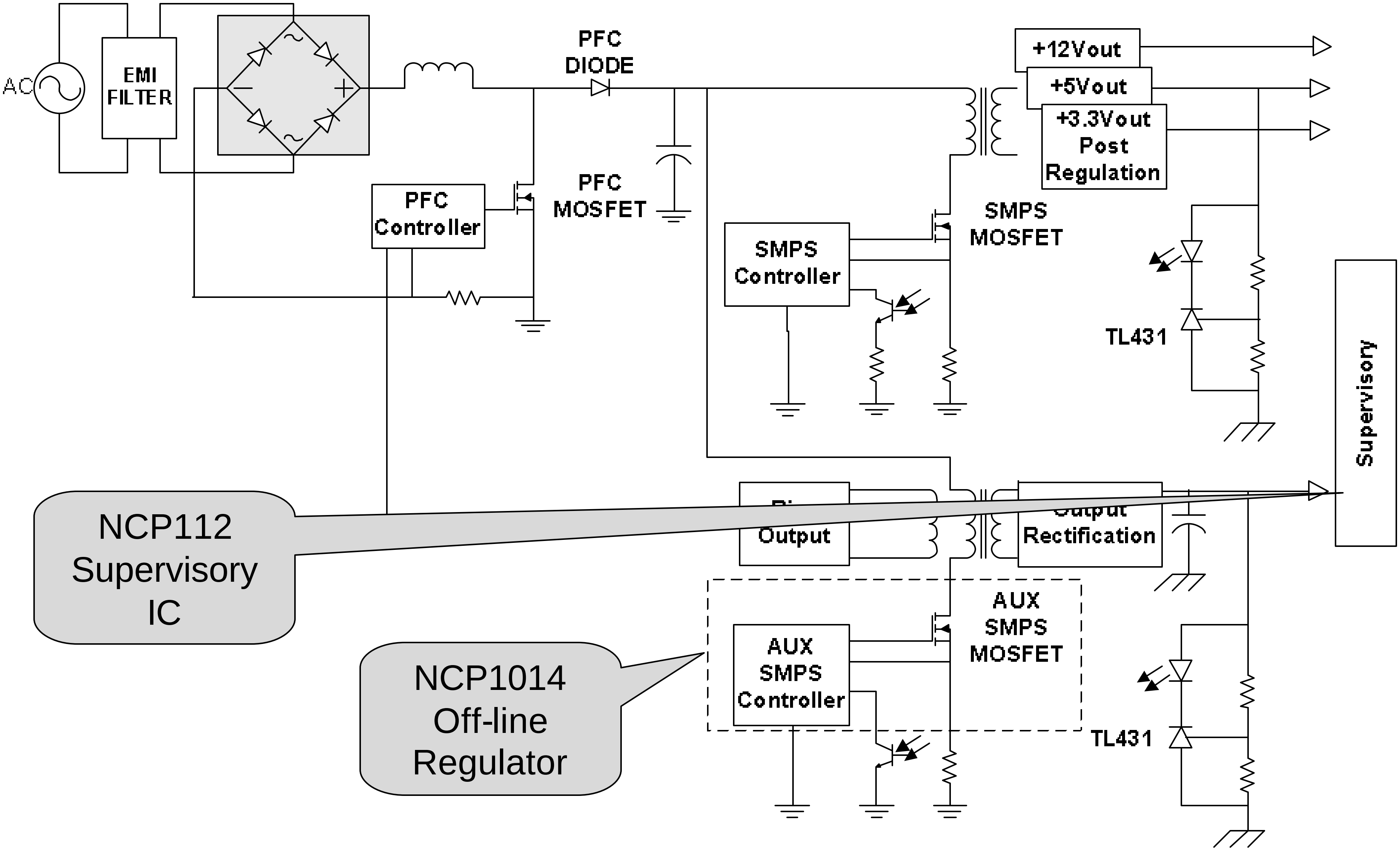
1. 5 V secondary after the 5 V rectifier (from the 300 W ATX supply).
2. Input to the 3.3 V output inductor.
3. Lower gate drive.



NCP4330 DCM Waveforms

1. 5 V secondary after the 5 V rectifier (from the 300 W ATX supply).
2. Input to the 3.3 V output inductor.
3. Upper gate drive.
4. Lower gate drive.

ATX Block Diagram



NCP101X – Self-supplied Monolithic Switcher For Low Standby-power Off-line SMPS

ON Semiconductor

Description

The NCP101X series integrates a fixed-frequency (65-100-130kHz) current-mode controller and a 700V voltage MOSFET (11Ω and 23Ω) . Housed in a PDIP7 package, the NCP101X offers everything needed to build a rugged and low-cost power supply, including soft-start, frequency jittering, skip mode, short-circuit protection, skip-cycle, a maximum peak current setpoint and a Dynamic Self-Supply (no need for an auxiliary winding).

Applications

- Auxiliary Power Supply
- Stand-by Power Supply
- AC/DC Adapter
- Off-line Battery Charger

Features	Benefits
Current-Mode control	Good audio-susceptibility Inherent pulse-by-pulse control
Skip-cycle capability	Provides improved efficiency at light loads No acoustic noise
High-voltage start-up current source	Clean a loss less start-up sequence
Dynamic Self-Supply (DSS)	No Auxiliary winding
Internal Short–Circuit Protection independent of aux. voltage by permanently monitoring the feedback line	Reliable short circuit protection, immediately reducing the output power
Reduced optocoupler consumption	Further improvement of stand-by behaviou
Frequency jitterin	Reduced EMI signatur

Ordering Information

NCP101XAP06, NCP101XAP10 NCP101XAP13: PDIP7 = 50/Tube

More Information Online: www.onsemi.com/NCP1010

- Datasheet: NCP1010/D
- Application note: ANXXX
- Limited Demoboards for large opportunities to come.

Device Detail - Standby

NCP112 Supervisory

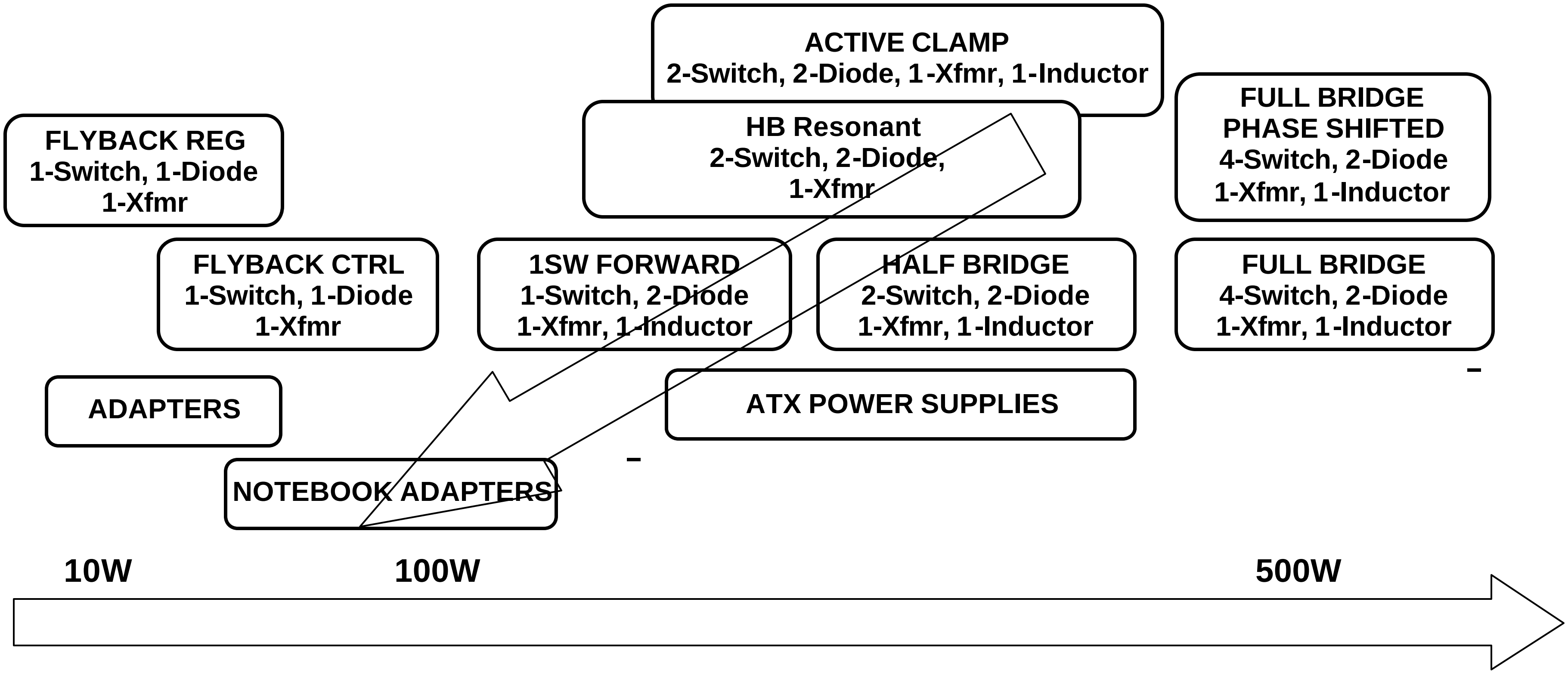
Description
The NCP112 incorporates all the monitoring functions required in a multi-output power supply. It can monitor 3 outputs and communicate their status to a system controller with programmable delays to prevent spurious operation. Functionally and pin-compatible to other supervisory ICs, the NCP112 provides improved performance .

Applications
- Desktop ATX Power

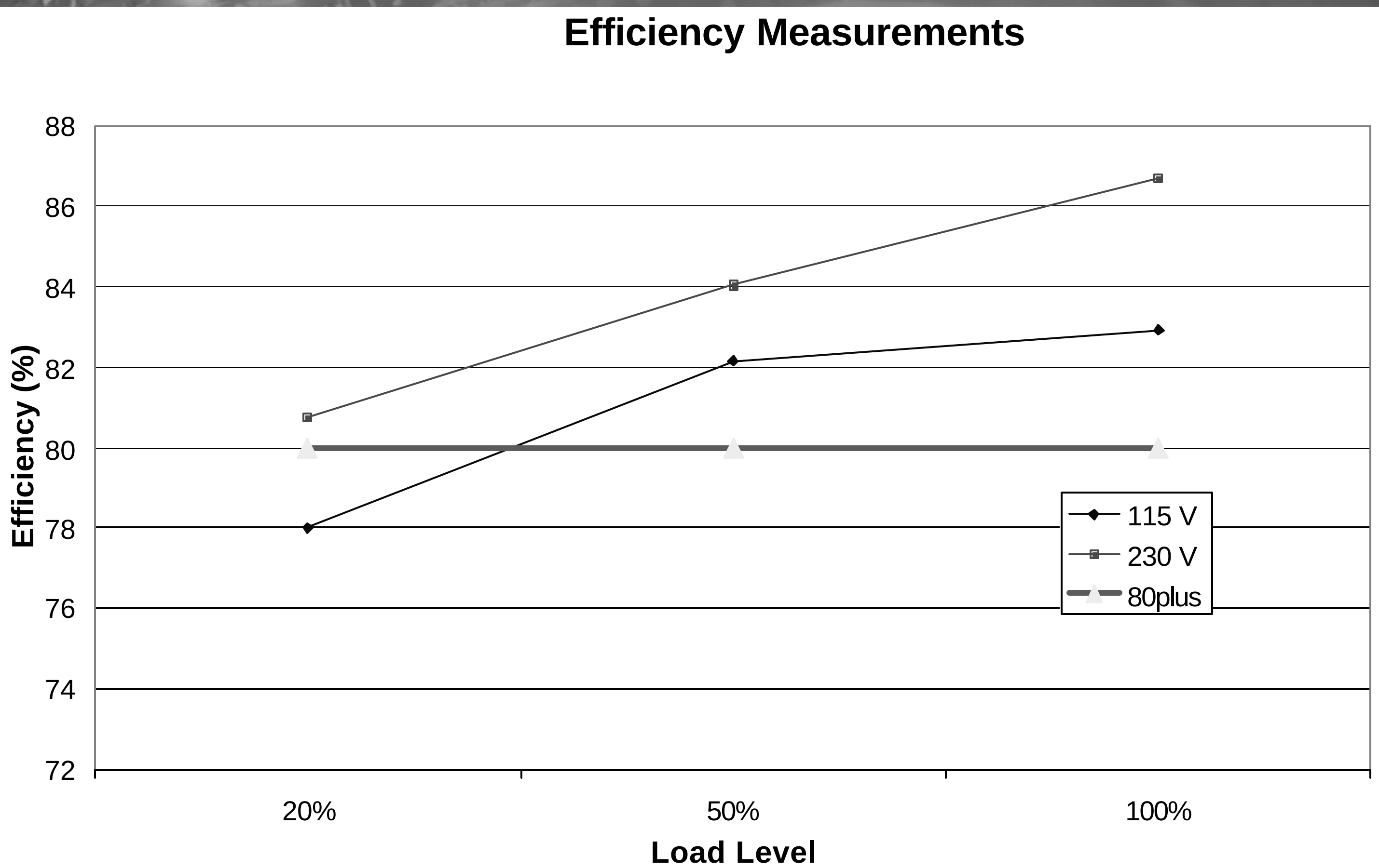
Features	Benefits
Overvoltage and undervoltage protection for 12 V, 5 V and 3. 3 V outputs	Minimizes external components
• Additional uncommitted OV protection input • Programmable UV blanking during powerup	Extra flexibility Accommodates any startup characteristics
• Fault o/p with enhanced (20 mA) sink current	Guarantees shutdown under fault conditions
Programmable on/off delay time Programmable power good delay time	Allows system specific flexibility

SMPS Topologies Progression

- Higher power applications are technology leaders
  - Spillover to lower power as technology matures
- External power supplies are market impact leaders
  - Can drive innovation through customer perception



Complete System Results

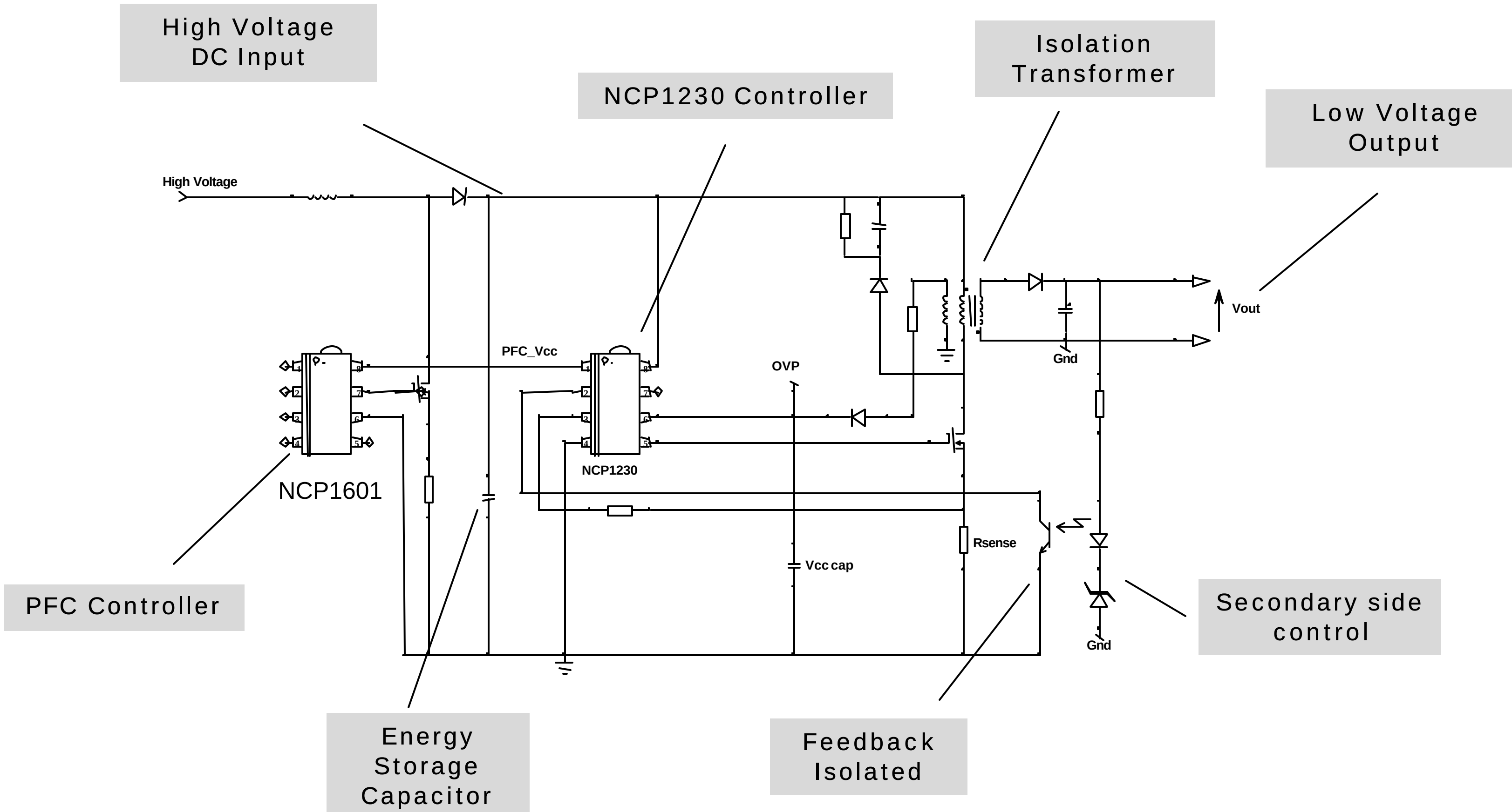


- THD at high line – 9 % (meets IEC1000-3-2)
- Input power at Vin=115 Vac and Standby load =0.5 W is <1.0 W

High Power Adapter Requirements

- Increasing power levels for mainstream applications
  - 50 W (2002), 100 W (2004) => 150 W (2006)
- Need for low standby power consumption
  - 1 W (2004) => 0.5 W (2005)
- Addition of PFC requirements for > 75 W
- Output voltages from 15 to 24 V
- Need for **high** efficiency (>85%), **small** size, **low cost**

Typical Application Circuit

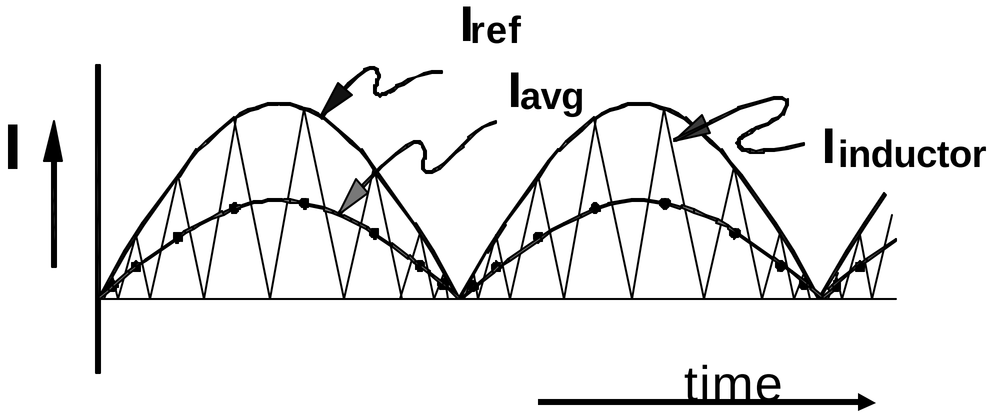


Few external components ⇒ Reduces overall power supply cost and size

Critical Conduction Mode (CRM)

• The instantaneous inductor current varies from zero to the reference voltage. There is no dead time.

• The average inductor current follows the same wave-shape as the input voltage, so there is no distortion or phase shift.



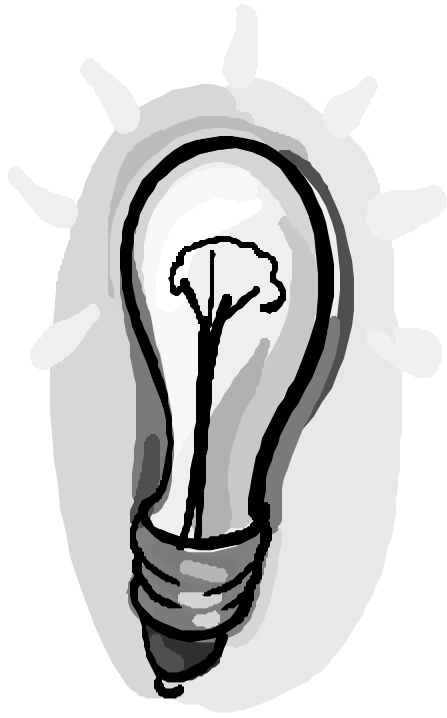
- CRM suffers from large switching frequency variations:
  - power factor degradation in light load conditions.
  - high switching losses unless a large and expensive coil is implemented.
  - Last but not least:
    - difficulty to filter the EMI
    - risk of generating interference that disturb the systems powered by the PFC stage (tuner, screens).

NCP1601 Basics

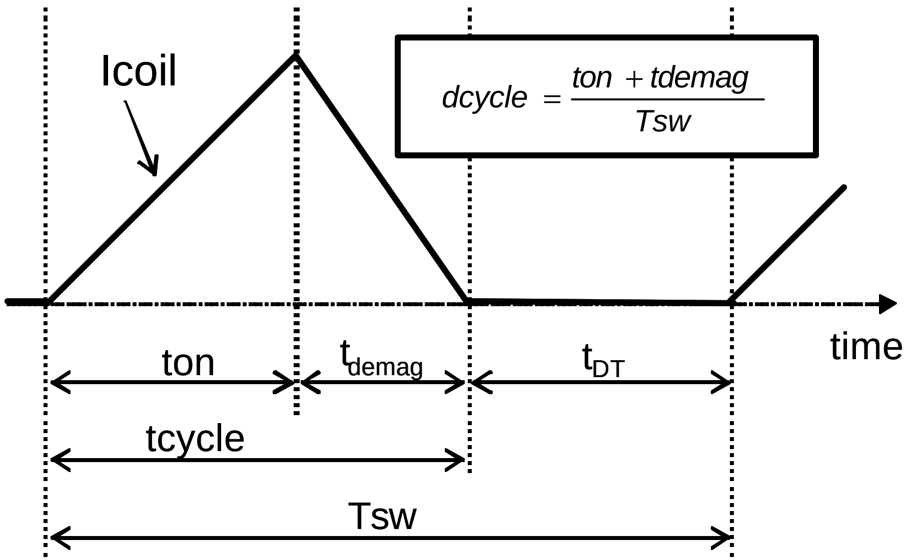
- Why not to associate fixed frequency and Discontinuous Conduction Mode?

- If furthermore, the circuit can enter CRM without PF degradation while in heavy load, there is no RMS current increase due the dead-time presence.

- Couldn’t it be the ideal option for low to medium power applications?



NCP1601 Principle



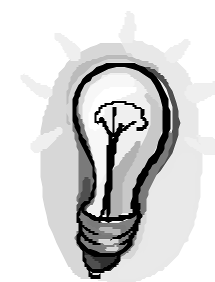
The averaged coil current over one switching period is:

$$\langle Icoil \rangle_{Tsw} = \frac{Vin}{2 * L} * \left(ton * d_{cycle} \right) = Iin$$

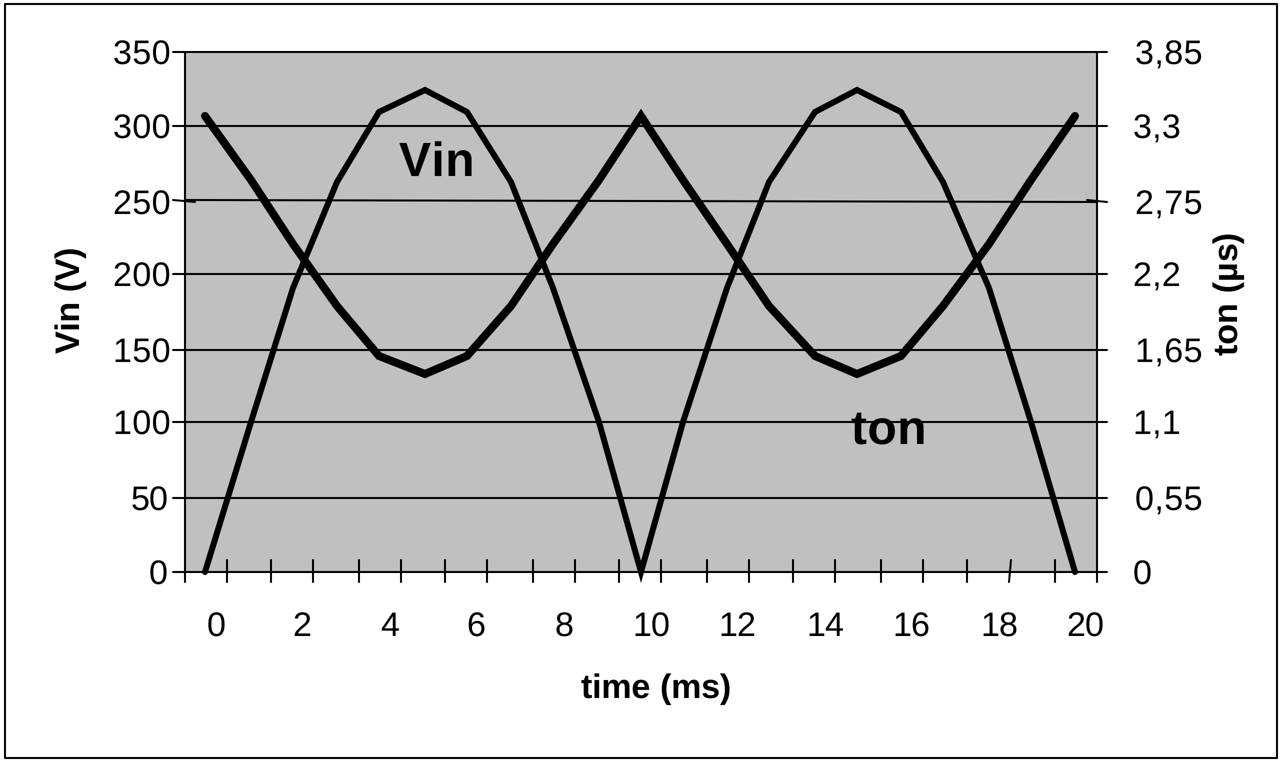
If (ton*dcycle) is made constant:

⇒ the input current is proportional to Vin

⇒ the input current is sinusoidal.

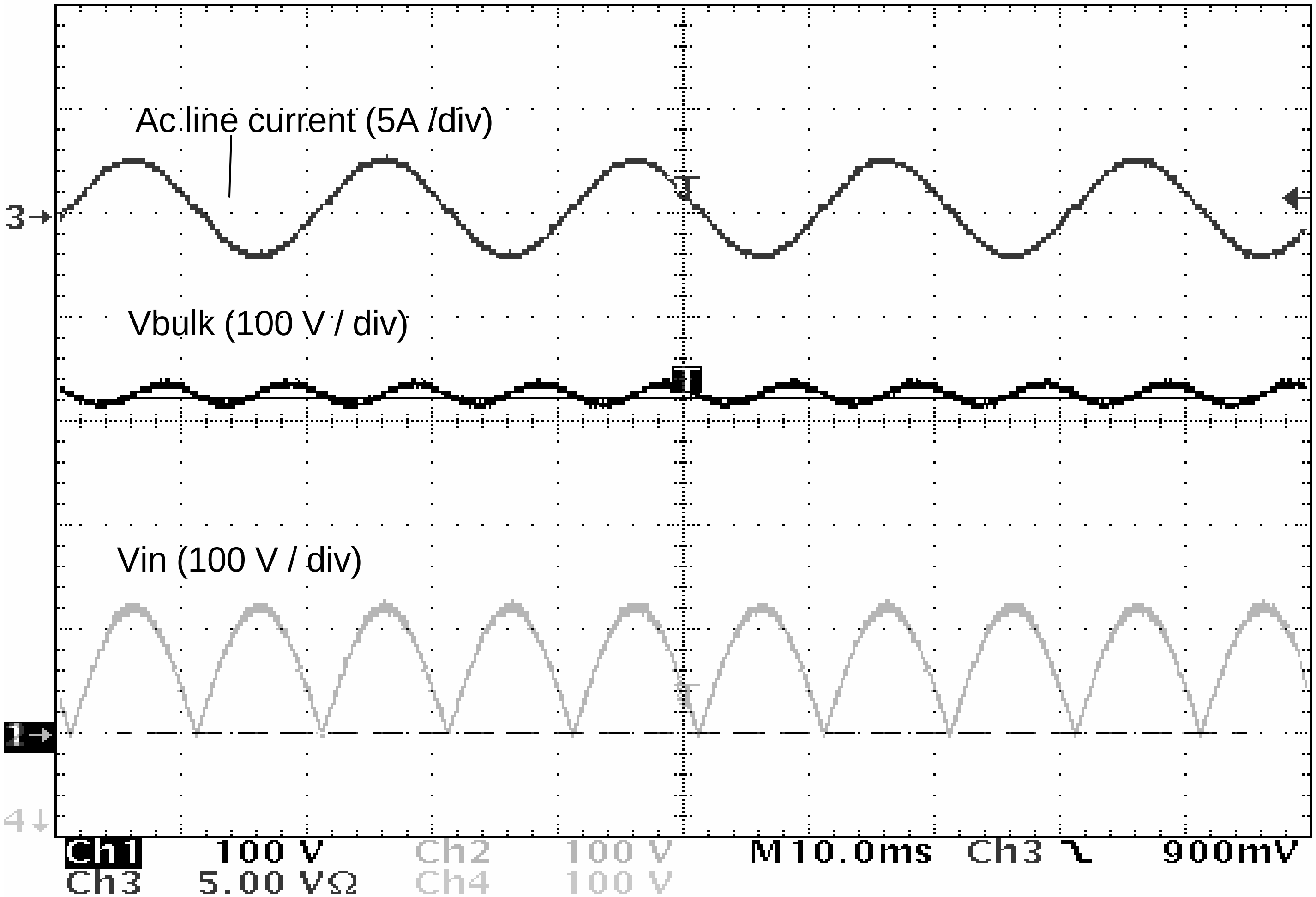


NCP1601: On-Time Modulation



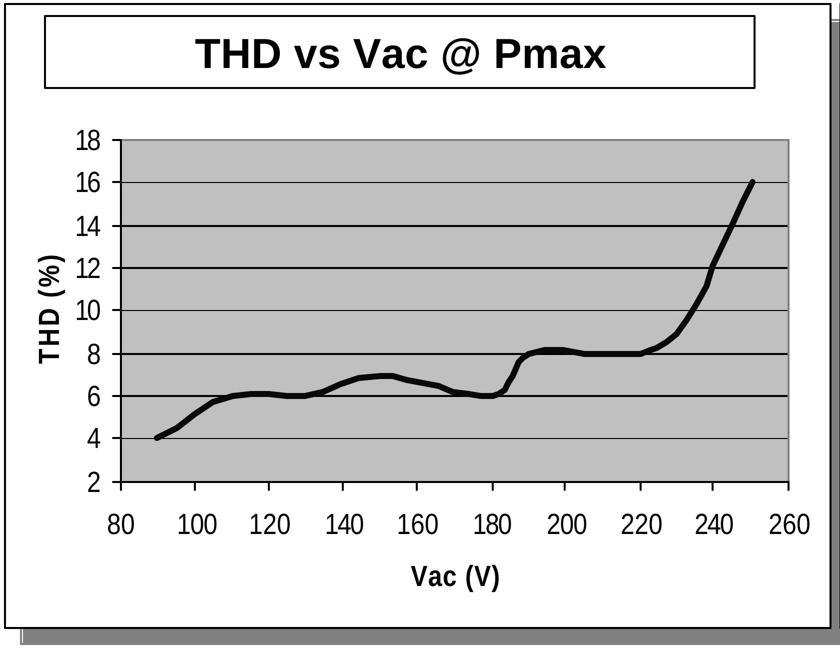
Conditions: fsw = 100 kHz, Pin = 150 W, Vac = 230 V, L = 200 µH

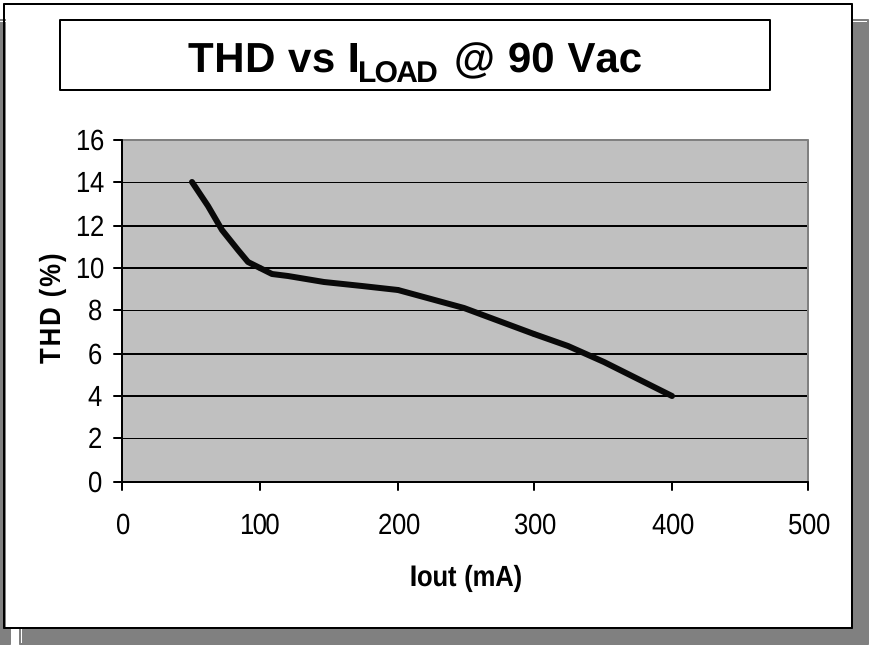
NCP1601: It works



Conditions: Pout = 130 W, Vac = 90 V, PF = 0.998, THD = 4%

NCP1601 THD Performance



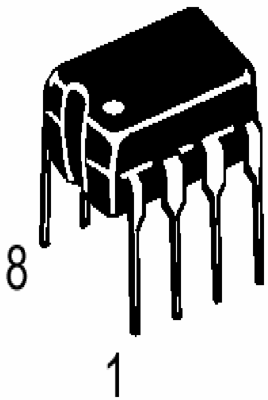


The NCP1601 yields high PF ratios and effectively limits the Total Harmonic Distortion over a large ac line and load range.

NCP1601 at a glance

According to the coil and the oscillator frequency you select, the NCP1601 can:

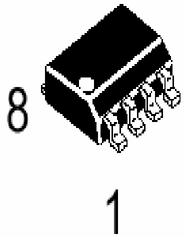
- Mostly operate in Critical Conduction Mode and use the oscillator as a frequency clamp.
- Mostly operate in fixed frequency mode and only run in CRM at high load and low line.
- Permanently operate in fixed frequency mode.



In all cases, the circuit provides near-unity power factor.

The protection features it incorporates, ensures a reliable and rugged operation.

Housed in a DIP8 or SO8, it requires few external components and eases the PFC implementation.



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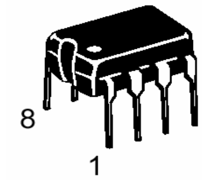
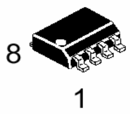
NCP1230 – Low-standby High Performance Controller





Features	Benefits
• Current-Mode control	➔ Good audio-susceptibility ➔ Inherent pulse-by-pulse control
• Skip-cycle capability • Soft skip mode (NCP1230A only)	➔ Provides improved efficiency at light loads ➔ No acoustic noise
• Go To Standby for PFC stage or main PSU	➔ Disable the front end PFC or main PSU during standby ➔ Reduces the no load total power consumption
• High-voltage start-up current source	➔ Clean a loss less start-up sequence
• Internal Short–Circuit Protection independent of aux. voltage permanently monitoring the feedback line	➔ Reliable short circuit protection, immediately reducing the output power
• Internal Ramp Compensation	➔ Saves components ➔ Suitable for continuous mode FB with DC >50%
• Frequency jittering	➔ Reduced EMI signature
• Latched Primary Over voltage and Over current protections	➔ Rugged Power Supply

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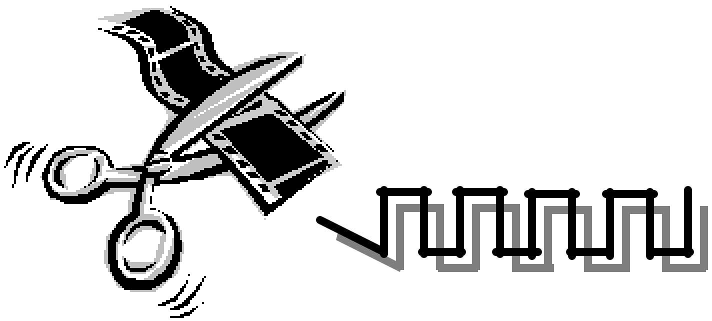
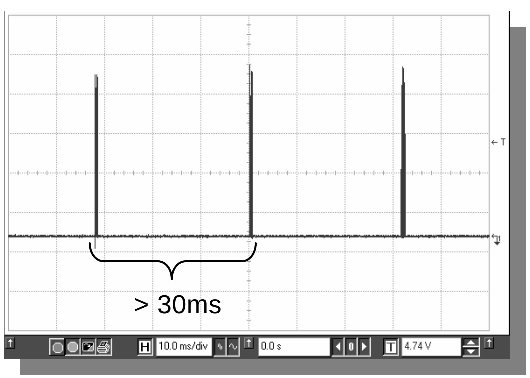
How to reduce the standby power?

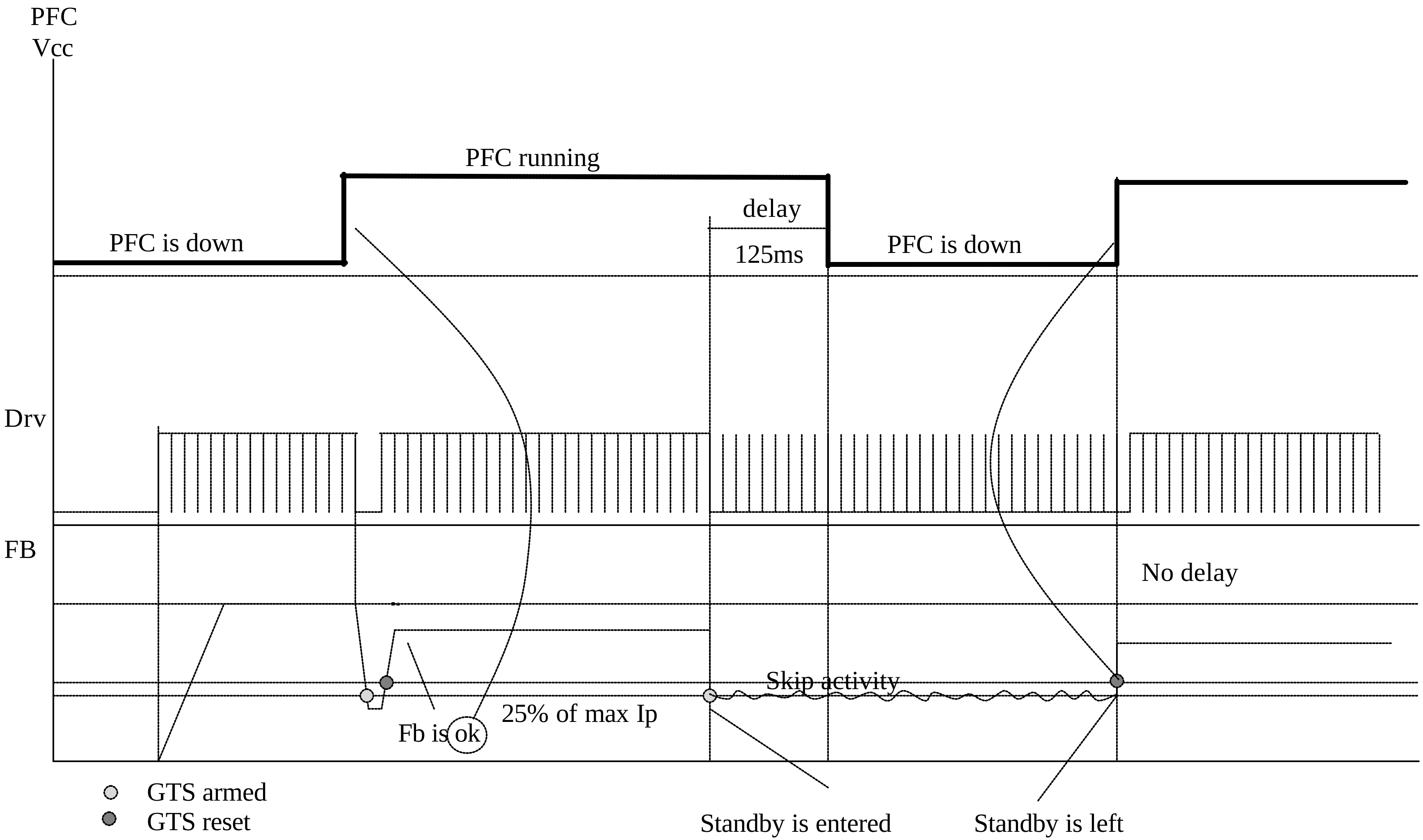




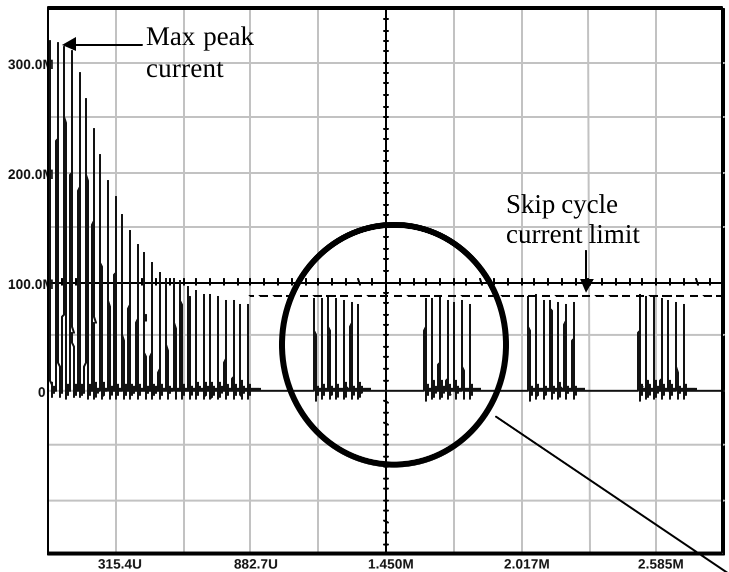
Skipping un-wanted switching cycles:
The *skip* mode…

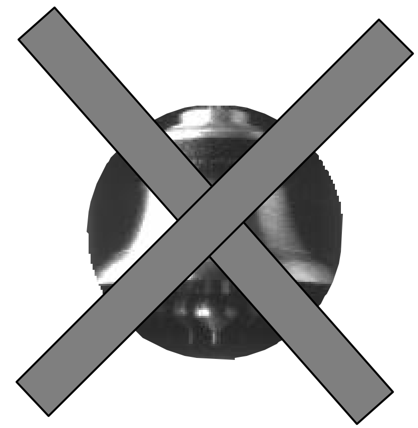
- excellent no-load standby power
- reduces switching losses
- improves low load efficiency
- cheap implementation!

Observing the loop to detect the **standby**



NCP1230 Skip Cycle



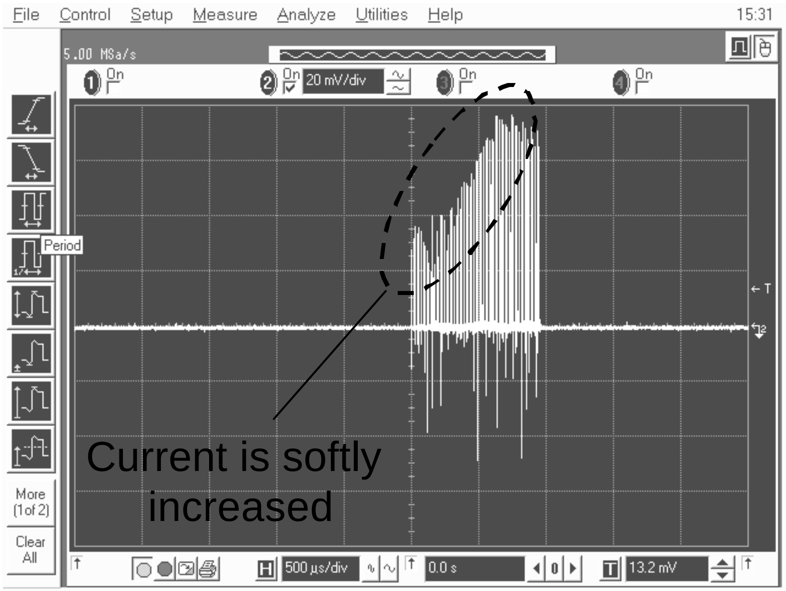


Cycle skiping in standby

Advantages

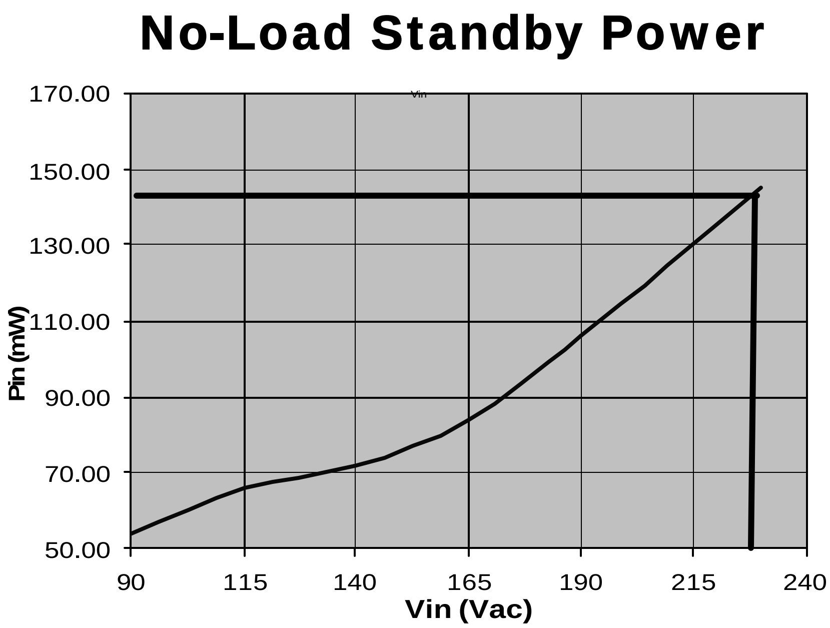
- Reduce the average input power drawn from the line (standby power)
- No acoustic noise → A low cost magnetic component can be used
- Under fault conditions, reduces the stress on the power components

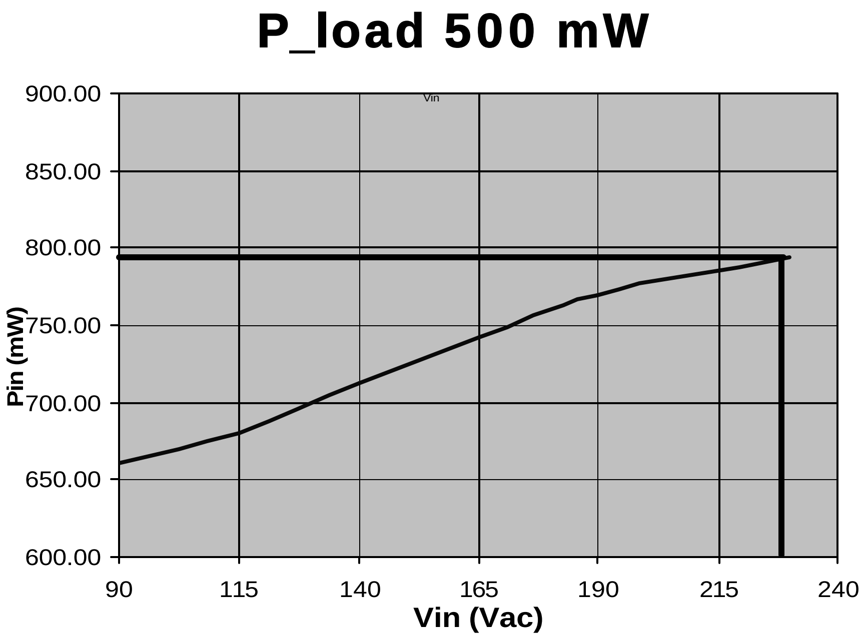
Skip Cycle Operation



Reduces further the acoustical noise!

Final standby power measurements





Standby power @ no-load = 145 mW
Pactive mode = 794 mW @ 230 vac

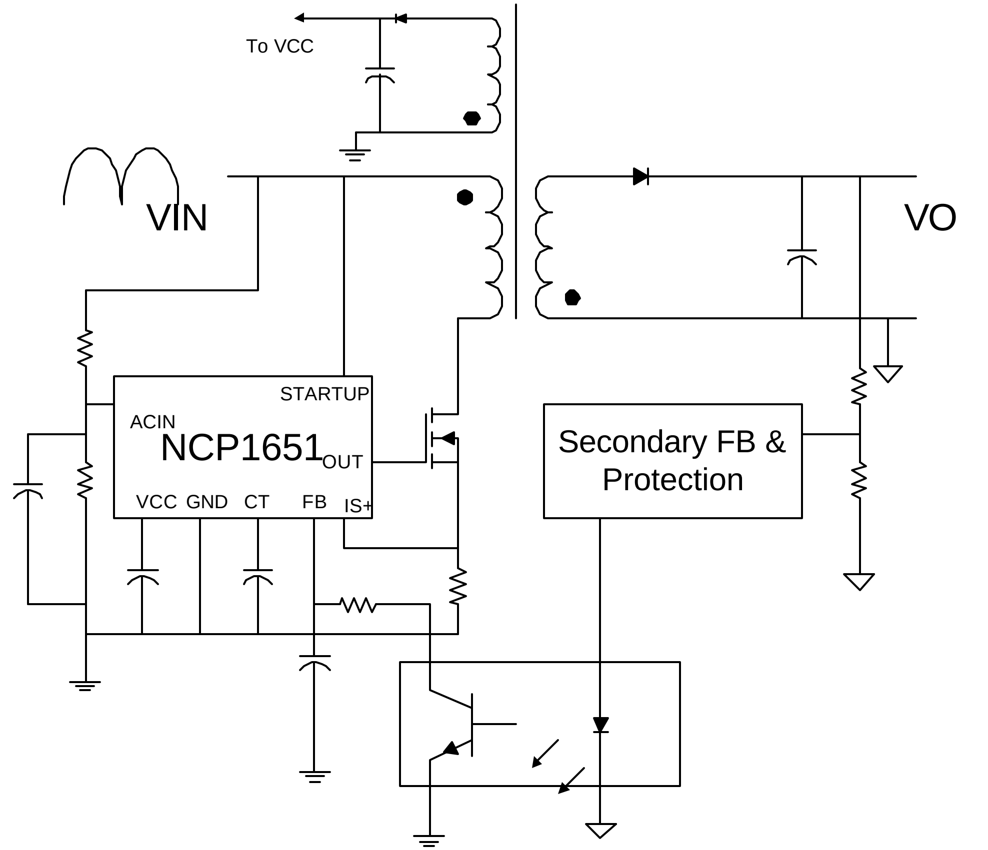
Single Stage Topology

Advantages

- Elimination of **one** power processing stage
- Requires a **single** switch, **single** magnetic, **single** rectifier & **single** cap.
- Ideal for mid-high output voltage systems (12-150 V)

Beware

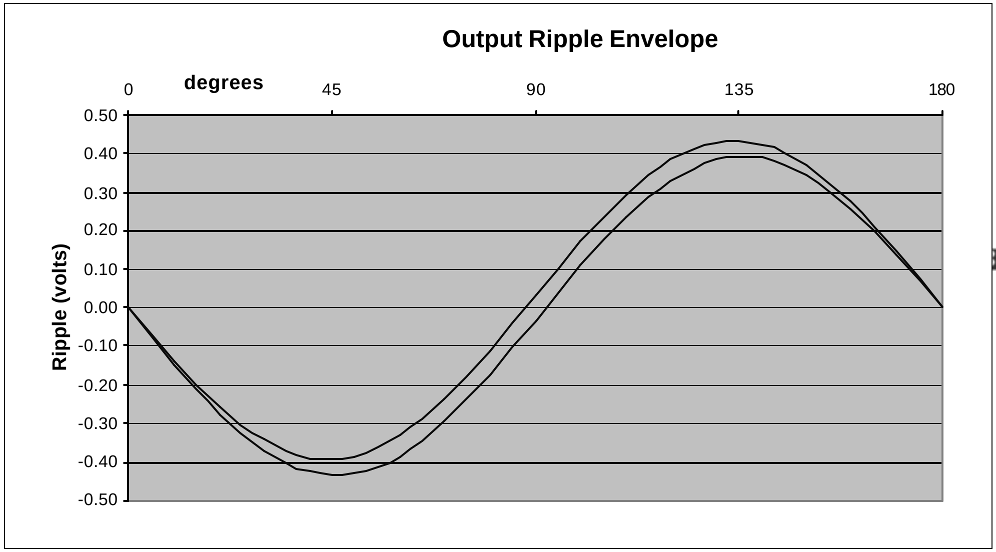
- Low frequency output ripple can be high

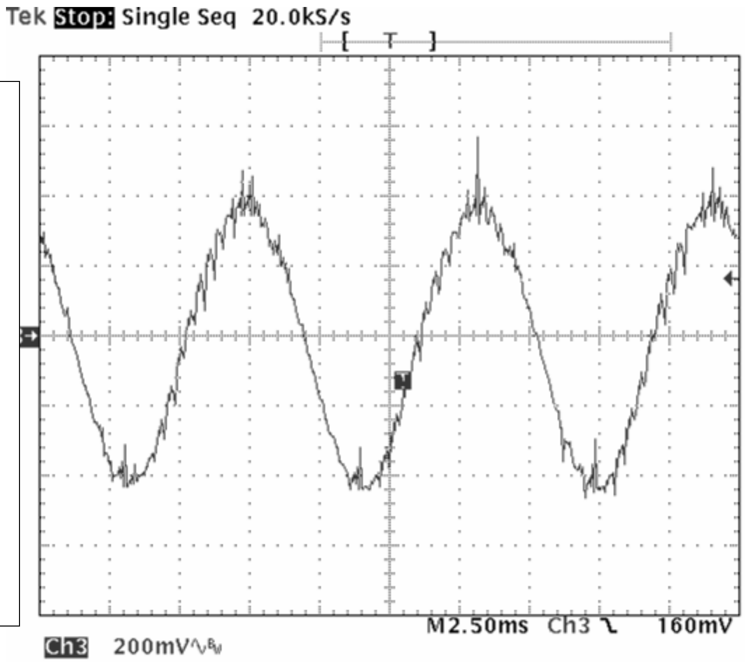


Component Comparisons

	2-stage converter (with critical mode PFC)	1-stage converter
Input peak current	~3.5 A for 90 W	~3.5 A for 90 W
PFC MOSFET	500 V	800 V
Inductor	600 uH	600 uH (need secondary windings)
PFC Rectifier	600 V, ultrafast (4 A)	Not needed
PFC capacitor	100 uF, 450 V	Not needed
SMPS transformer		Not needed
SMPS Switch	600 V or higher	Not needed
Output capacitor	X uF	4X uF

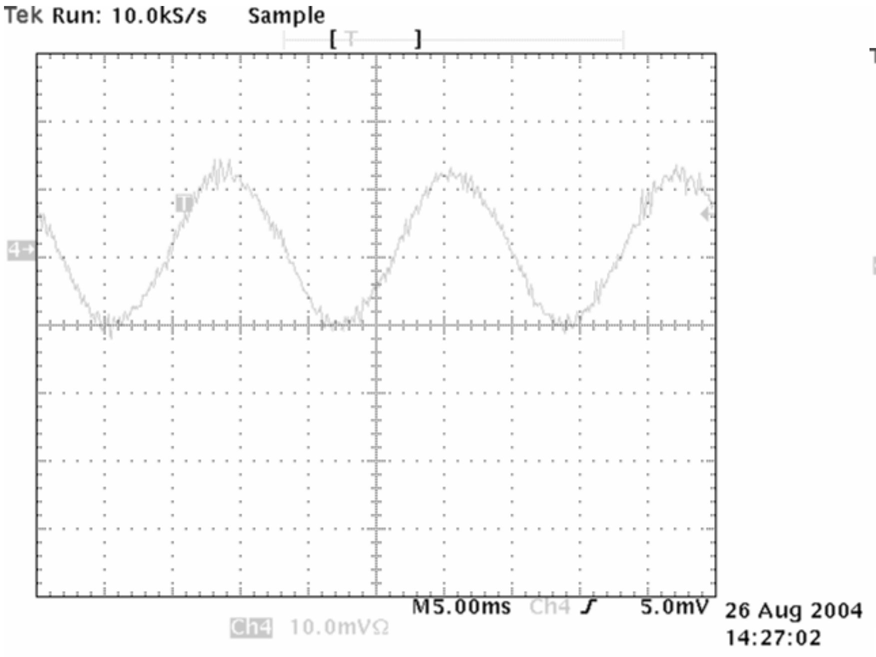
Results – Output Ripple



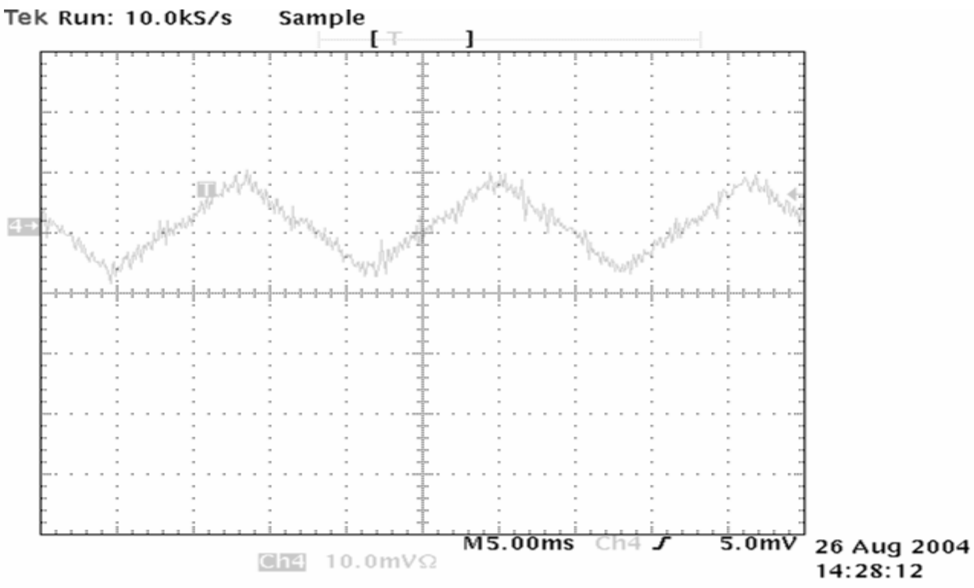


- Output ripple is dominated by 120 Hz signal
  - Inversely proportional to output capacitance value

Results - Input Current Waveforms



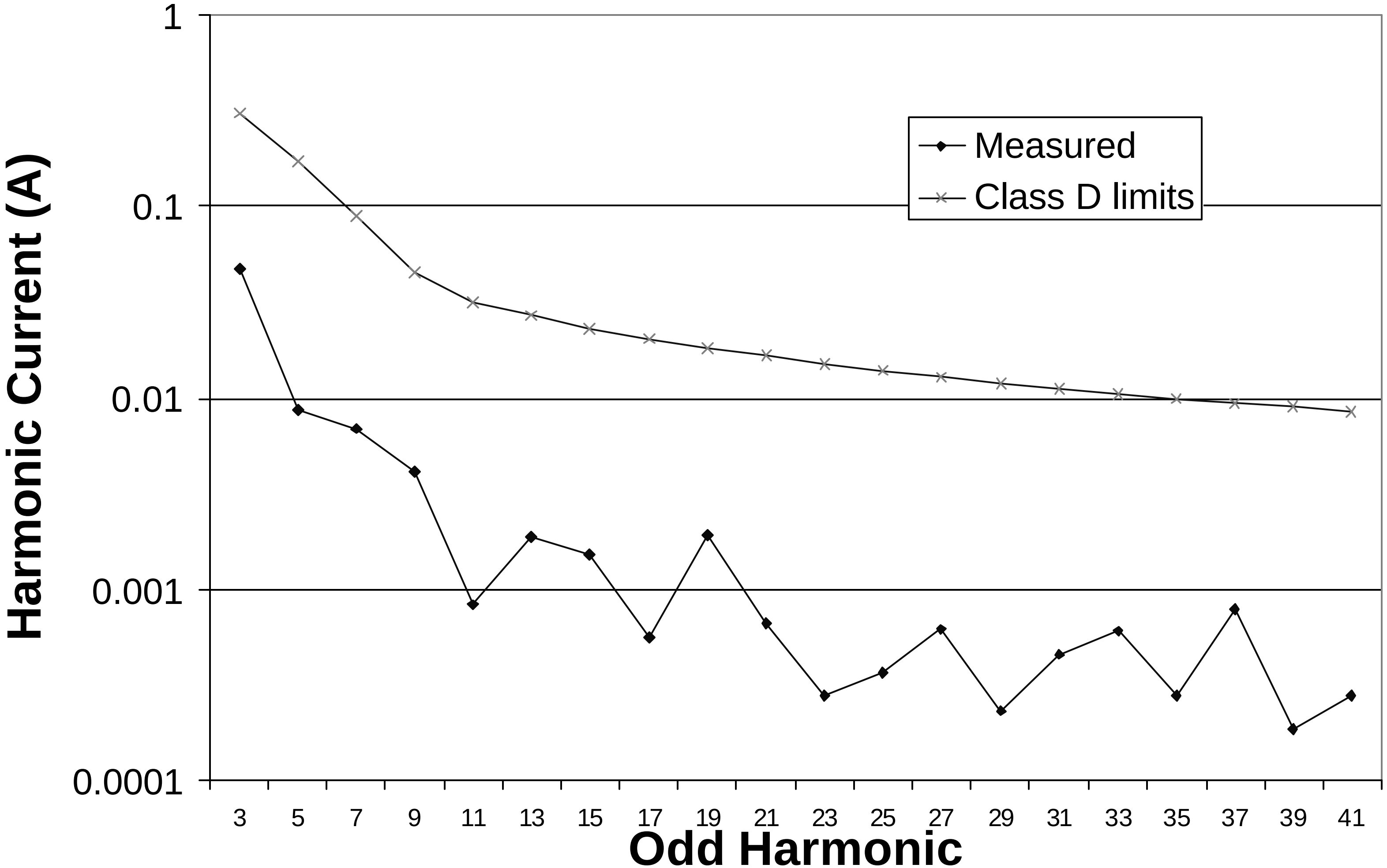
Vin = 115 V



Vin = 230 V

- Easily meet the high-line requirements for IEC1000-3-2
- THD can be improved with better snubbers or higher inductance (trade-off with losses)

IEC 1000-3-2 Compliance



Results – Regulation and Efficiency

- Regulation meets the typical specifications
  - Output line regulation: 20 mV
  - Output load regulation: 20 mV
- No Load power (at 230 V input) = 465 mW
  - Meets all stringent existing requirements
- Full load efficiency at 90 V input = 85.90 %
  - Compares favorably with optimized 2-stage designs
  - Meets the CECP and EPA requirements

Conclusions

- Efficiency improvements are key to achieving regulatory and market requirements for NB adapters and DT power supplies
- This seminar showed the means to achieve these cost effectively
- Stay tuned for more exciting computing power solutions from ON Semiconductor