Design Solutions for Preventing Process Induced ESD Damage during Manufacturing of Interconnects

J. Ackaert[1], B. Greenwood [2]
1)On semiconductor, Westerring 15, 9700 Oudenaarde, Belgium
2)On semiconductor USA
Tel: (32)-55-332343 Email: jan.ackaert@onsemi.com

1. Abstract

ESD problems are commonly thought to be an electrostatic discharge event through the device pins. All known models like HBM, MM, CDM are based on this assumption. During assembly discharge into devices, directly into the surface is also well known. Pad – related, ESD protective structures are useless against this ESD-surface-discharge-path, called ESDFOS [1]. Little is known however on the impact of simple wafer cleaning/spraying as used frequently during the wafer manufacturing itself. In many cases these processes do include high risks of generating electrostatic charge; subsequent discharge into devices and can easily induce ESD-like events internally in the interconnect circuitry of a device. In this paper, charging induced damage (CID) into common metal interconnect is reported. The damage is caused by the build up of charges on a resist surface during a water rinsing step. This charging is inducing a mirror charge on the interconnect circuitry and results in a discharge through the inter metal dielectric layer (IMD) towards a grounded structure. This CID can lead to direct severe yield loss. In milder cases the damage is difficult to detect but is proven to result in reliability issues. The charging has been detected, measured and evaluated with the help of a non contact surface potential measurement. The phenomena has been characterized and quantified. This paper is describing the occurrence of the failures, the design of the test structures, the measurement results. This work is concluding on how a design can be made safe from ESDFOS during processing by applying the popper layout rules.

1. Introduction

In common understanding, electrostatic discharge (ESD) is known as a charge introduction into or out from a semiconductor device via its pins, following specific models like HBM (human body model), CDM (charge device model) or MM (machine model).
All usual methods to avoid ESD are focused on device design (pad protective structures) and ESD protection zones in the production, where most attention is paid to antistatic clothing, shoes, workplaces, floors and robotic handling [1]. Lots of effort has been done in the last three decades in order to improve in these areas, but much less activities were done considering ESD risks generated by inherent processing steps such as cleaning and coating itself.
In several investigations failures were observed resulting from surface ESD-impacts. Direct discharge into the device interlevel dielectric (ILD) caused defects raging between very small shorts of the top metals and large craters in the ILD. In such case, the ‘‘classical” way of ESD via the pads was bypassed, such eliminating the pad protective structures.
Earlier work describes charging affects specific for metal-insulator-metal capacitors devices (MIMC) [2]. For the first time however a charging phenomena is describe occurring simple during spin rinsing with DI water affecting common metal interconnects in semiconductor devices.

Fig.1: SEM picture of severe defects after an internal ESD event between interconnect networks. The blue are the remain of the metal lines

This paper is describing how the charging has been detected, measured and analysed with the help of a non contact surface potential measurement. The phenomena has been characterized quantified. Proposals are made on how to make a layout failsafe from ESDFOS by design.

2. Experimental

The defects were discovered right after the definition of the via mask on top of the ILD covering the interconnect networks. The defect itself is located where the a floating partially processed network is in close proximity to a grounded network already connected to silicon. In order to determine the parameters that have an affect of the occurrence of the discharging, special set of test structures have been designed and manufactured. As depicted in Fig. 2, a

large electrically floating metal feature is designed close to a grounded metal line.

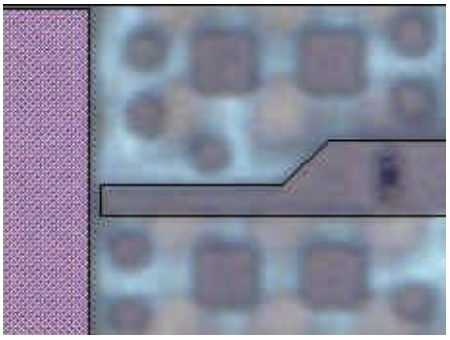

Fig.2: Picture of the test s structure with on the right side a grounded metal stripe and on the left side a metal line connected to a large floating metal.

Variations are made in the area of the metal feature and the spacing between floating and grounded network. These teat structures were processed through the via module where the defects were observed previously.

3. Measurements.

De EDS events have been measured optically and electrically Very much like oxide punch trough caused by ESD, an electric field over the IMD in between the metal feature and the grounded metal line had sufficient magnitude to causes breakdown allowing charge collected in the capacitor to pass. Because the oxide is a poor thermal conductor, the discharge is confined to a very small region, causing high energy densities and rapid temperature rise [3].

In case of aluminum, the thermal expansion is more than that of the surrounding oxide, while the melting points behave vice versa. In case of an ESDFOS spark, the aluminum immediately melts and expands, while the oxide around suffers cracking. The molten and expanding aluminum, thus generating very small shorts between both top metals, fills these cracks (Fig. 3). A large variation of the severity of ESD events have been observed ranging from large craters in the ILD to minimal cracks: Fig 3.

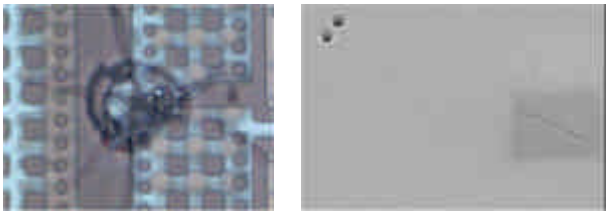

Fig.3 ESD events that can be observed optically range from large craters (left) to minimal cracks (right)

Electrically the events have been detected as a short between the floating interconnect network and grounded metal line. Fig 4 is depicting the location of the optical observations and the location and frequency of the electrical observations. All defects are located in the center of the wafer.

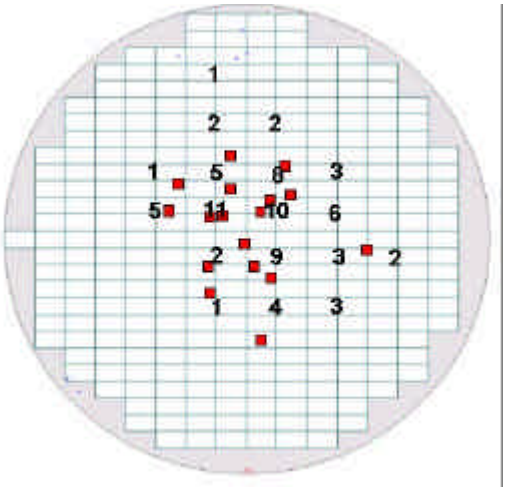

Fig.4: The location of the optical observations and the location and frequency per die of the electrical observations.

Fig. 5 is depicting the distribution of the defects as a function of the spacing between the networks both for the optical as for the electrical defects. The optically observed events are in general the more severe events that are occur with the smallest spacing. The electrically detectable defects occur at spacing wider then where the EDS events can be detected optically. With severe EDS events sufficient metal has been removed so that chance of occurrence of a metal short becomes very small

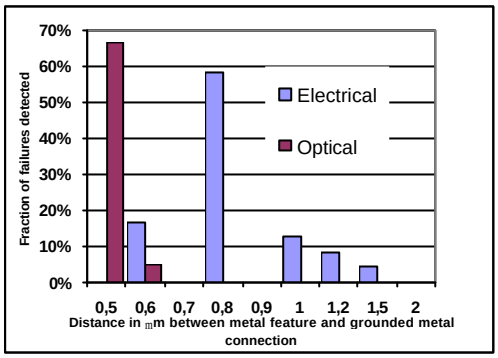

Fig.5 The distributions of the optical observations and the electrical observations as a function of spacing between the interconnect networks

Fig 6 shows the effect of stressing an apparently good device: initial good device may be affected as well and develop an electrical short after stressing. This observation is especially important towards the assessment of impact o the ESDFOS on reliability of a device. Where ESDFOS could be judged as having impact on yield only, this data shows that due to ESDFOS also failures during the lifetime of the device can occur.

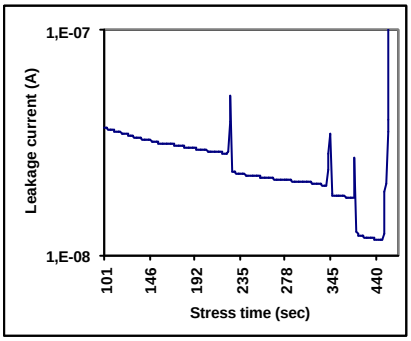

Fig.6 An initial good device may be affected as well and develop an electrical short after stressing

To investigate further on this phenomena, structures that are in between 2 failing similar structures have been analysed by cross section. Fig 7 shows the cross section of an electrical "good" device in the centre of the wafer. Clearly the traces of an EDS event are visible, still there was no electrical or optical signal to detect this device. In the cross section thin metal stringers are visible the can explain the occurrence of the short after stressing the structure as shown in Fig 6.

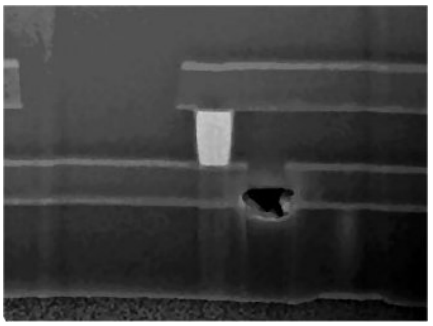

Fig.7 Cross section of an affected device without optical or electrical observable defect.

Fig. 8 is depicting the occurrence of EDSFOS events as a function area of the metal feature in the floating network. Larger metal features generate more defects. This area dependence is a clear indication that a surface charging and capacitive coupling is involved in the failure mechanism.

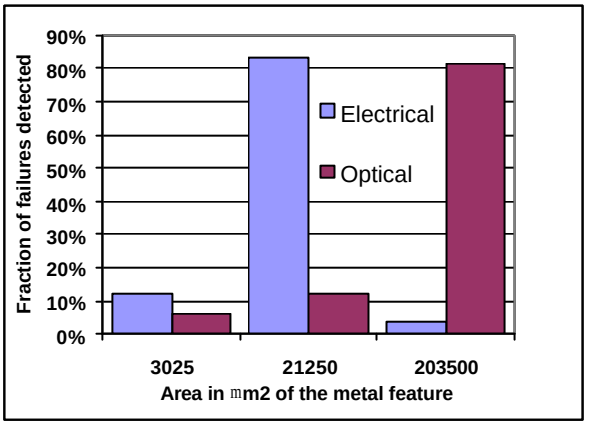

Fig.8 Cross section of an affected device without optical or electrical observable defect.

4. Surface Charging.

Taking in account the area dependence of the ESDFOS events, the surface charge density has been measured. Fig.9 is showing the surface charges of an oxide layer after spin rinsing in the same process as were the ESD events occurred on the device wafers. The highest levels of charging are measured in the center of the wafer. This is corresponding with the region of the wafer where ESDFOS events have been observed One could expect, since linear rotation speed, is highest in on the edge, that the edges would be charged most. One should know that the water jet is put on the wafer close to the centre . At the point of contact, the speed gradient between the water in the wafer is highest, causing the highest friction. When moving to the edge, the water takes over the speed of

the wafer surface, in that region, the speed gradient becomes much lower causing less friction and as a consequence, less charging.

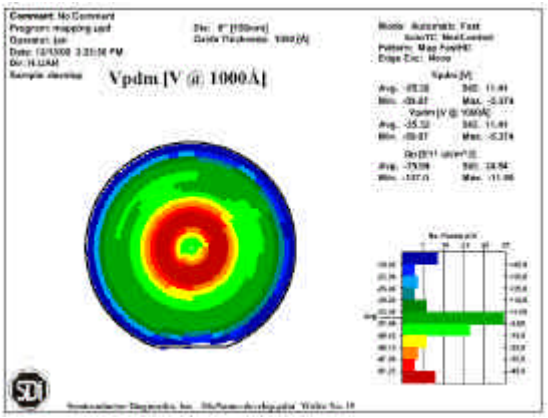

Fig 9: PDM mapping of a 1000Å **oxide layer after a spin rinse process showing –59V charging in the centre ring.**

4. Discussion

The nature of the defects as depicted in Fig. 1 points in the direction of ESD like discharge. Therefore the distribution of the surface charging as generated by the via mask process was mapped by means op non contact surface potential measurements. The mapping is presented in fig 9. As can be observed, there is a highly charged location in the centre of the wafer corresponding with the location of the defects. Fractioning of the processes revealed that the water rinsing step is sufficient the generate the defects.

The most efficient way to prevent the ESDFOS to have impact on the circuits is to ensure that by design a is safe distance is kept between large area floating interconnect networks and networks connected to silicon already. From figure 5 we can conclude that for the given devices processed in the given conditions, 2µm could be considered as a safe distance: No defects have been observed at with a spacing between the networks larger than 2µm. However taking in account that devices that look not affected by the ESDFOS still might show failures during the lifetime, and extra safety margin needs to be taken in account.

Considering the spacing between the interconnect networks, certainly some hundreds of volts were achieved to obtain such damage.

The 59V as measured by the PDM, is too low the cause the observed ESD like defects. One has to realize that ESD type defects are not only caused by the voltage potential but in fact by electric field. In the given circumstances, there is a point shaped conductor in front of a large conductor. Under these conditions, electric field can be increased easily by an order of magnitude [4].

5. Conclusions.

Earlier work describes charging affects specific for metal-insulator-metal capacitors devices (MIMC) [2] In this work a charging phenomena is described, occurring simple during spin rinsing with DI water affecting common metal interconnects in semiconductor devices.

Simple wafer cleaning/spraying includes high risks of generating electrostatic charge; subsequent discharge into devices and can easily induce ESD-like events internally in floating interconnect circuitry of a device. The effect of the ESD event can rage from an easy detectable defect all the way to a subtle defect revealing itself after electrical stressing. These present a threat towards the reliability of the device. The occurrence of this defect mechanism can be prevented by implantation of proper design rules.

References

[1] S Peter Jacob Surface ESD (ESDFOS) in assembly fab machineries as a functional and reliability risk–failure analysis, tool diagnosis and on-site-remedies.ESREF (2008)

[2] J. Ackaert, Z. Wang, E. De Backer, P. Coppens, Charging Damage in Floating Metal-Insulator-Metal Capacitors, 6th International Symposium on Plasma Process-Induced Damage, pp. 120-123, 2001.

[3] D.G. Pierce, Electrostatic Discharge Failure Mechanisms, ESD Tutorial Notes, ESD Association (1996)

[4] N. Jonassen,, Fundamentals of Electrostatics, ESD Tutorial Notes, ESD Association (1996).