Comparison of gettering capability of various extrinsic techniques and enhancement of gettering ability of polycrystalline silicon layers

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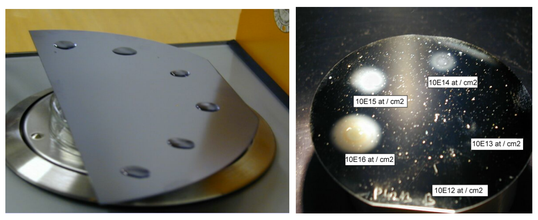
Abstract

The gettering capability of silicon wafers with various back side treatment was measured by the Method of Controlled Contamination (MCC) prior and after high temperature annealing. The MCC measurements on wafers with polycrystalline silicon layers (POLY) agree with the x-ray diffraction measurement. Wafer bowing as a function of annealing temperature is discussed in terms of layer-induced stress. We developed multilayer system (sandwich layers) consisting of a number of alternating polycrystalline silicon - silicon dioxide layers. Its ability of solving the undesirable loss of the gettering capability of polycrystalline silicon layers after high temperature annealing was demonstrated.

Experiment

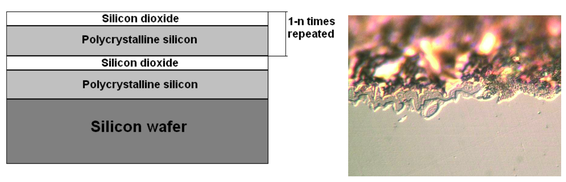
The samples were produced in ON Semiconductor Czech Republic. Silicon wafers were sliced from Czochouralski-grown ingot doped with Sb. Wafers parameters were: resistivity 10 - 20 mΩcm, orientation (100), thickness 525 μm, diameter 100 mm. Wafers back side was treated in three ways: (a) POLY deposition, (b) Back Side Damage (BSD), (c) deposition of sandwich layers. The layers were grown by the Low Pressure Chemical Vapor Deposition (LPCVD) technique with SiH_4 as the source gas. Thickness of the POLY and sandwich layers was 1.1 μm. BSD was made by blasting by SiO_2 particles. X-ray diffraction was measured on Masaryk Univerzity in Brno, Czech Republic.

Method of Controlled Contamination



The MCC method starts with intentional contamination of the wafer front side by droplets of $Ni(NO_3)_2$ solution. The droplets yield Ni surface contamination of 10e12 - 10e17 at / cm^2. After diffusion of Ni into the wafer (900 °C / 7 min) wafers are fast cooled to room temperature. Haze formed on the surface after selective etching is evaluated. The highest Ni concentration that was completely gettered by the wafer (i.e. forms no haze) is considered to be the wafer gettering capability.

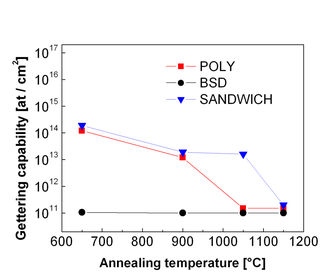
Sandwich layers

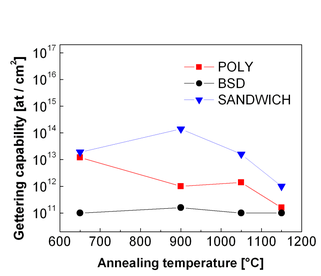


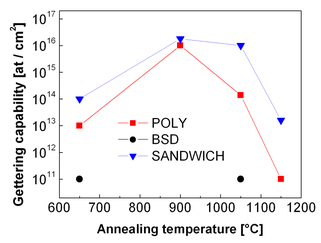
POLY layers enhance the gettering capability of a semiconductor wafer by about two orders of magnitude (measured by MCC) and it is efficient for gettering of heavy metals. However, after each high temperature annealing during the device fabrication process POLY layers losses a great part of its gettering capability.

By introducing several SiO_2 layers into the polycrystalline silicon the multilayer structure of polycrystalline silicon - SiO_2 layers (sandwich structure) is created. Number and thickness of the SiO_2 layers as well as polycrystalline silicon layers are critical in order to achieve good gettering properties and thermal stability of the whole multilayer structure. Utilization of the multilayer structure of polycrystalline silicon - SiO_2 for backside gettering is the subject of US Patent proceedings and it is proprietary of ON Semiconductor.

Gettering capability of Si wafers with various back side treatments

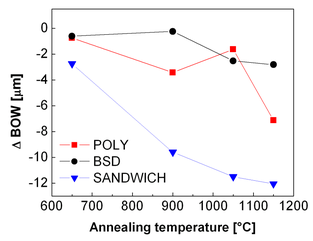


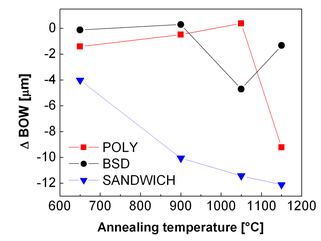




Gettering capability was measured by MCC after annealing at 650 °C, 900 °C, 1050 °C and 1150 °C for 0.5, 2 and 24 hours, respectively. In general, BSD shows the lowest gettering capability, POLY exhibits medium gettering capability and sandwich layers the best gettering capability. The temperature dependence of the gettering capability of the wafers with POLY or sandwich for 0.5 hour annealing is a decreasing function, which corresponds to the recrystallization phenomenon. With increasing annealing time the dependency turns into a single-peak function. We believe that the increase in gettering capability at 900 °C - 1050 °C is the consequence of the intrinsic gettering caused by oxygen precipitation. Layer deposition acts as the nucleation step and promotes oxygen precipitation. Wafers with BSD only do not experience any nucleation step and therefore do not exhibit the increase in gettering capability.

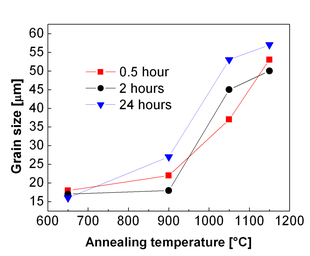
Bowing of Si wafers with various back side treatments

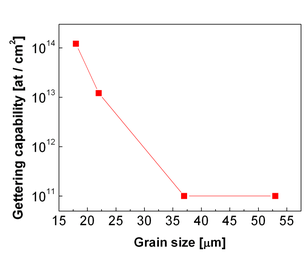




Changes in wafer bowing is the consequence of the stress induced by the back side treatment of the wafer. The stress induced by POLY layers decreases with increasing grain size and it is affected by the crystallographic orientation of the grains. Our results show that annealing at the temperatures of 650 °C and 900 °C does not cause significant changes in grain size while annealing at the temperature above 900 °C leads to POLY recrystallization, subsequent relaxation of the layers-induced stress and simultaneous decrease in wafer bowing. It is obvious that the stress relaxation in sandwich layers proceeds in a different way. It is a consequence of introduced SiO_2 layers.

Recrystallization of polycrystalline silicon layers





The x-ray measurement of the polycrystalline silicon grain size shows that the grain size increases with the annealing temperature. At the temperature of 900 °C the increment of the grain size is small, comparable with the measurement accuracy. We concluded that the annealing temperature above 900 °C is necessary for noticeable changes in the layer structure. By the measurement of the gettering capability as a function of annealing time we found that the gettering capability of POLY layers doesn't change at the annealing temperature of 650 °C, slightly decreases at the annealing temperature of 900 °C (but the decrement is comparable with the accuracy of the MCC method) and steeply fall at higher annealing temperatures. Both x-ray and MCC thus show that remarkable changes in the POLY layer proceed only at the temperature above 900 °C. This correlation, however, can be made only for the sample series annealed for 0.5 hour. For longer annealing time intrinsic gettering of the wafer overlaps the drop in the gettering capability of POLY. Combining x-ray and MCC results we constructed the dependence of the gettering capability of the POLY layer on the grain size, showing that the gettering capability significantly decreases with increasing grain size.

Conclusion

We introduced a newly developed technique of extrinsic gettering based on the multilayer structure (sandwich) of alternating POLY-SiO_2 layers. Its properties and thermal stability were compared to two various techniques of extrinsic gettering. BSD has the lowest gettering capability, POLY medium and sandwich layers have superior gettering capability. All studied techniques lose their gettering capability with increasing annealing temperature after annealing for 0.5 hour. The observed increase in the gettering capability at the annealing temperature around 1000 °C in samples annealed for 2 hours and 24 s is explained in terms of intrinsic gettering. The new sandwich structure shows higher thermal stability of the gettering capability compared to common POLY layer. Our data show that the grain size of the polycrystalline silicon increases with the annealing temperature and that the gettering capability of the POLY layer decreases with increasing grain size. We found out that annealing temperature above 900 °C is necessary for significant recrystallization of the polycrystalline silicon. We observed that the stress relaxation in sandwich layers proceeds differently from the POLY layers. It is a consequence of introduced silicon dioxide layers.

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