Top Cool Package for Power Discrete MOSFETs

AND90190/D

Introduction

In power applications, the majority of MOSFETs utilized tend to be surface mount devices (SMD). Some package examples include SO8FL, u8FL, and LFPAK. These SMDs are usually selected due to their power capabilities while maintaining a compact size. This in turn, allows for a more compact application solution. Although these devices have good power capabilities, the heat dissipation is not ideal because the heat propagation is mainly through the PCB. The heat flows through the board because the lead frame of the device, including the exposed drain pad, is soldered directly onto a copper footprint. The rest of the device is enclosed in mold compound and cooled only through air convection. The efficiency of heat transfer is then largely dependent on the board properties: Cu plane size, Cu layers, Cu weight, and Cu layout. This is the case regardless of the board being mounted to a heatsink or not. Due to this, the maximum power capability of the device is not optimal since PCBs don't generally have high thermal conductivity and thermal mass. To counter this issue and to improve on application size even further, a new MOSFET package has been developed which exposes the lead frame (drain) of the MOSFET on the top side of the package (e.g., Figure 1).

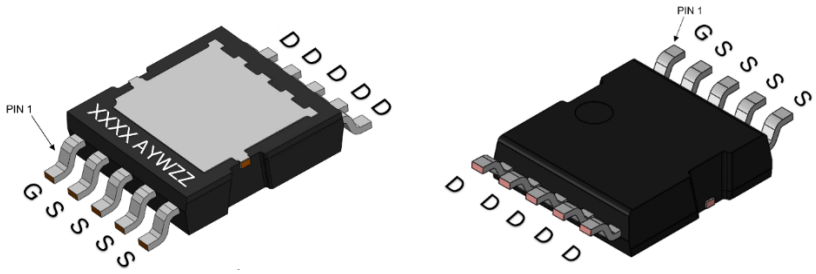

Figure 1. Top Cool Package

Top Cool Layout Benefits

Although traditional power SMDs yield small solutions, they have the need for the back of the board to remain unpopulated underneath them. This is for heatsinking reasons. Thus, some board space is unavailable and nets a larger overall board size. Top cool devices bypass this issue because the heatsinking occurs through the top of the device. This allows for board population underneath the MOSFETs. This space can be utilized for but not limited to, components such as:

- Power devices
- Gate drive circuitry
- Supporting components (capacitors, snubbers, etc)

This in turn can yield smaller board sizes, reduced path lengths for gat drive signals, and more desirable solution size.

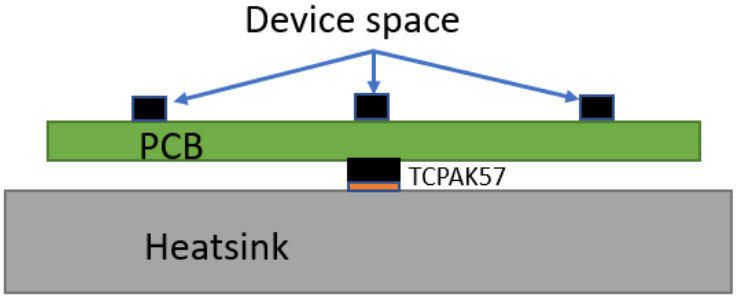

Figure 2. PCB Device Space

In addition to more population space, top cool devices cause less heat sharing than the standard SMD devices. Since most of the heat propagation for the top cool package goes directly into the heatsink, the PCB sustains less heating. This helps obtain lower operating temperatures for surrounding devices.

Top Cool Thermal Benefit

Unlike traditional surface mount MOSFETs, the top cool package allows for direct heatsinking to the lead frame of the device. Heatsink materials are usually metal due to their high thermal conductivity. For example, the majority of heatsinks are aluminum with a thermal conductivity between 100 – 210 W/mk. This sinking to a high thermal conductivity material greatly reduces the thermal resistance compared to the conventional heatsinking through a PCB. Thermal conductivity and material size are key constituents of thermal resistance. The lower the thermal resistance, the better the thermal response.

$R\theta$ = absolute thermal resistance
Δx = thickness of material parallel to heat flow
A = cross sectional area perpendicular to heat flow
k = thermal conductivity

In addition to improved thermal conductivity, heatsinks provide a much greater thermal mass which helps avoid saturation, or provide a longer thermal time constant. This is because the top mounted heatsink can be varied in size. Thermal mass or capacitance is proportional to the change in temperature given for a set amount of thermal energy input.

Cth = Thermal capacitance, J/K
Q = thermal energy, J
ΔT = Temperature change, K

PCBs tend to have varying layouts and low copper weight that leads to low thermal mass and results in poor heat propagation. All these factors lead to standard surface mount MOSFETs not being used with an optimal thermal response. In theory, given the benefit of being heatsinked directly to high thermal mass, high thermally conductive source, the top cool package will have a better thermal response (Zth (C/W)). The better thermal response allows for higher power input for a given junction temperature increase. This allows the same MOSFET die packaged in a top cool package to have higher current and power capability than the same die placed in a standard SMD package.

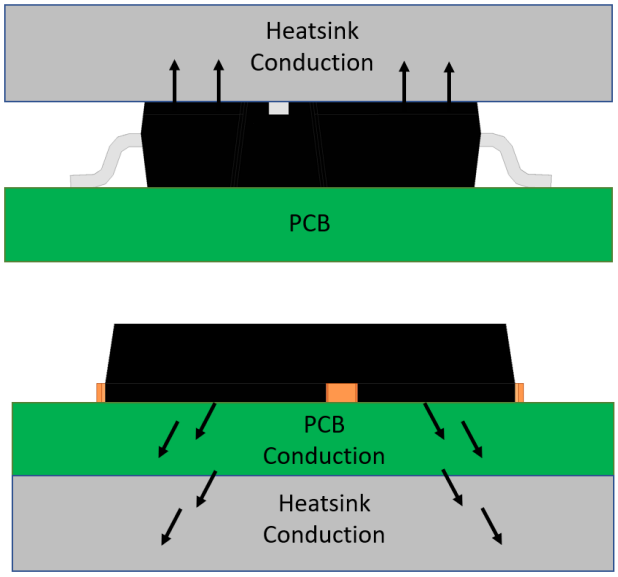

Figure 3. Heat Dissipation Paths for the Top Cool Package (top image) and the SO8FL Package (bottom image)

Thermal Performance Comparison Test Set−up

To demonstrate and validate the top cool thermal benefits, a test was performed comparing the die temperature rise and thermal response between a TCPAK57 and SO8FL device given equal thermal boundaries. To make this comparison valid, both devices were subjected to the same electrical conditions and thermal boundaries. The difference being that the TCPAK57 is mounted to a heatsink on the top side of the device while the SO8FL device heatsink is mounted to the bottom of the PCB, directly under the MOSFET area (Figure 3). This replicates how the devices would be used in field applications. Different thermal interface material (TIM) thicknesses will also be used during testing to validate which device package is able to be optimized using different thermal boundaries. The overall test will be done by applying a fixed current and therefore fixed power, to both devices and then monitoring the change in junction temperature to see which one performs better.

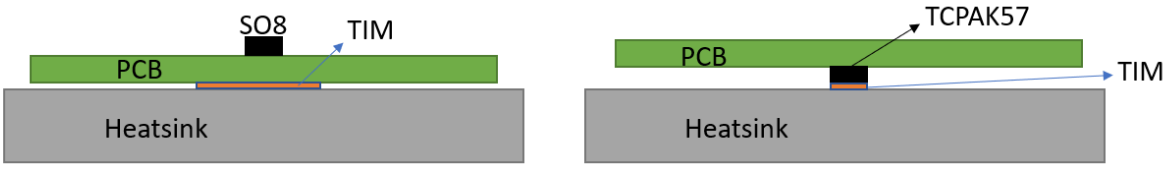

Figure 4. Application Set−up for each Device

Device Selection and PCB Layout

When it comes to device selection, a MOSFET from each package is used that shares the same die size and technology. This is to ensure that each device will share the same power dissipation for a given current and to align package level thermal response. This ensures that the thermal response differences collected, are known to be due to package differences. For these reasons, the TCPAK57 and SO8FL were selected. They utilize slightly different clip and lead frame designs because one is leaded (TCPAK57) and the other is leadless (SO8FL). It should be noted that these differences are minor and will not have a large impact on the steady state thermal response and can be omitted. Given the parameters, the devices selected are as follows:

- NVMFS5C410N SO8FL
- NVMJST0D9N04CTXG TCPAK57

To further ensure all other thermal boundaries remained equivalent, two identical PCBs were designed having either a SO8FL footprint or TCPAK57 footprint. The PCB was designed as a 4−layer board, containing 1 ounce copper for each layer. The dimensions are 122 mm x 87 mm. The SO8FL board has no thermal vias attaching the drain pad to other conductive layers of the board. This is not optimal in terms of heat dissipation and may serve as a worst−case scenario given this set−up comparison.

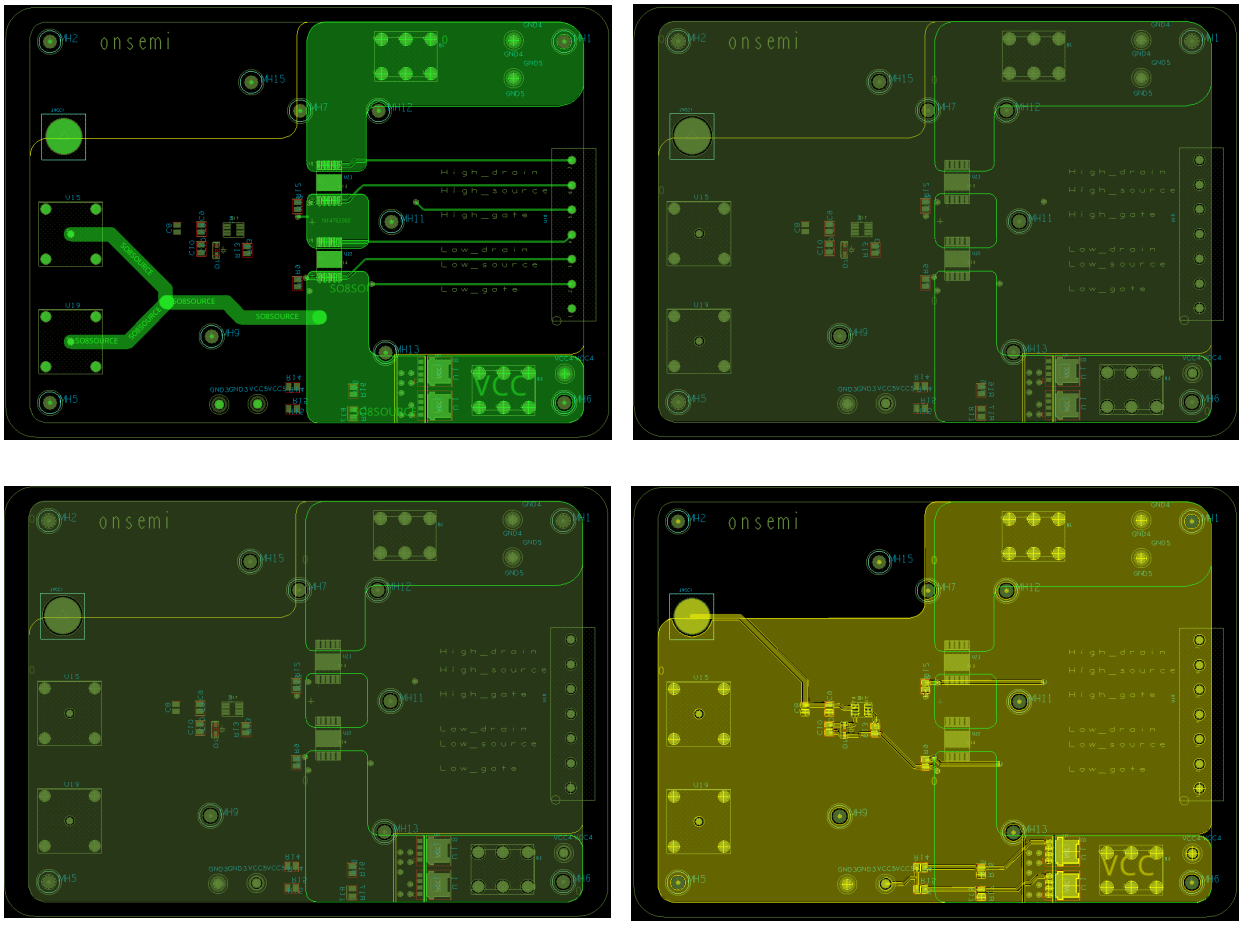

Figure 5. Each Layer of the PCB (1st layer is shown on the top left, 2nd layer on the top right, 3rd layer on the bottom left, and the 4th layer on the bottom right).

Heatsink and Thermal Interface Material (TIM)

The heatsink used during testing is aluminum and was specifically designed to mount to the PCBs. The 107 mm x 144 mm heatsink is liquid cooled with a 35 mm x 38 mm cooling area placed right under the MOSFET location. The liquid passed through the heatsink is water. Water is used as a generic representation of a cooling fluid that would be used in field applications. It is set at a fixed flow rate of 0.5 gpm for all test scenarios. This water acts as additional thermal mass and transfers heat from the heatsink into the water supply, helping lower the device temperature.

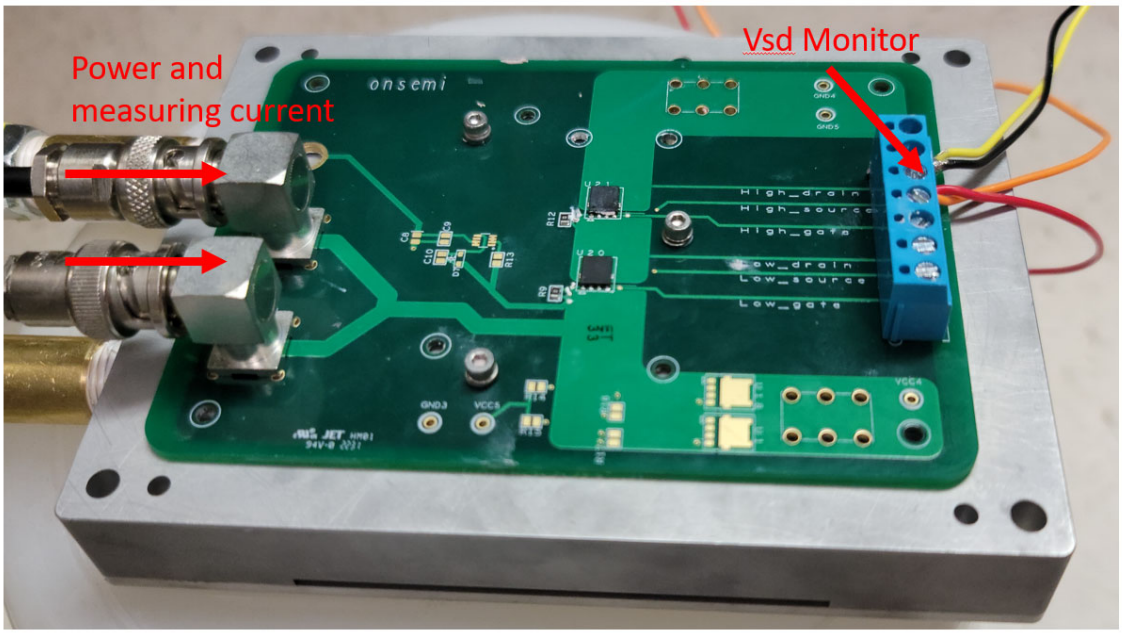

Figure 6. Application Set−up

To better facilitate the MOSFET to sink interface, a thermal gap filler is used. This helps fill in possible imperfection in the interface surfaces. Any air gaps yield increased thermal resistance since air is a poor thermal conductor. The TIM being used is Bergquist 4500CVO gap filler that has a thermal conductivity of 4.5 W/mK. This TIM will be used with a few different thicknesses to demonstrate the possibility of thermal response optimization. The fixed thicknesses are achieved by using precision shims between the board and the heatsink. The targeted thicknesses used are:

- ~200 μm
- ~700 μm

Test Circuit and Heating/Measuring Method

The on−board circuit configuration chosen was a half bridge set−up. This was chosen because it represents a generic field application. Both devices are in proximity of each other. This is also accurate to how field layouts are since shorter traces help reduce parasitic properties. This can play a role in the thermal response due to shared heating from device to device.

To allow for relevant heating with lower current values, the MOSFETs will used by passing current through the body diodes. To ensure this is the case at all times, the gate to source pins are shorted. The thermal responses will be obtained for a given device by heating the half−bridge FETs until a steady state junction temperature is achieved (no longer increasing in temperature) and then monitoring the source to drain voltage (Vsd) via a small 10 mA source as the junction temperature returns to cooled conditions. The time required to reach steady state during heating and the time to return to none powered conditions are equivalent. Since the Vsd of the body diode has a linear relationship with junction temperature, it can be correlated to a ΔTj by using a constant (mV/C) ratio determined through characterization for each device. The ΔTj throughout the cool down period is then used to characterize a thermal response of the given system (Zth) by dividing it by the power dissipation at the end of the heating period.

$$\Delta Tj = \frac{Vsd_{Cooled} - Vsd_{@GivenTime}}{Constant\ (mV/W)}$$

$$Zth = \Delta Tj \,/\, Pd_{@end\ of\ 2\ A\ pulse}$$

The 2 A supply, the 10 mA supply, and the measuring of Vsd are all handle by a T3ster. The T3ster is a commercial piece of test equipment specifically made to monitor thermal response. It calculates it with the previously mentioned methodologies.

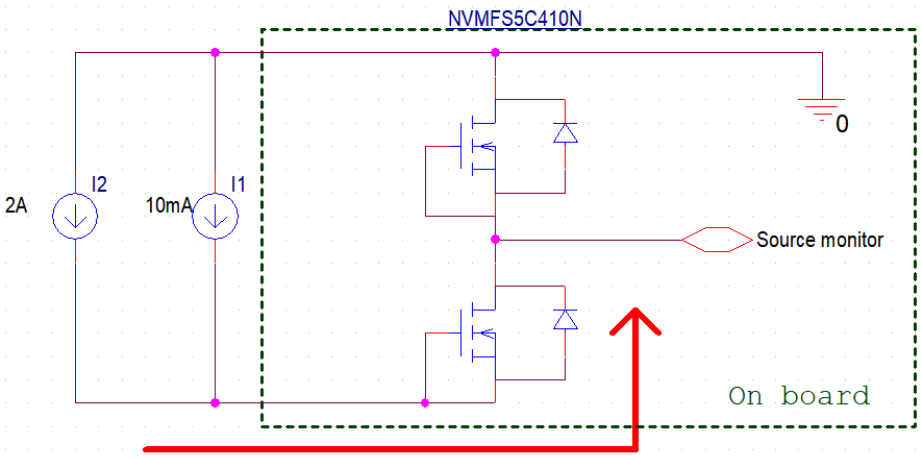

Figure 7. Circuit Diagram

Thermal Comparison Results

Thermal response results were collected under two conditions for each device:

- 200 μm TIM
- 700 μm TIM

The objective for these two runs is to identify which package has the better thermal response given a controlled system and which device's thermal response can be optimized using external cooling methods. It is important to note that these results are not translatable to all applications and are specific to the mentioned thermal boundaries.

Package Comparison Mounted to Sink with 200 μm TIM

For the first test, each device was mounted to the water cooled heatsink with a 200 μm TIM. Each device was subjected to a 2 A pulse until steady state was reached. The T3ster monitors Vsd during cool off and correlates it back to a thermal response curve for this system. The top cool shows a steady state thermal response of ~4.13 C/W compared to the SO8FL value of ~25.27 C/W. This large difference aligns with expected results given that the top cool is mounted directly to a high thermally conductive, large thermal mass heatsink which leads to good heat propagation. The SO8FL struggles with heat transfer due to the poor thermal conductivity of the PCB.

To help understand how these benefits can be used in application, the thermal response values can be correlated to the amount of power each device can withstand. This power required to raise Tj from 23C coolant to the max operating temperature of 175C is computed as:

TCPAK57 –

$$Pd = \frac{175 - 23}{4.13} = 36.8\ W$$

SO8FL –

$$Pd = \frac{175 - 23}{25.27} = 6.01\ W$$

NOTE: This power difference is expected in this particular thermal system.

In this thermal system, the top cool unit can handle 6 times the amount of power compared to the SO8FL. In a field application, this can be capitalized on a few different ways. Some benefits are:

- For a set amount of demanded current, a smaller top cool device can be used compared to an SO8FL due to the increase in power capability. In turn, this can possibly generate cost savings.
- For switched mode power supply applications, switching frequency can be increased while maintaining comparable thermal margins
- Can be used in higher power application that may have not been originally suitable for an SO8FL.
- For a given die size, the top cool device will have a higher margin of safety compared to the SO8FL by running cooler for a given current need.

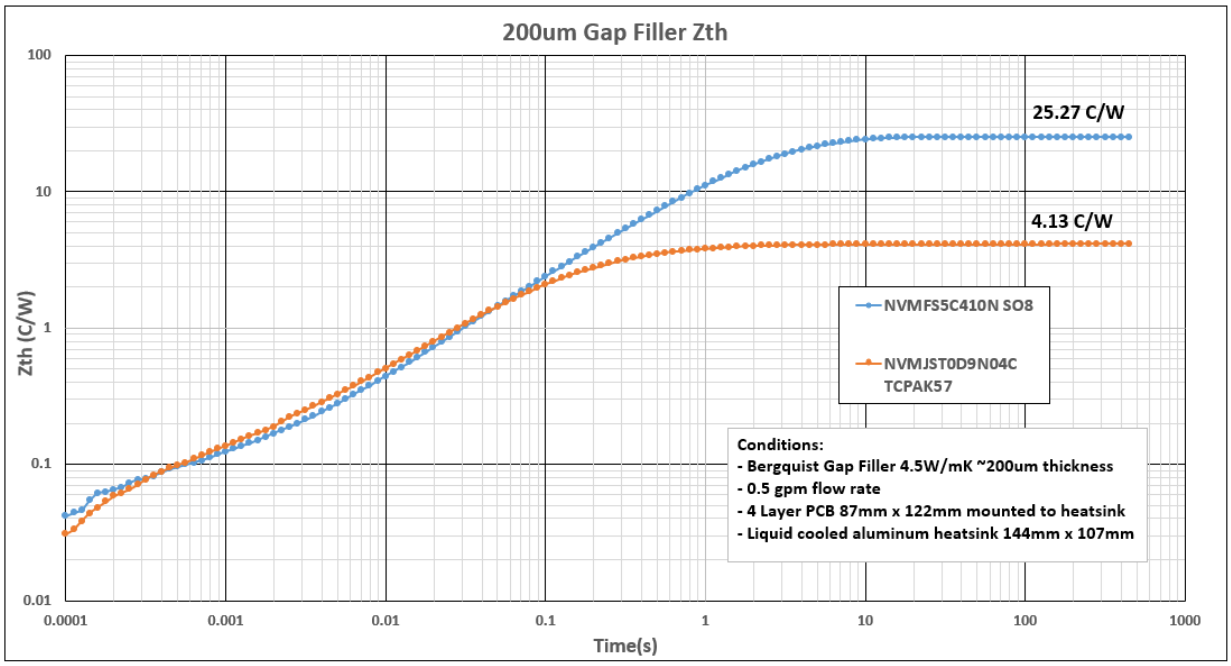

Figure 8. Thermal Response Curves using 200 μm TIM

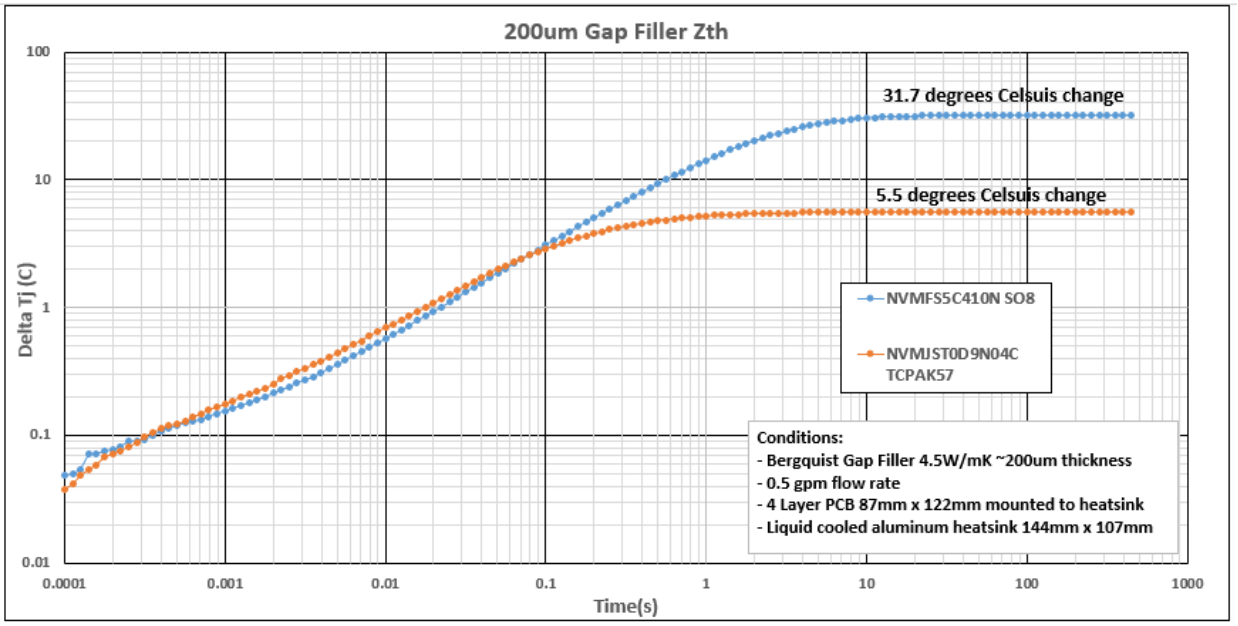

Figure 9. Change in Temperature Curve using 200 μm TIM

Package Comparison Mounted to Sink with 700 μm TIM

Another test run was done using a TIM thickness of 700 μm. This is done to validate the effects the external cooling methods have on each package by comparing the change thermal responses to the 200 μm TIM test run. The test run yielded a thermal response of 6.51 C/W for the top cool device and 25.57 C/W for the SO8FL. A difference of 2.38 C/W between each TIM run was obtained for the top cool while the SO8FL had a difference of 0.3 C/W. This means that the given external cooling methods have a large effect on the top cool device while having a little effect on the SO8FL. This is also expected since the top cool device response is dominated by the TIM layer thermal resistance. The TIM has a lower thermal conductivity compared to the heatsink. So, when the thickness is increased, the thermal resistance increases and results in a higher Rth.

The S08FL TIM variation happens between the board and the heatsink. Since his devices heat must propagate through the board before reaching the TIM and heatsink, the thickness change does little to the primary heat paths thermal

resistance. Therefore, a small change occurred in the response.

These observed changes in their thermal responses due to the TIM thickness change demonstrates the overall advantage the top cool package has. The TCPAK57 having an exposed lead frame on the top of the package allows for better control over the heat paths thermal resistance. This can then be utilized to optimize a thermal response given a particular application and cooling method. This in turn yields more controllable and beneficial power capabilities. The SO8FL and similar SMD devices struggle to dissipate heat through the boards they are mounted to depending on PCB properties. This is something that is not easily manipulated since PCB designs have many variables to consider in design outside of heat dissipation.

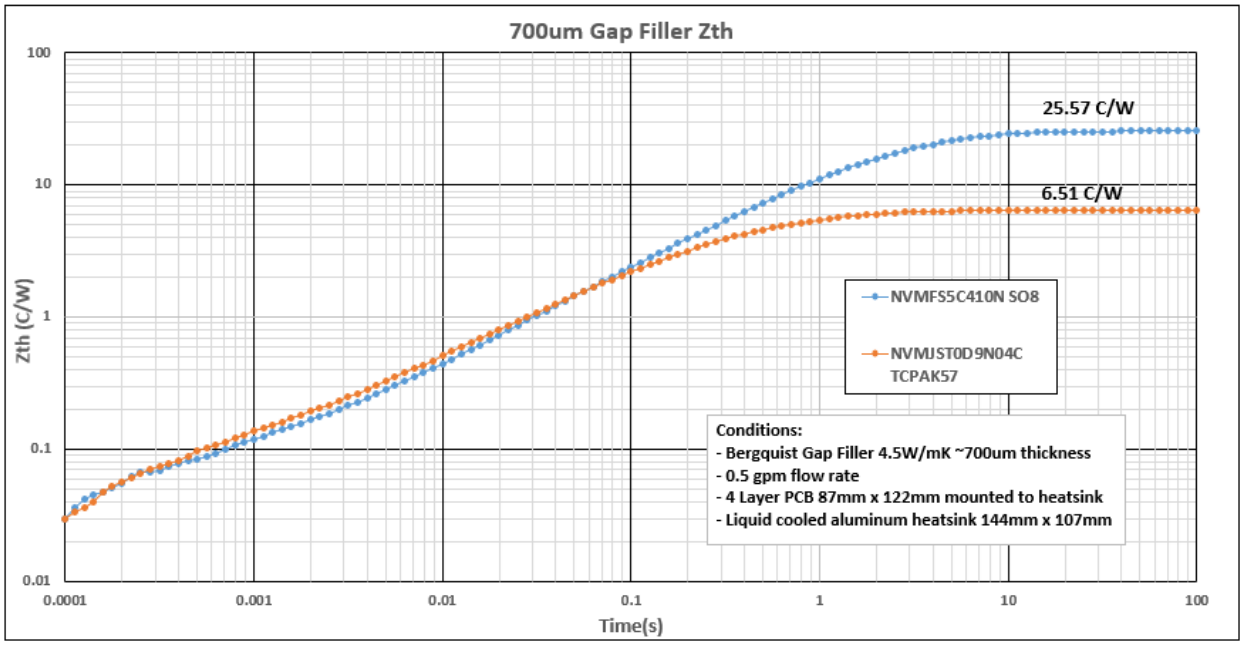

Figure 10. Change in Temperature Curve using 700 μm TIM

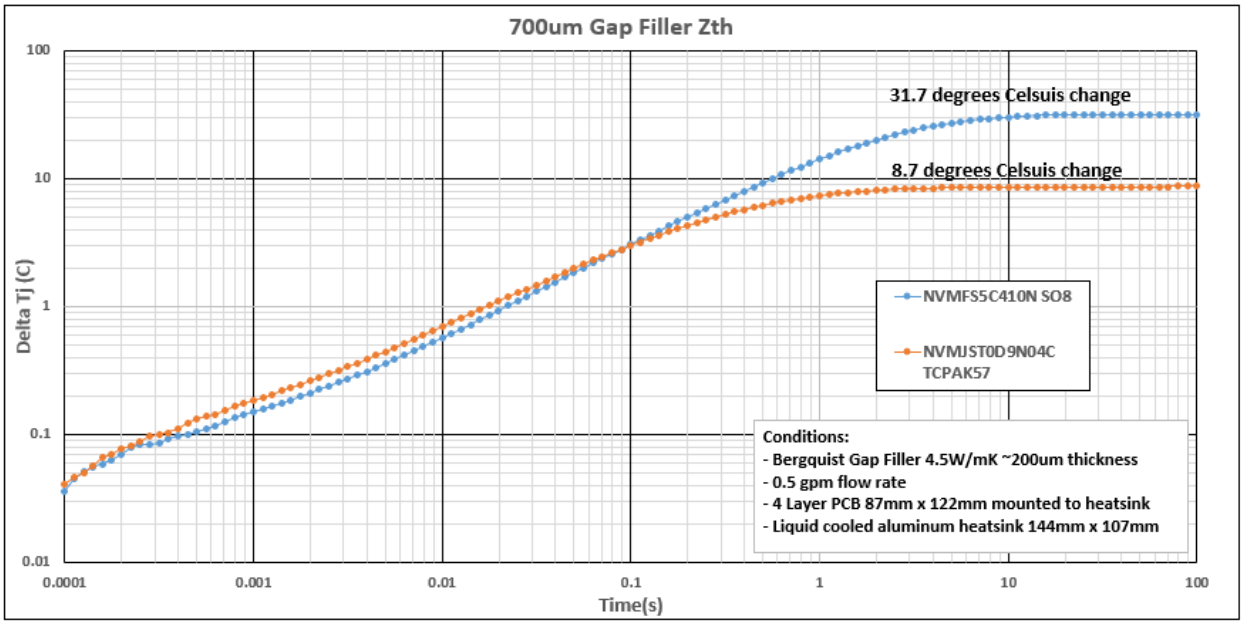

Figure 11. Change in Temperature Curve using 700 μm TIM

Key Takeaways

- The Top Cool package gives the ability to shorten the heat path from the die to the heatsinking method by avoiding cooling through the PCB. This reduces thermal resistance of the device. The thermal resistance becomes directly dependent on the heatsink and the thermal interface material properties. The possibility of reduced thermal impedance leads to application benefits such as:
  - For a set amount of demanded current, a smaller top cool device can be used compared to an standard SMD due to the increase in power capability. In turn, this can possibly generate cost savings.
  - For switched mode power supply applications, switching frequency can be increased while maintaining comparable thermal margins.
  - Can be used in higher power application that may have not been originally suitable for a standard SMD.
  - For a given die size, the top cool device will have a higher margin of safety compared to an SMD equivalent by running cooler for a given current need.
- Greater thermal response optimization ability. This is achieved by altering the thermal interface material and/or the thickness. The thinner the TIM and/or the better the thermal conductivity, the lower the thermal response will be. The thermal response can also be altered by changing the heatsink properties.
- Top Cool packages allow for less heat propagation through the PCB which in turn reduces heat sharing from device to device.
- Top side cooling gives the option for more condensed PCB population since the back of the PCB does not need to be attached to a heatsink.

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