AND9353/D

AX5031 Programming Manual

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APPLICATION NOTE

OVERVIEW

AX5031 is a true single chip low−power CMOS transmitter primarily for use in SRD bands. The on−chip transmitter consists of a fully integrated RF generation with modulator and power amplifier. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication via the SPI interface.

Connecting the AX5031 to a Micro−Controller

The AX5031 can easily be connected to any micro−controller. The micro−controller communicates with the AX5031 via a register file that is implemented in the AX5031 and that can be accessed serially via an industry standard Serial Peripheral Interface (SPI) protocol.

Reset can be performed via the register file. Therefore, and due to an integrated power−on−reset (POR) block there is no dedicated reset pin.

The AX5031 sends data via the SPI port in frames. This standard operation mode is called frame mode.

In frame mode, the internal communication controller performs frame delimiting, and data is transmitted via a 32 level x 10 bit FIFO, accessible via the register file. Figure 1 shows the corresponding diagram. Connecting the interrupt line is highly recommended, though not strictly required.

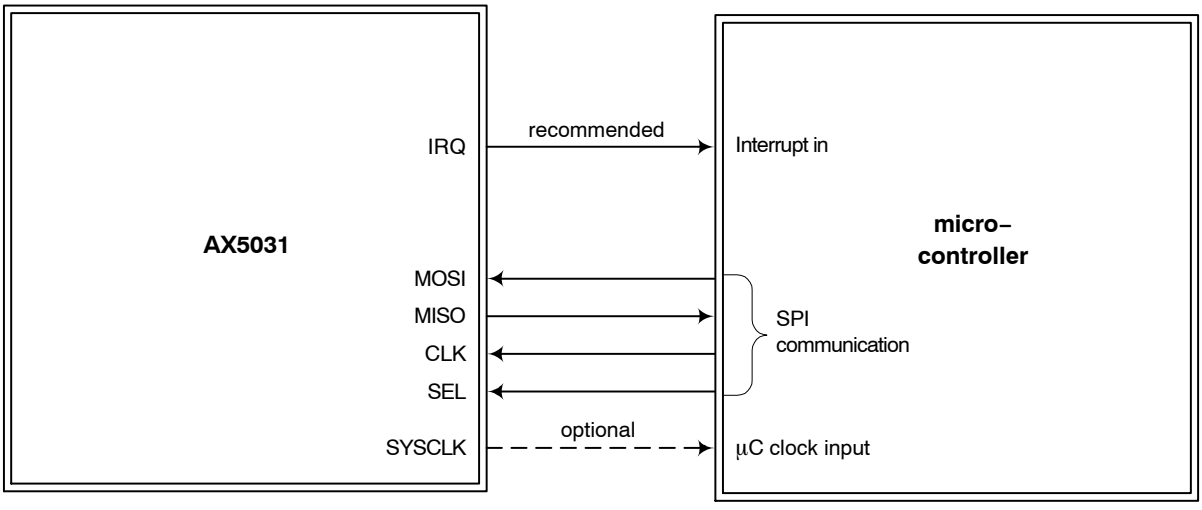

Figure 1. Connection Diagram with a Micro−Controller

Pin Function Descriptions

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
VDD	1	P	Power supply, must be supplied with regulated voltage VREG
ANTP	2	A	Antenna output
ANTN	3	A	Antenna output
VDD	4	P	Power supply, must be supplied with regulated voltage VREG
NC	5	N	
NC	6	N	
SYSCLK	7	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin.
SEL	8	I	Serial peripheral interface select
CLK	9	I	Serial peripheral interface clock
MISO	10	O	Serial peripheral interface data output
NC	11	N	
MOSI	12	I	Serial peripheral interface data input
NC	13	N	
IRQ	14	I/O	Default functionality: Interrupt Can be programmed to be used as a general purpose I/O pin.
VDD_IO	15	P	Unregulated power supply
NC	16	N	
VREG	17	P	Regulated output voltage VDD pins must be connected to this supply voltage. A 1 μF low ESR capacitor to GND must be connected to this pin.
VDD	18	P	Power supply, must be supplied with regulated voltage VREG
CLK16P	19	A	Crystal oscillator input/output
CLK16N	20	A	Crystal oscillator input/output
GND	Center pad	P	Ground on center pad of QFN

A = analog input
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 5 V tolerant.

SPI Register Access

Registers are accessed via a synchronous Serial Peripheral Interface (SPI). Most registers are 8 bit wide and accessed using the waveforms detailed in Figure 2. These waveforms are compatible to most hardware SPI master controllers, and can easily be generated in software. MISO changes on the falling edge of CLK, while MOSI is latched on the rising edge of CLK.

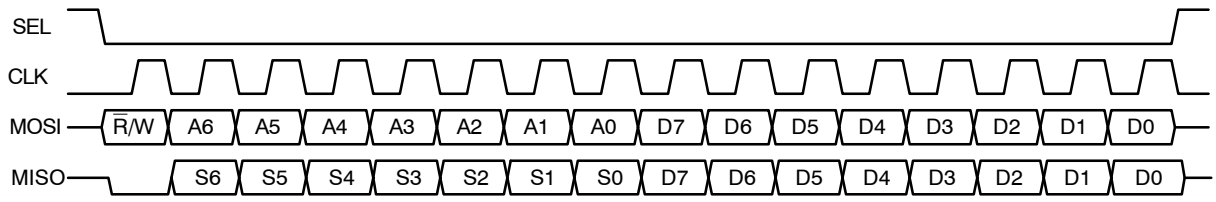

Figure 2. SPI 8 Bit Read/Write Access

It is necessary to deactivate and reactivate SEL between register accesses. Some registers perform preparatory actions on the falling edge of SEL and perform cleanup actions on the rising edge of SEL, so if SEL is left active between register accesses, some registers may fail.

Status Bits

During the address phase of the access, the chip outputs the most important status bits. This feature is designed to speed up software decision on what to do in an interrupt handler. Table 2 shows which register bit is transmitted during the status timeslots.

Table 2. SPI STATUS BITS

SPI Bit Cell	Status	Register Bit
0	–	0
1	S6	PLL LOCK
2	S5	FIFO OVER
3	S4	FIFO UNDER
4	S3	FIFO FULL
5	S2	FIFO EMPTY
6	S1	FIFOSTAT(1)
7	S0	FIFOSTAT(0)

For information on the meaning of the status bits see the Transmit section of the next chapter as well as the description of the register FIFOCTRL in the Register Description section.

PROGRAMMING THE CHIP

The operation sequences of the chip are controlled using the PWRMODE register.

Table 3. PWRMODE REGISTER STATES

PWRMODE Register	Name	Description	Typical Idd
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltage is reduced to conserve leakage power. SPI registers are still accessible, but at a slower speed. FIFO access is possible.	0.25 μA
0100	VREGON	All digital and analog functions, except the register file, are disabled. The core voltage, however is at its nominal value for operation, and all SPI registers are accessible at the maximum speed.	140 μA
0101	STANDBY	The crystal oscillator is powered on; the transmitter is off.	500 μA
1100	SYNTHTX	The synthesizer is running on the transmit frequency. The transmitter is still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.	10 mA
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.	11 – 45 mA

Figure 3 shows the basic programming flow chart of the device for transmitting.

1. Power up references and oscillators:
   Set PWRMODE to STANDBY
   First, the on−chip references and the crystal oscillator are powered up, but the synthesizer is still powered down. Settling time of this phase is dominated by the crystal oscillator start−up time, which depends on the specific crystal used but is typically 3 ms.
2. Program parameters
   Then the desired modulation, carrier frequency and encoding is set (see section “Parameter Programming”). This can be done while the crystal oscillator is settling.
3. Power up synthesizer: Set PWRMODE to SYNTHTX
   After all the modulation parameters are set, the synthesizer can be powered up. The settling time of the synthesizer is 5 – 50 μs depending on settings (see section AC Characteristics in the AX5031 Datasheet)
4. Auto−ranging
   After powering up, the VCO in the synthesizer needs to be auto−ranged to the correct range setting. This is done using the auto−ranging procedure, for details see section: Synthesizer VCO Auto−Ranging. The auto−ranging needs to be performed, if it has not been done in a previous TX session, if the temperature or VDD have changed or if the frequency has changed.
5. Start transmitter: Set PWRMODE to FULLTX
6. Power down: Set PWRMODE to POWERDOWN
   When transmission is finished, the chip can be powered down.

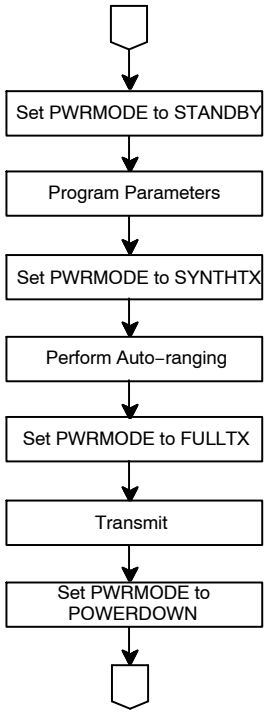

Figure 3. Transmit Flow Chart

The register contents are preserved as long as the chip is powered, therefore, registers that do not change between different transmit cycles do not need to be reprogrammed.

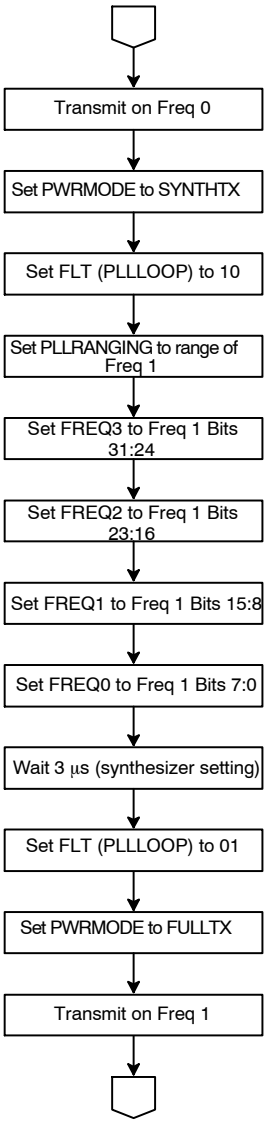

Figure 4. Transmit Frequency Change Flow Chart

In Frequency Hopping systems, it is important to perform fast frequency changes. Figure 4 shows the recommended frequency change flow chart for frequency hopping transmitters.

This flow chart details the recommended sequence to change the transmit frequency. It does not detail the synchronization necessary to keep transmitter and receiver hopping schedules synchronous.

It is assumed that auto−ranging has been performed offline for all frequencies of the hopping schedule, and the auto−ranging results (VCOR bits of register REGPLLRANGING) have been stored in the micro−controller.

The transmitter must be disabled before starting the frequency change and must only be re−enabled once the synthesizer has settled on the new frequency, in order to avoid spurious transmissions.

Parameter Programming

Choosing the Fundamental Communication Characteristics

Table 4 lists the fundamental communication characteristics that need to be chosen before the device can be programmed.

Table 5 gives an overview of the trade−offs between the different modulations that AX5031 offers, they should be considered when making a choice.

Table 4. FUNDAMENTAL COMMUNICATION CHARACTERISTICS

Parameter	Description
f_{XTAL}	Frequency of the connected crystal in Hz
modulation	FSK, MSK, ASK, PSK or OQPSK (for recommendations see Table 5: Modulation Trade−offs)
$f_{CARRIER}$	Carrier frequency (i.e. center frequency of the signal) in Hz
BITRATE	Desired bit rate in bit/s
h	Modulation index, determines the frequency deviation for FSK $32 > h \geq 0.5$ for FSK, $f_{deviation} = 0.5 * h *$ BITRATE h = 0.5 for MSK and OQPSK h = 0 for all other modulations
encoding	Inversion, differential, manchester, scrambled, for recommendations see the description of the register ENCODING and Table 13: Customary telecom modes description.

Table 5. MODULATION TRADE−OFFS

Modulation	Trade−offs
ASK	For bit rates up to 2000 kbit/s The sensitivity for equivalent peak output power is 3 dB lower than for other modulation types, as the average transmit power is only half the maximum transmit power. It is recommended to use shaped ASK for data transmissions, as the spectral efficiency is greatly improved vs. non−shaped ASK.
FSK	For bit rates up to 350 kbit/s Frequency deviation is a free parameter
MSK	For bit rates up to 350 kbit/s Robust and spectrally efficient form of FSK (Modulation is the same as FSK with h=0.5) Frequency deviation given by bit rate The advantage of MSK over FSK is that it can be demodulated with higher sensitivity. Slightly longer pre−ambles required than for FSK.
PSK	For bit rates up to 2000 kbit/s Slightly longer pre−ambles required than for FSK. It is recommended to use shaped PSK for data transmissions, as the spectral efficiency is greatly improved vs. non−shaped PSK.
OQPSK	For bit rates up to 350 kbit/s Very similar to MSK, with added precoding / postdecoding For new designs, use MSK instead

Setting−up the Chip

The AX5031 should be programmed according to the following guide−line, for more detailed recommendations and descriptions see the corresponding register descriptions in the section Register Bank Description:

1. Program the PLLLOOP register
   Bits FLT and PLLCPI must be set to program the synthesizer loop bandwidth. Recommended settings are given in Table 6. Bit BANDSEL is programmed to select the appropriate frequency band for $f_{carrier}$, set to 0 for 868/915 MHz band, set to 1 for 433 MHz band.

Table 6. RECOMMENDED SYNTHESIZER LOOP BANDWIDTH SETTINGS

Register Settings		Characteristics		
FLT	PLLCPI	Loop Band−width	Start−up Time	Usage
01	010	100 kHz	25 μs	Recommended setting for all modulations, all values of BITRATE Mandatory for FSK, MSK, OQPSK with BITRATE > 50 kHz
01	001	50 kHz	50 μs	Use if phase noise between 300 kHz and 1 MHz from carrier is critical Cannot be used for FSK, MSK, OQPSK with BITRATE > 50 kHz
11	010	200 kHz	12 μs	Use to speed up start−up or switching Do not use for TX
10	010	500 kHz	5 μs	Use to speed up start−up or switching Do not use for TX

2. Program the frequency registers FREQ3, FREQ2, FREQ1 and FREQ0 or FREQB3, FREQB2, FREQB1 and FREQB0.
   $FREQ = [\ f_{CARRIER}/f_{XTAL} \cdot 2^{24} + ½\ ]$
   Set bit FREQSEL in register PLLLOOP to 1 to use registers FREQB3, FREQB2, FREQB1 and FREQB0**,** set it to 0 if using FREQ3, FREQ2, FREQ1 and FREQ0.
   Ensure the bit 0 of FREQ0 or FREQB0 is set to one; this ensures that the built−in ΣΔ modulator does not exhibit tonal behaviour.
   NOTE: [x] denotes the floor function of the real number x. It returns the highest integer less than or equal x.
   Note that to program frequencies in the 433 MHz band registers FREQ3, FRE2, FREQ1 and FREQ0 must be programmed to appropriate values and the bit BANDSEL in the PLLLOOP register must be set to 1.
3. Program the TXPWR register according to the desired output power
4. Program the frequency deviation registers FSKDEV2, FSKDEV1 and FSKDEV0;
   $f_{DEVIATION} = h/2 \cdot BITRATE$
   $FSKDEV = [\ f_{DEVIATION}/f_{XTAL} \cdot 2^{24} + ½\ ]$

5. Program the transmit bit−rate registers TXRATEHI, TXRATEMID and TXRATELO; TXRATE = [BITRATE/f_{XTAL} · 2^{24} + ½]
6. Program the MODULATION register. See Table 12 for coding details.
7. Program the ENCODING register according to the desired bit encoding
8. Program the FRAMING register according to the desired framing mode
9. Program the PINCFG1, PINCFG2, PINCFG3 according to the desired pin usage

Synthesizer VCO Auto−Ranging

Whenever the frequency or the environment (e.g. temperature, voltage) of the chip changes, the synthesizer VCO should be set to the correct range using the built−in auto−ranging. A re−ranging of the VCO is required if the frequency change required is larger than 5 MHz in the 868/915 MHz band or 2.5 MHz in the 433 MHz band.

Figure 5 shows the flow chart of the auto−ranging process.

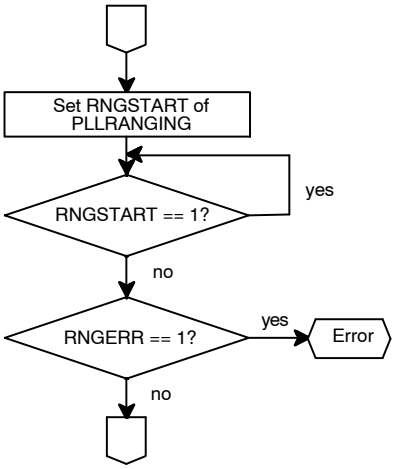

Figure 5. Synthesizer VCO Auto−Ranging Flow Chart

Before starting the auto−ranging, the frequency registers (FREQ3, FREQ2, FREQ1 and FREQ0 or FREQB3, FREQB2, FREQB1 and FREQB0) need to be programmed, and the chip should be in SYNTHTX mode.

Auto−ranging starts at the VCOR (register PLLRANGING) setting; if you already know the approximately correct synthesizer VCO range, you should set VCOR to this value prior to starting auto−ranging; this can speed up the ranging process considerably. If you have no prior knowledge about the correct range, set VCOR to 8. Starting with VCOR < 6 should be avoided, as the initial synthesizer frequency can exceed the maximum frequency specification.

Hardware clears the RNG START bit automatically as soon as the ranging is finished; the device may be programmed to deliver an interrupt on resetting of the RNG START bit.

Transmit

During transmit, the software communicates with the transmitter through a 10 bit wide and 32 levels deep FIFO. Figure 6 shows the FIFO write process.

FIFO full, empty, overrun and underrun flags are also transmitted during the status phase of SPI transfers. See section 1.3 SPI Register Access and Table 1: SPI Status bits for details. FIFO flags may also be used to generate interrupts. The AX5031 also features an arbitrary FIFO level threshold interrupt.

The AX5031 can also be programmed to automatically stop the transmitter on FIFO underrun.

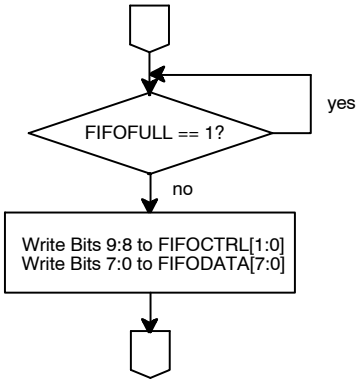

Figure 6. Write FIFO Flow Chart

Bits [7:0] are data information. During a write access to the FIFO, Bits 9 and 8 hold the FIFOCMD[1:0] bits of the FIFOCTRL register. The function of these bits depends on the framing mode (for more information see following sections). The device offers two different framing modes, namely HDLC and 802.15.4 (ZigBee). Additionally, Raw Mode allows the implementation of legacy protocols in software. FIFO operation differs slightly depending on the framing mode.

Write Access:

Bits 9 and 8 hold the bits FIFOCMD[1:0] of the FIFOCTRL register during a write access to the FIFO.

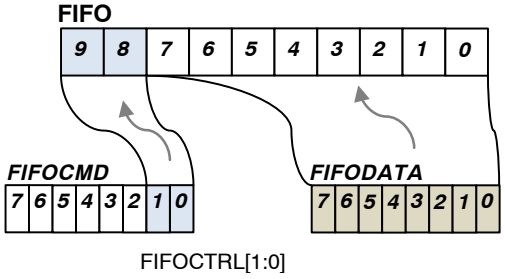

Figure 7.

HDLC

In HDLC mode, frames start and end with the bit pattern 01111110.

HDLC uses bit−stuffing: In order to ensure that no bit pattern inside the frame can be erroneously detected as a

frame end, the transmitter inserts a 0 bit after five consecutive one bits.

At the end of a HDLC frame, a checksum is transmitted. Seven or more consecutive one bits are treated as an ABORT, causing the current packet to be discarded. See [4] for a more elaborate description of HDLC.

In HDLC mode the meaning of the additional 2 bits in the 10 bit FIFO describe the content of FIFODATA[7:0]:

Table 7. HDLC MODE BITS

Bit [9:8]	Transmit FIFOCTRL[1:0]
00	Data Byte (bit stuffed)
01	CRC Byte
10	Not used
11	RAW Byte (not bit−stuffing, CRC is initialized) Used for flags (e.g. EOF)

In transmit the bits [9:8] describe the type of data in the FIFODATA[7:0] to be transmitted. This controls the internal framing block and enables or disables bit stuffing for data or flags, respectively. It also initiates CRC calculation. However the flag content and the CRC bytes have to be written by the host processor according to the sequence shown in Figure 9. The number of CRC bytes has to be chosen according to the type of CRC chosen in the FRAMING register (16 bit or 32 bit). For CRC insertion it does not matter what is written in the CRC bytes, as the chip will calculate the CRC value and will change the values.

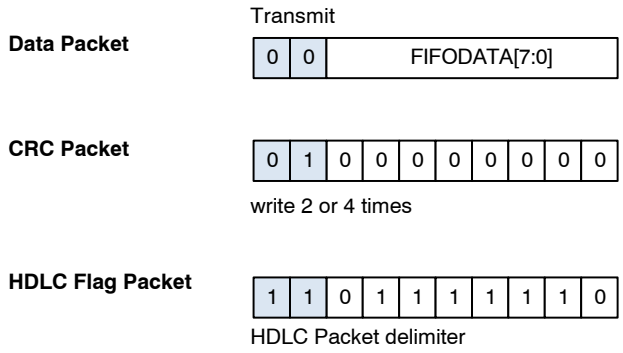

Figure 8.

Figure 9 shows the HDLC transmit process.

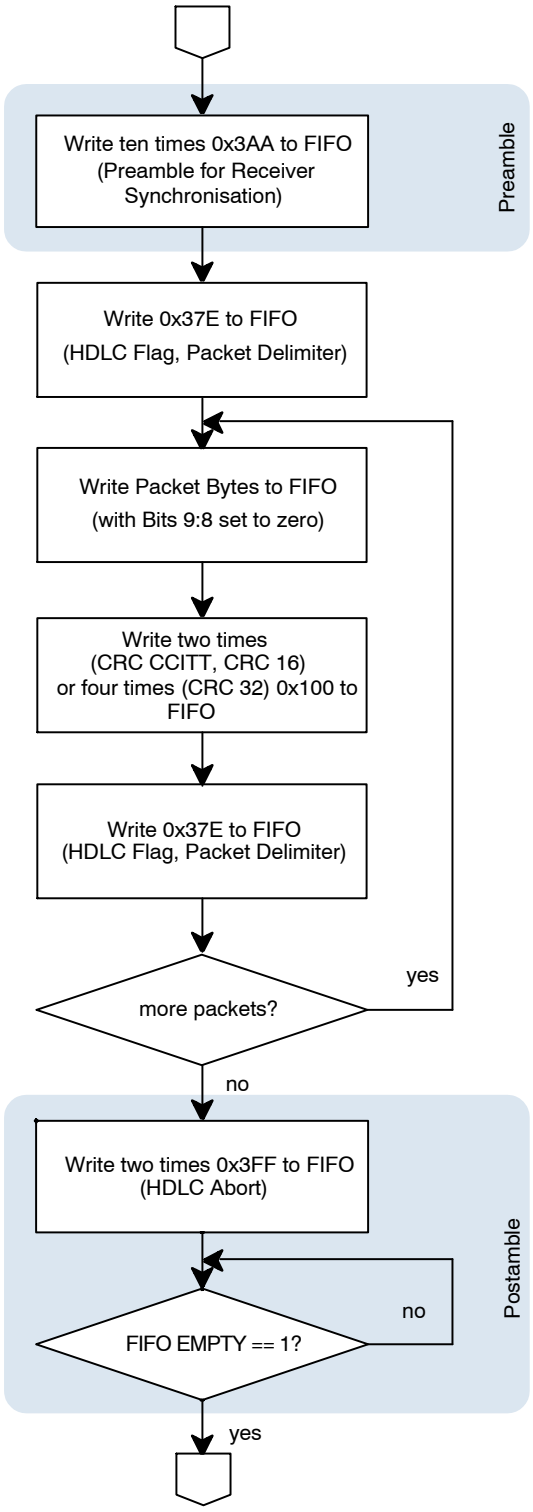

Figure 9. HDLC Transmit Flow Chart

802.15.4 (ZigBee)

Transmitter operation differs slightly in 802.15.4 mode versus HDLC mode, due to 802.15.4 not having a PHY CRC, and 802.15.4 determining packet length from the first byte transmitted. See [3] for a description of the 802.15.4 PHY.

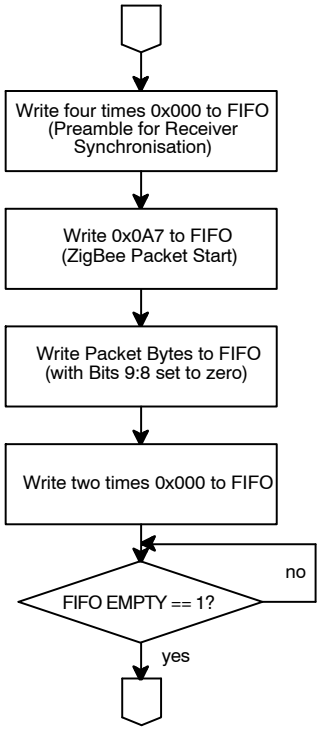

Figure 10. 802.15.4 Transmit Flow Chart

Figure 10 details the 802.15.4 transmit operation.

Raw Mode

In Raw Mode, no framing is performed. Transmit bits are retrieved from the FIFO as 8 bit bytes and then serialized. The bits are transmitted LSB first, that means that bit 0 will be transmitted first. No byte synchronisation is performed.

Raw mode is useful to implement legacy protocols in software on the micro−controller.

4−FSK Mode

The AX5031 also supports 4−FSK. In 4−FSK mode, four frequencies are used to transmit two bits simultaneously during each symbol. Table 8 shows the mapping from bits to frequencies. A gray code is used to minimize bit errors.

Table 8. 4−FSK BIT TO FREQUENCY MAPPING

M_x	L_x	Frequency
0	0	$f_C - 3 \cdot f_{DEVIATION}$
0	1	$f_C - f_{DEVIATION}$
1	1	$f_C + f_{DEVIATION}$
1	0	$f_C + 3 \cdot f_{DEVIATION}$

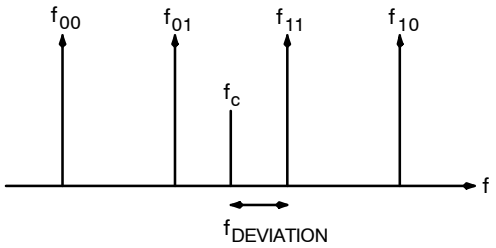

Figure 11. 4−FSK Frequency Diagram

Interrupts

The AX5031 supports interrupts for all non−immediate actions. Interrupts, while not strictly necessary, allow the micro−controller to perform other tasks instead of waiting for the AX5031.

The AX5031 supports level triggered interrupts.

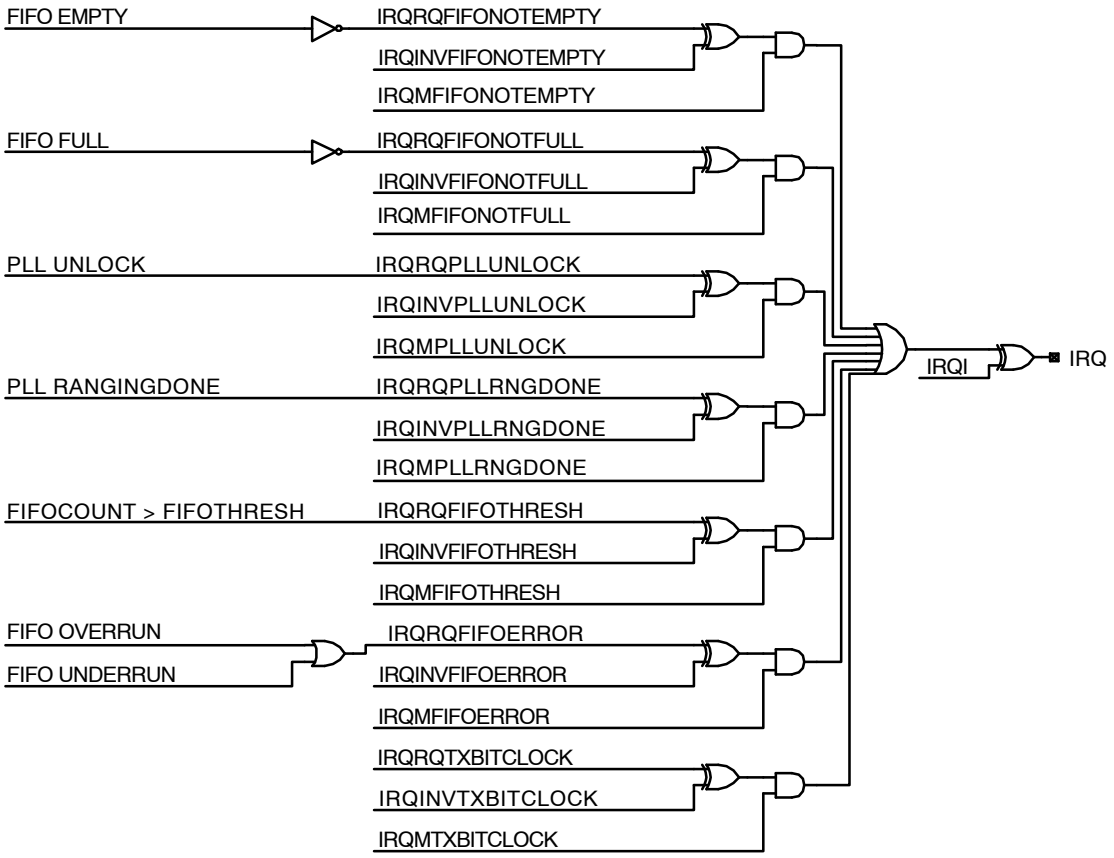

Figure 12. Interrupt Logic Diagram

Figure 12 shows the interrupt logic. The AX5031 supports 7 interrupt sources. Each source may be individually inverted and masked. The final interrupt pin may also be inverted, to support both level active high and level active low interrupts. Table 9 lists all interrupt sources, and how they can be cleared.

Registers used for interrupt configuration programming are IRQMASK, IRKREQUEST and IRKINVERSION.

Table 9. INTERRUPT SOURCES

Source	When Active	How to Clear
FIFO Not Full	The FIFO contains less than 32 words. At least one word can be written without causing an overrun	Write words into the FIFO until it is full. Be careful not to cause overruns.
FIFO Not Empty	The FIFO contains at least one word. At least one word can be transmitted without causing an underrun.	Wait until all words from the FIFO have been transmitted. Be careful not to cause underruns.
PLL Unlock	The PLL has lost lock	This interrupt can be cleared by reading the PLLRANGING register. After switching the synthesizer on, and after frequency changes, the synthesizer requires some time to settle on the correct frequency and to achieve phase lock with the reference crystal. After that, it should remain locked. The synthesizer losing lock after that point indicates a severe problem. Check the following: • Synthesizer programming (esp. frequency, loop filter settings, charge pump settings, VCO settings) are correct • Synthesizer has been auto−ranged (calibrated) properly • VDD is within spec and not too noisy • Temperature is within spec • Synthesizer is enabled
PLL Ranging Done	The synthesizer has finished auto−ranging its VCO	PLL Ranging Done can be cleared only by restarting a new auto−ranging process. If no more ranging processes are needed, mask the interrupt.

Table 9. INTERRUPT SOURCES

Source	When Active	How to Clear
FIFO Threshold	The FIFO contains more words than FIFOTHRESH, i.e. FIFOCOUNT > FIFOTHRESH	This interrupt can be cleared by writing words into the FIFO until FIFOCOUNT > FIFOTHRESH, or by writing a value greater than or equal to FIFOCOUNT into the FIFOTHRESH register.
FIFO Error	A FIFO overrun or underrun has occurred	This interrupt is cleared as soon as the FIFO OVER and FIFO UNDER bits in the FIFOCTRL register are cleared, i.e. by reading the FIFOCTRL register.
TX Bitclock	Transmit bit clock is high	This interrupt is cleared by doing one of the following: • Wait half the bit time • Mask the interrupt

Edge triggered interrupts are not directly supported. In the unlikely event that the chosen micro−controller does not support level triggered interrupts and only supports edge triggered interrupts, they need to be emulated in software. The following C pseudo code illustrates how this can be done:

```
void interrupt_handler(void)
{
     acknowledge_interrupt();
     do {
     handle_interrupt();
     } while (IRQ);
}
```

The first line, acknowledge_interrupt(), acknowledges the interrupt in the interrupt controller of the micro−controller. How this is done is specific to the micro−controller in question, and may even be implicit. The following loop handles interrupts as long as the IRQ line is still active. It is important that the interrupt handler is not terminated before IRQ goes inactive, because otherwise no new edges will be produced by the AX5031, and the interrupt becomes stuck.

Interrupt Strategies

The AX5031 supports three interrupt strategies:

1. The default strategy is to assert IRQ as soon as there is one word empty space in the FIFO (transmit, using the FIFONOTFULL interrupt). The micro−controller is required to service the interrupt within 24 bit times (24/BITRATE) to prevent a FIFO overrun or underrun. The micro−controller will receive one interrupt per received FIFO word (message byte). This strategy is recommended for micro−controllers with low interrupt overhead (which is true for most micro−controllers).
2. The second strategy is to assert IRQ only when absolutely necessary, i.e. when the FIFO is empty (transmit, using the inverted FIFONOTEMPTY interrupt). The micro−controller will receive one interrupt every three FIFO words (message bytes). This strategy is useful for micro−controllers with a very high interrupt overhead. Care must be taken to avoid FIFO overruns and underruns.
3. The FIFOTHRESH interrupt allows an arbitrary trade−off between interrupt rate and interrupt service latency.

Preamble

At the beginning of a data transfer, a preamble must be transmitted, before the actual data can be transmitted. The preamble has many purposes:

- The preamble allows the power amplifier to ramp up to operational power levels. This is not an issue with the built−in amplifier of the AX5031, which is nearly instantaneous, but may be an issue if external amplifiers are used.
- The preamble allows the receiver to achieve lock
- The preamble allows the encoder (transmitter) and the decoder (receiver) to initialise

Choosing the Preamble Bit Pattern

In 802.15.4, the preamble bit pattern is specified by the standards committee. This specification, which is four bytes of 0x00, should be followed.

In all other modes, the preamble bit pattern as it enters the modulator should be chosen such that:

- It is DC−free, to ensure that frequency offset estimation works correctly
- It contains as many transitions as possible

Now the transmitter cannot directly control the modulator bits, only the bits that enter the encoder. Thus, the bytes transmitted during the preamble should be chosen according to the selected encoder mode:

Table 10. RECOMMENDED PREAMBLE VALUES

Encoder Settings	Preamble Byte
INV=X, DIFF=0, SCRAM=0, MANCH=0	0x55 or 0xAA
INV=0, DIFF=1, SCRAM=0, MANCH=0	0xFF
INV=1, DIFF=1, SCRAM=0, MANCH=0	0x00
INV=X, DIFF=X, SCRAM=1, MANCH=X	0x55 or 0xAA.
INV=X, DIFF=0, SCRAM=0, MANCH=1	0x00 or 0xFF
INV=0, DIFF=1, SCRAM=0, MANCH=1	0x00
INV=1, DIFF=1, SCRAM=0, MANCH=1	0xFF

Postamble

After the data is transmitted, the micro−controller must write two additional postamble bytes to the FIFO. These bytes are used to clear the transmit pipeline. Their contents do not matter; HDLC flags can be used in HDLC mode.

After these preamble bytes are written to the FIFO, the micro−controller must wait until the FIFO is fully drained (empty). Only then can the transmitter be turned off.

REGISTER BANK DESCRIPTION

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

NOTES: Whole registers or register bits marked as reserved should be kept at their default values. All addresses not documented here must not be accessed, neither in reading nor in writing.

Table 11. CONTROL REGISTER MAP

Addr	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
Revision & Interface Probing												
0	REVISION	R	00100001	SILICONREV(7:0)								Silicon Revision
1	SCRATCH	RW	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode												
2	PWRMODE	RW	011–0000	RST	REFEN	XOEN	–	PWRMODE(3:0)				Power Mode
Crystal Oscillator, Part 1												
3	XTALOSC	RW	––––0010	–	–	–	–	XTALOSCGM(3:0)				GM of Crystal Oscillator
FIFO, Part 1												
4	FIFOCTRL	RW	––––––11	FIFOSTAT(1:0)		FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOCMD(1:0)		FIFO Control
5	FIFODATA	RW	––––––––	FIFODATA(7:0)								FIFO Data
Interrupt Control												
6	IRQMASK	RW	–0000000	–	IRQMASK(6:0)							IRQ Mask
7	IRQREQUEST	R	––––––––	–	IRQREQUEST(6:0)							IRQ Request
Interface & Pin Control												
0C	PINCFG1	RW	00101000	–		IRQZ	–	SYSCLK(3:0)				Pin Configuration 1
0D	PINCFG2	RW	00000000	–		IRQE	–	–		IRQI	–	Pin Configuration 2
0E	PINCFG3	RW	0–––––––	reserved	–	–	SYSCLKR	–		IRQR	–	Pin Configuration 3
0F	IRQINVERSION	RW	–0000000	–	IRQINVERSION(6:0)							IRQ Inversion
Modulation & Framing												
10	MODULATION	RW	–0000010	–	MODULATION(6:0)							Modulation
11	ENCODING	RW	––-00010	–	–	–	ENC NOSYNC	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings
12	FRAMING	RW	–0000000	–	HSUPP	CRCMODE(1:0)		FRMMODE(2:0)			–	Framing settings
14	CRCINIT3	RW	11111111	CRCINIT(31:24)								CRC Initialization Data or Preamble
15	CRCINIT2	RW	11111111	CRCINIT(23:16)								CRC Initialization Data or Preamble
16	CRCINIT1	RW	11111111	CRCINIT(15:8)								CRC Initialization Data or Preamble
17	CRCINIT0	RW	11111111	CRCINIT(7:0)								CRC Initialization Data or Preamble
Voltage Regulator												
1B	VREG	R	––––––––	–	–	–	–	SSDS	SSREG	SDS	SREG	Voltage Regulator Status
Synthesizer												
1C	FREQB3	RW	00111001	FREQB(31:24)								Synthesizer Frequency
1D	FREQB2	RW	00110100	FREQB(23:16)								Synthesizer Frequency
1E	FREQB1	RW	11001100	FREQB(15:8)								Synthesizer Frequency
1F	FREQB0	RW	11001101	FREQB(7:0)								Synthesizer Frequency
20	FREQ3	RW	00111001	FREQ(31:24)								Synthesizer Frequency
21	FREQ2	RW	00110100	FREQ(23:16)								Synthesizer Frequency

Table 11. CONTROL REGISTER MAP

Addr	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
22	FREQ1	RW	11001100	FREQ(15:8)								Synthesizer Frequency
23	FREQ0	RW	11001101	FREQ(7:0)								Synthesizer Frequency
25	FSKDEV2	RW	00000010	FSKDEV(23:16)								FSK Frequency Deviation
26	FSKDEV1	RW	01100110	FSKDEV(15:8)								FSK Frequency Deviation
27	FSKDEV0	RW	01100110	FSKDEV(7:0)								FSK Frequency Deviation
2C	PLLLOOP	RW	00011101	FREQSEL	reserved	BANDSEL	PLLCPI(2:0)			FLT(1:0)		Synthesizer Loop Filter Settings
2D	PLLRANGING	RW	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCOR(3:0)				Synthesizer VCO Auto−Ranging
Transmitter												
30	TXPWR	RW	----1000	–	–	–	–	TXRNG(3:0)				Transmit Power
31	TXRATEHI	RW	00001001	TXRATE(23:16)								Transmitter Bitrate
32	TXRATEMID	RW	10011001	TXRATE(15:8)								Transmitter Bitrate
33	TXRATELO	RW	10011010	TXRATE(7:0)								Transmitter Bitrate
34	MODMISC	RW	------11	–	–	–	–	–	–	reserved	PTTLCK GATE	Misc RF Flags
FIFO, Part 2												
35	FIFOCOUNT	R	--000000	–	–	FIFOCOUNT(5:0)						FIFO Fill state
36	FIFOTHRESH	RW	--000000	–	–	FIFOTHRESH(5:0)						FIFO Threshold
37	FIFOCONTROL2	RW	0-----00	CLEAR	–	–	–	–	–	STOPONERR (1:0)		Additional FIFO control
Crystal Oscillator, Part 2												
4F	XTALCAP	RW	--000000	–	–	XTALCAP(5:0)						Crystal oscillator tuning capacitance
Transmitter, Part 2												
50	FOURFSK	RW	-------0	–	–	–	–	–	–	FOUR FSK ENA		Four FSK Control

Register Descriptions

REVISION

The register holds the revision index of the chip.

Table 12. REVISION

Name	Bits	R/W	Reset	Description
REVISION	7:0	R	00100001	Silicon Revision

SCRATCH

The SCRATCH register does not affect the function of the chip in any way. It is intended for the micro−controller to test communication to the AX5031.

Table 13. SCRATCH

Name	Bits	R/W	Reset	Description
SCRATCH	7:0	R	11000101	Scratch Register

PWRMODE

This register controls the powering and reset of the various blocks on the chip.

Table 14. PWRMODE

Name	Bits	R/W	Reset	Description
RST	7	RW	0	Reset; setting this bit to 1 resets the whole chip. This bit does not auto−reset − the chip remains in reset state until this bit is cleared.
REFEN	6	RW	1	Reference Enable
XOEN	5	RW	1	Crystal Oscillator Enable
PWRMODE	3:0	RW	0000	Powermode; see Table 3: PWRMODE Register States

NOTES: Before RST can be written to 1, the SPI interface of the chip needs to be reset. This is done by setting the SEL line to high.

The reference is enabled whenever the REFEN bit is one or the mode set by PWRMODE requires it (or both); the crystal oscillator is enabled whenever the XOEN bit is one or the mode set by PWRMODE requires it (or both). Normally, it is not necessary to set the REFEN or the XOEN bit, they can be programmed to zero. Since the crystal oscillator requires the reference, REFEN should be set whenever XOEN is set.

XTALOSC

This register controls the transconductance of the crystal oscillator. Optimal settings will depend on the characteristics of the specific crystal that is used. For a table containing the values as a function of the register settings see the AX5031 Datasheet.

Table 15. XTALOSC

Name	Bits	R/W	Reset	Description
XTALOSCGM	3:0	RW	0010	Transconductance of the Crystal Oscillator

For other crystal oscillator settings see the register XTALCAP.

Note that crystal oscillator settings should be chosen, that avoid amplitudes that exceed 0.5 V at pin CLK16P.

FIFOCTRL

This register is used to send control commands (depending on the selected frame mode) and holds the FIFO status information. For further FIFO settings see the registers FIFODATA, FIFOCOUNT, FIFOTHRESH and FIFOCONTROL2.

Table 16. FIFOCTRL

Name	Bits	R/W	Reset	Description
FIFOCMD	1:0	RW	11	FIFO command bits (written to FIFO during next write to FIFO-DATA); see section “Transmit” for exact operation of these bis
FIFO EMPTY	2	R	–	FIFO is empty if 1
FIFO FULL	3	R	–	FIFO is full if 1; if 1, the FIFO contains 32 words.
FIFO UNDER	4	R	–	FIFO under run occurred since last read of FIFOCTRL when 1. This bit is set when a read operation by the micro−controller (was attempted while the FIFO was empty.
FIFO OVER	5	R	–	FIFO over run occurred since last read of FIFOCTRL when 1. This bit is set when a write operation by the micro−controller was attempted while the FIFO was full.
FIFOSTAT	7:6	R	–	FIFO Status bits associated with current FIFO top word; see section “Transmit” for exact operation of these bis

FIFODATA

This register is used to read from and write to the 31 level x 10 bit FIFO. For further information on FIFO settings see section: “Transmit” and the register FIFOCTRL.

The FIFO can be accessed in powerdown mode.

Table 17. FIFODATA

Name	Bits	R/W	Reset	Description
FIFODATA	7:0	RW	–	FIFO access register

IRQMASK

This register allows to mask or de−mask interrupts. For further information on interrupt related settings see section: “Interrupts” and the registers IRQREQUEST and IRQINVERSION as well as PINCFG1 and PINCFG2.

Table 18. IRQMASK

Name	Bits	R/W	Reset	Description
IRQMFIFONOTEMPTY	0	RW	0	FIFO not empty interrupt enable
IRQMFIFONOTFULL	1	RW	0	FIFO not full interrupt enable
IRQMPLLUNLOCK	2	RW	0	Synthesizer lock lost interrupt enable
IRQMPLLRNGDONE	3	RW	0	Synthesizer auto−ranging done interrupt enable
IRQMFIFOTHRESH	4	RW	0	FIFO count ≥ threshold interrupt enable
IRQMFIFOERROR	5	RW	0	FIFO error (overrun or underrun) interrupt enable
IRQMTXBITCLOCK	6	RW	0	Transmit Bitclock interrupt enable

IRQREQUEST

This register indicates pending interrupts. For further information on interrupt related settings see section: “Interrupts” and the registers IRQREQUEST and IRQINVERSION as well as PINCFG1 and PINCFG2.

Table 19. IRQREQUEST

Name	Bits	R/W	Reset	Description
IRQRQFIFONOTEMPTY	0	R	–	FIFO not empty interrupt pending
IRQRQFIFONOTFULL	1	R	–	FIFO not full interrupt pending
IRQRQPLLUNLOCK	2	R	–	Synthesizer lock lost interrupt pending
IRQRQPLLRNGDONE	3	R	–	Synthesizer auto−ranging done interrupt pending

Table 19. IRQREQUEST

Name	Bits	R/W	Reset	Description
IRQRQFIFOTHRESH	4	R	–	FIFO count ≥ threshold interrupt pending
IRQRQFIFOERROR	5	R	–	FIFO error (overrun or underrun) interrupt pending
IRQRTXBITCLOCK	6	R	–	Transmit Bitclock interrupt pending

PINCFG1

This register allows to configure the SYSCLK and IRQ pins for application specific use.

Table 20. PINCFG1

Name	Bits	R/W	Reset	Description
SYSCLK	3:0	RW	1000	See Table 21.
IRQZ	5	RW	1	1: configure IRQ pin as input (tri−state) 0: configure IRQ pin as output This bit is only active when IRQE=1

Table 21. SYSCLK BIT VALUES

SYSCLK Bits	Meaning
0000	SYSCLK pin outputs static ‘0’
0001	SYSCLK pin outputs static ‘1’
0010	SYSCLK pin is an input (tri−state)
0011	SYSCLK pin outputs inverted f_{XTAL}
0100	SYSCLK pin outputs f_{XTAL}
0101	SYSCLK pin outputs $f_{XTAL}/2$
0110	SYSCLK pin outputs $f_{XTAL}/4$
0111	SYSCLK pin outputs $f_{XTAL}/8$
1000	SYSCLK pin outputs $f_{XTAL}/16$
1001	SYSCLK pin outputs $f_{XTAL}/32$
1010	SYSCLK pin outputs $f_{XTAL}/64$
1011	SYSCLK pin outputs $f_{XTAL}/128$
1100	SYSCLK pin outputs $f_{XTAL}/256$
1101	SYSCLK pin outputs $f_{XTAL}/512$
1110	SYSCLK pin outputs $f_{XTAL}/1024$
1111	SYSCLK pin outputs $f_{XTAL}/2048$

PINCFG2

This register allows to configure the IRQ pin to function as a General Purpose I/O (GPIO) pin rather than having its special default function.

IRQE is used to enable the special function of the IRQ pin or set it to GPIO. IRQI is used to set the state of the pin, if defined as GPIO and configured as output in PINCFG1. If the pin is configured as special function pin, then bit IRQI is used to chose if the output signal should be inverted.

Table 22. PINCFG2

Name	Bits	R/W	Reset	Description	
				GPIO pin	Special pin
IRQI	1	RW	0	0: set IRQ pin to ‘1’ 1: set IRQ pin to ‘0’	0: level high active interrupt 1: level low active interrupt
IRQE	5	RW	0	0: IRQ pin carries the interrupt signal 1: IRQ pin is a general purpose I/O (GPIO)	

PINCFG3

GPIO state register: This register holds the signals on the GPIO pins. (can be used to read back signals, if PINCFG1 configures the respective pin as input).

Table 23. PINCFG3

Name	Bits	R/W	Reset	Description
IRQPTTR	1	R	–	Logic State of IRQPTT Pin
SYSCLKR	4	R	–	Logic State of SYSCLK Pin

IRQINVERSION

This register allows to invert the logic levels of the level−triggered interrupts.

Table 24. IRQINVERSION

Name	Bits	R/W	Reset	Description
IRQINVFIFONOTEMPTY	0	RW	0	FIFO not empty interrupt inversion
IRQINVFIFONOTFULL	1	RW	0	FIFO not full interrupt inversion
IRQINVPLLUNLOCK	2	RW	0	Synthesizer lock lost interrupt inversion
IRQINVPLLRNGDONE	3	RW	0	Synthesizer auto−ranging done interrupt inversion
IRQINVFIFOTHRESH	4	RW	0	FIFO count ≥ threshold interrupt inversion
IRQINVFIFOERROR	5	RW	0	FIFO error (overrun or underrun) interrupt inversion
IRQINVTXBITCLOCK	6	RW	0	Transmit Bitclock interrupt inversion

MODULATION

This register sets the modulation type. For details on coding see also section: “Programming the Chip”.

Table 25. MODULATION

Name	Bits	R/W	Reset	Description
MODULATION	6:0	RW	0000010	See Table 26.

Table 26. MODULATION BIT VALUES

MODULATION Bits	Meaning
0000000	ASK
0000010	ASK Shaped
0000100	PSK
0000101	PSK Shaped
0000110	OQSK
0000111	MSK
10nnnnn	FSK; nnnnn = FSKMUL − 1
11nnnnn	FSK; nnnnn = FSKMUL − 1

TX operation is the same for all FSKMUL values. This coding for FSK is implemented for software compatibility with AX5051.

ENCODING

The register configures the encoder.

Table 27. ENCODING

Name	Bits	R/W	Reset	Description
ENC INV	0	RW	0	Invert data if set to 1
ENC DIFF	1	RW	1	Differential encode of data if set to 1
ENC SCRAM	2	RW	0	Enable scrambler if set to 1
ENC MANCH	3	RW	0	Enable manchester encoding. FM0/FM1 may be achieved by also appropriately setting ENC DIFF and ENC INV
ENC NOSYNC	4	RW	0	Disable synchronisation of 4−FSK symbols to byte boundaries in raw frame mode

The intention of the scrambler is the removal of tones contained in the transmit data, i.e. to randomize the transmit spectrum. The scrambler polynomial is $1 + X^{12} + X^{17}$, it is therefore compatible to the K9NG/G3RUH Satellite Modems.

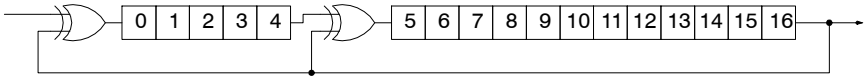

Figure 13. Scrambler Operation

Figure 13 shows a schematic circuit diagram for the scrambler. The numbered boxes represent a delay by one bit.

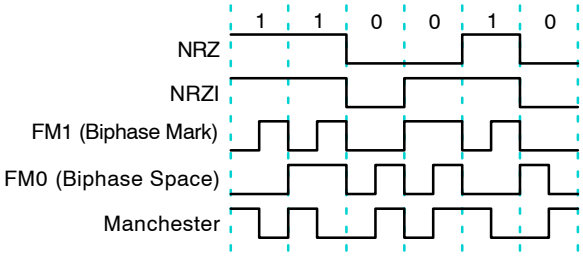

Figure 14. Customary Telecom Encoding Modes

Table 28. CUSTOMARY TELECOM MODES DESCRIPTION

Name	Bits	Description
NRZ	INV=0, DIFF=0, SCRAM=0, MANCH=0	NRZ represents 1 as a high signal level, 0 as a low signal level. NRZ performs no change
NRZI	INV=1, DIFF=1, SCRAM=0, MANCH=0	NRZI represents 1 as no change in the signal level, and 0 as a change in the signal level. NRZI is recommended for HDLC. The HDLC bit stuffing ensures that there are periodic zeros and thus transitions, and the encoding is inversion invariant, and therefore useable for PSK.
FM1	INV=1, DIFF=1, SCRAM=0, MANCH=1	FM1 (Biphase Mark) always ensures transitions at bit edges. It encodes 1 as a transition at the bit centre, and 0 as no transition at the bit centre.
FM0	INV=0, DIFF=1, SCRAM=0, MANCH=1	FM0 (Biphase Space) always ensures transitions at bit edges. It encodes 1 as no transition at the bit centre, and 0 as a transition at the bit centre.
Manchester	INV=0, DIFF=0, SCRAM=0, MANCH=1	Manchester encodes 1 as a 10 pattern, and 0 as a 01 pattern. Manchester is not inversion invariant.

Figure 14 shows a few well known encoding formats used in telecom and Table 28 describes them.

Guidelines:

- Manchester, FM0, and FM1 are not recommended for new systems, as they double the bit rate
- In HDLC mode, use NRZI, NRZI+Scrambler, or NRZ+Scrambler. If HDLC is to be transmitted over PSK, NRZI and NRZI+Scrambler are valid choices.
- In 802.15.4, use NRZ mode.
- In Raw modes, the choice depends on the legacy system to be implemented.

FRAMING

The register sets the framing mode and the CRC type.

Table 29. FRAMING

Name	Bits	R/W	Reset	Description
FRMMODE	3:1	RW	000	Defines framing type. See Table 30.
CRCMODE	5:4	RW	00	Defines the CRC type. See Table 31. This field is only available in HDLC mode.
HSUPP	6	RW	0	Suppress unneeded abort / flag / data indications. This field is only available in HDLC mode.

Table 30. FRAME MODE BIT VALUES

FRMMODE Bits	Meaning
000	Raw
001	Raw, Soft−Decision
010	HDLC
011	Raw, Preamble Match
110	802.15.4 900 MHz
111	Reserved for future use

Table 31. CRC MODE BIT VALUES

CRCMODE Bits	Meaning
00	CCITT (16 bit)
01	CRC−16
10	CRC−32
11	Invalid

CRCINIT3, CRCINIT2, CRCINIT1, CRCINIT0

This register can be used to set the reset value of the CRC calculation. Normally this register is left at all ones.

Table 32. CRCINIT3, CRCINIT2, CRCINIT1, CRCINIT0

Name	Bits	R/W	Reset	Description
CRCINIT	31:0	RW	0xFFFFFFFF	CRC reset Value; normally all ones

VREG

This contains status information of the internal voltage regulator.

Table 33. VREG

Name	Bits	R/W	Reset	Description
SREG	0	R	−	This bit is 1 if the voltage regulator is in high−power mode and the output voltage is > 2.3 V
SDS	1	R	−	1 if the voltage regulator start−up is complete
SSREG	2	R	−	Sticky version of SREG, meaning that this bit is 0 if it was 0 at any time since the last read access
SSDS	3	R	−	Sticky version of SDS, meaning that this bit is 0 if it was 0 at any time since the last read access

FREQ3, FREQ2, FREQ1, FREQ0, FREQB3, FREQB2, FREQB1, FREQB0

This register sets the carrier frequency.

Table 34. FREQ3, FREQ2, FREQ1, FREQ0, FREQB3, FREQB2, FREQB1, FREQB0

Name	Bits	R/W	Reset	Description
FREQ(B)	31:0	RW	0x3934CCCD	Frequency; FREQ = [$f_{CARRIER}/f_{XTAL} \cdot 2^{24} + ½$]

NOTE: Note that to program frequencies in the 433 MHz band carrier frequency registers must be programmed to appropriate values and the bit BANDSEL in the PLLLOOP register must be set to 1.
The device provides two frequency registers, to ease switching between multiple frequencies. The FREQSEL bit in the PLLLOOP register selects which frequency register is used.

FSKDEV2, FSKDEV1, FSKDEV0

This register is used to set the FSK frequency deviation.

Table 35. FSKDEV2, FSKDEV1, FSKDEV0

Name	Bits	R/W	Reset	Description
FSKDEV	23:0	RW	0x026666	FSK Frequency Deviation; FSKDEV = [$f_{DEVIATION}/f_{XTAL} \cdot 2^{24} + ½$]

NOTE: Note that $f_{DEVIATION}$ is actually half the deviation. The mark (bit=1) frequency is $f_{CARRIER} + f_{DEVIATION}$, the space (bit=0) frequency is $f_{CARRIER} - f_{DEVIATION}$.

$f_{DEVIATION} = h/2 \cdot BITRATE$

PLLLOOP

This register allows to configure the synthesizer loop bandwidth and the frequency band. For recommendations on settings see Table 6: Recommended synthesizer loop bandwidth settings.

Table 36. PLLLOOP

Name	Bits	R/W	Reset	Description
FLT	1:0	RW	01	Loop Filter configuration. See Table 37.
PLLCPI	4:2	RW	111	Charge pump current multiplier
BANDSEL	5	RW	0	Band selection. See Table 38.
FREQSEL	7	RW	0	Frequency Register selection. See Table 39.

Table 37. FILTER BIT VALUES

FLT Bits	Meaning
00	Invalid
01	Loop filter configuration with nominal bandwidth
10	Boosted loop filter configuration with x5 nominal bandwidth
11	Boosted loop filter configuration with x2 nominal bandwidth

Table 38. BAND SELECTION BIT VALUES

BANDSEL Bit	Meaning
0	868/915 MHz
1	433 MHz

Table 39. FREQUENCY REGISTER SELECTION BIT VALUES

FREQSEL Bit	Meaning
0	FREQ registers
1	FREQB registers

NOTE: Note that to program frequencies in the 433 MHz band registers the carrier frequency registers must be programmed to appropriate values and the bit BANDSEL in the PLLLOOP register must be set to 1.

PLLRANGING

This register is used to initiate ranging of the synthesizer VCO. It also holds the VCO range that is currently being used. For a description of the VCO ranging procedure see section: “Synthesizer VCO Auto−Ranging”.

Table 40. PLLRANGING

Name	Bits	R/W	Reset	Description
VCOR	3:0	RW	1000	VCO Range
RNG START	4	RS	0	Synthesizer VCO auto−ranging; Write 1 to start auto−ranging, bit clears when auto−ranging done
RNGERR	5	R	−	Ranging Error; this bit is set when RNG START transitions from 1 to 0 and the programmed frequency cannot be achieved
PLL LOCK	6	R	−	Synthesizer LOCK indicates the state of the synthesizer at the moment of the register access. Synthesizer is locked if 1
STICKY LOCK	7	R	−	STICKY LOCK indicates, the state of synthesizer since last read of the register. if 0, synthesizer lost lock after last read of PLLRANGING register

TXPWR

This register programs the transmit output power.

Table 41. TXPWR

Name	Bits	R/W	Reset	Description
TXRNG	3:0	RW	1000	Transmit Power, see AX5031 Datasheet for details.

TXRATEHI, TXRATEMID, TXRATELO

These registers set the transmit bit rate.

Table 42. TXRATEHI, TXRATEMID, TXRATELO

Name	Bits	R/W	Reset	Description
TXRATE	23:0	RW	0x09999A	Transmit Bitrate; TXRATE = [BITRATE/$f_{XTAL} \cdot 2^{24}$ + ½]

MODMISC

The behaviour of the transmitter if the synthesizer looses lock is set with this register.

Table 43. MODMISC

Name	Bits	R/W	Reset	Description
PTTLCK GATE	0	RW	1	If set to 1 then the transmitter is automatically disabled if the synthesizer looses lock

FIFOCOUNT

This register allows the micro−controller to obtain the number of words contained in the FIFO. FIFOCOUNT returns the number of words that can be read without underrun. Since the AX5031 contains a 32 level deep FIFO, the FIFO will contain 32 – FIFOCOUNT empty words. 32 – FIFOCOUNT can be written without an overrun error.

Table 44. FIFOCOUNT

Name	Bits	R/W	Reset	Description
FIFOCOUNT	5:0	R	------	Current number of FIFO words

FIFOTHRESH

This register specifies the FIFO count that must be exceeded to activate the FIFO threshold interrupt. That is, if IRQMFIFOTHRESH is one and FIFOCOUNT > FIFOTHRESH, an interrupt is requested. IRQINVFIFOTHRESH may be used to invert the sense of this interrupt.

Table 45. FIFOTHRESH

Name	Bits	R/W	Reset	Description
FIFOTHRESH	5:0	RW	000000	FIFO threshold

FIFOCONTROL2

This register specifies the action the transmitter should take on FIFO error, and allows the FIFO to be cleared.

If a FIFO error (an overrun or an underrun) occurs, the transmitter performs the action specified in STOPONERR, but does not change the PWRMODE register. Thus, to recover from the error, the software must first write SYNTHTX or STANDBY mode into the PWRMODE register, and then clear the overrun and underrun bits by reading FIFOSTAT.

Name	Bits	R/W	Reset	Description	
STOPONERR	1:0	RW	00	This bitfield determines what should happen on FIFO overrun or underrun	
				Bits	Meaning
				00	No action taken, transmitter continues
				01	Switch off transmitter, continue synthesizer
				10	Switch off transmitter and synthesizer, continue crystal oscillator
				11	Switch off everything
CLEAR	7	W	0	Clear the FIFO by writing 1. This bit is self clearing.	

XTALCAP

This register allows to program the tuning capacitor array at pins CLK16P and CLK16N.

Table 46. XTALCAP

Name	Bits	R/W	Reset	Description
XTALCAP	5:0	RW	000000	Crystal oscillator tuning capacitance

For the capacitance values see the AX5031 Datasheet.

Note that crystal oscillator settings should be chosen, that avoid amplitudes that exceed 0.5 V at pin CLK16P.

FOURFSK

This register is used to configure the 4−FSK mode.

Table 47. FOURFSK

Name	Bits	R/W	Reset	Description
FOURFSKENA	0	RW	0	Enable Four FSK Mode

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[1] ON Semiconductor. AX5031 Datasheet, see http://www.onsemi.com
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[4] Wikipedia. High−Level Data Link Control. http://en.wikipedia.org/wiki/HDLC

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